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SIGNAL PROCESSING STUDIES PROGRAM

**Digitally Controlled
Analog Signal Processing**

by
Randall L. Geiger
and
Edgar Sanchez-Sinencio

April 1988
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ABSTRACT

A design methodology for precision high-frequency monolithic continuous-time signal processing was introduced in the first phase of this project. The methodology applies local intelligence via a digital controller which precisely controls a continuous-time signal path. An architecture which ensued from this design methodology which is termed Digitally Controlled Analog Signal Processing (DCASP) has been introduced. The DCASP approach is inherently insensitive to nominal and statistical parameter variations, passive and active component mismatches, temperature variations, aging and parasitics. The DCASP architecture is amenable to adaptive applications and has potential to be used to implement in-field self-testing and/or correcting algorithms. The architecture is flexible, allowing for post fabrication establishment of system specifications. The flexibility along with the self-testing and/or correcting capabilities directly impact in a positive way both the reliability and cost of DCASP based systems.

In this report, the design and testing of a digitally controlled signal processor which is totally programmable and reconfigurable is discussed. This circuit forms the basic signal path of the DCASP architecture. The structure is capable of realizing filter transfer functions up to sixth order. An experimental version of this circuit was fabricated in a double polysilicon CMOS process. Experimental results show the resonant frequency and bandwidth of the filter circuits are digitally adjustable over a 3 decade range from 2khz to 2mhz. Resolution in resonant frequency over this entire range is to 0.5% or better and bandwidth resolution is to 1% or better.

The design and experimental performance of a general purpose digitally controlled Operational Transconductance Amplifier is also discussed. These circuits are used as the basic active elements in the DCASP filter structures but should find applications well beyond this project. These OTAs were fabricated in the same CMOS process and experimentally exhibited over two decades of adjustment range in the transconductance gain with a resolution of 1%. The fine resolution in gain of these structures was achieved through programmability of the tail voltage on the differential input stage and wide adjustment range through switch selection of output current mirror gain.

The design of sample and hold circuits are also discussed along with both parameter measurement and tuning algorithms. The sample and hold circuits are used in the performance detector section of the DCASP architecture. Finally, twenty test circuits which serve as building blocks in the subcomponents of the DCASP architecture are discussed from both theoretical and experimental viewpoints. These circuits were fabricated in a double polysilicon 3u CMOS process.

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GLOSSARY

A/D	Analog to Digital Converter
ADL	Address Decode and Latch
APdecode	Address Pre-Decode
Biquad	Second-Order Filter Structure
CSP	Controlled Signal Processor
CTA	Controlled Transconductance Amplifiers
DAC	Digital-To-Analog Converter
DCASP	The Digitally Controlled Analog Signal Processor (DCASP) is the complete signal processing system and is comprised of the Controlled Signal Processor (CSP), Performance Detector (PD), Exciter and Digital Controller. The DCASP architecture is depicted in Fig. 1.2-1.
DCASP-1	A CMOS integrated circuit which was fabricated in December 1986-January 1987. DCASP-1 contains only the CSP along with control circuitry. This was the first major test chip designed in this project.
DCASP-2	A CMOS integrated circuit which was fabricated in July-August 1987. DCASP-2 contains a CSP along with a preliminary Performance Detector. Several improvements and corrections over DCASP-1 were incorporated into the design of DCASP-2.
Fab. ID	ID Number for a specific MOSIS Process Run
$H(\omega)$	$H(\omega) = T(i\omega) $ is the function in the variable ω that equals the magnitude of $T(s)$ at $s = j\omega$.
Knots	The points in the domain of the spline functions where the function to the left differs from that to the right.
MOSIS	D.O.D./NSF IC Manufacturer
MOSIS ID	ID Number for a MOSIS Fabricated IC

ω'_o Approximate pole resonant frequency if system were exactly second-order. The exact definition of ω'_o is

$$\omega'_o = \sqrt{\omega_{3dB1}\omega_{3dB2}}$$

where ω_{3dB1} and ω_{3dB2} are the 3dB cutoff frequencies.

OpAmp Operational Amplifier

OTA Operational Transconductance Amplifier

PCA Programmable Capacitor Array

PSRR Power Supply Rejection Ratio

Q' Approximate pole Q if system were exactly second-order. The exact definition of Q' is

$$Q' = \frac{\sqrt{\omega_{3dB1}\omega_{3dB2}}}{\omega_{3dB2} - \omega_{3dB1}}$$

where ω_{3dB1} and ω_{3dB2} are the 3dB cutoff frequencies.

SPDT Single Pole Double Throw Switch

SPICE Circuit Analysis Program for IC's

SPST Single Pole Single Throw Switch

STA Controlled Transconductance Amplifier

T_{ACT} The actual system transfer function.

T_M A MODEL of the system. Ideally $T_M \cong T_{ACT}$.

$T_{MEAS}(s)$ The measured transfer function at the frequency s .

TAC Filters Filters comprised of Transconductance Amplifiers and Capacitors.

TTL Digital Logic Family

Tuning Host The tuning host is synonymous with the Digital Controller shown in the DCASP architecture of Fig. 1.2-1. The initial version of the tuning host is focused towards developing tuning algorithms and checking CSP functionality.

1.0 INTRODUCTION

In this report, the results of research efforts from March 1987 - September 1987 will be emphasized. This is an extension of work which was started in FY 1986 and which was reported in a final technical report dated 12/19/86. For reference purposes, a discussion of the Digitally Controlled Analog Signal Processing (DCASP) concept along with practical implications of this approach are presented in subsections 1.2 through 1.4 of this section. These are repeated from the final technical report dated 12/19/86.

The major focus on the first year of this project was on the development of the DCASP architecture and on the design of a Controlled Signal Processor (CSP) which comprises the digitally controllable analog signal path. The initial CSP structure selected was based upon using Transconductance Amplifiers and Capacitors to form the basic filter circuits. These are termed TAC Filters. This approach was selected because of the good high frequency performance characteristics of the Transconductance Amplifiers, the inherent availability of a method for digitally controlling the transconductance gain, and the existence of very simple and practical filter structures which can be synthesized with these devices. A first generation CSP was designed in a 3μ double polysilicon process. Silicon was available at the end of CY 1986.

Major effort during this fiscal year was placed upon testing and refining the CSP structure, investigating tuning algorithms, and on the design of a first-generation performance detector. Several test bars were fabricated for testing various subcircuits in the CSP and the performance detector. A second-generation CSP was also fabricated and tested.

There were several design errors on the initial CSP. The major affect of these errors was a limitation of the frequency adjustment range and the bandwidth adjustment range of the filter. Beyond these limitations, the circuit performed as expected. Experimental results are presented later in this report.

Classical tuning algorithms were investigated. These were all plagued by either convergence problems or tended to converge to unacceptable local minimums. A new approach to tuning which does not rely upon the conventional rational fraction approximation has been proposed. Simulations indicate this approach may circumvent some of the convergence problems which plague conventional algorithms in a useful class of applications.

A performance detector based upon a generic A/D converter has been investigated. This structure uses a fast sample and hold amplifier in conjunction with a slow speed A/D converter. Subcircuits which comprise this performance detector have been designed and fabricated. Results are presented later in this report.

1.1 PRACTICAL IMPLICATIONS OF DCASP SYSTEMS

A very high speed real-time precision signal processing capability is crucial for the successful development of a viable strategic defense system. The evolution of the signal processor proposed here has potential for real-time applications at frequencies which are approximately two orders of magnitude higher than can be attained by following a conventional microprocessor based strategy. The structures proposed are versatile, economical to produce, and physically and technologically compatible with existing VLSI technologies. They are inherently insensitive to processing variations, device matching and environmental parameters.

Beyond applications at very high frequencies where alternative signal processing techniques do not exist, a host of medium and low frequency analog signal processing applications exist in which precision and reliability throughout the life of the system is crucial for the viability of the system. Most existing analog instrumentation relies either upon factory-set calibration and/or periodic costly field tuning and/or selective self-calibration of some specific sub-components. The technology for automatic full system testing and subsequent automatic system calibration for drifts due to component aging, temperature variations or component failure has not evolved. The result is development and utilization of systems with suboptimal reliability and the associated implementation of costly personnel intense and humanly subjective maintenance programs which invariably miss some faulty systems. Furthermore, much of the electronic equipment which is actually removed from shipboard service for replacement and/or alignment is not faulty. This results in an unnecessary load on the logistic support system, especially supply support and training requirements. The adverse impact on both the economics and strengths of our military systems should be apparent.

Monolithic circuits capable of precision continuous-time signal processing have largely eluded IC designers for the past decade. This can be attributed primarily to the inability of researchers to solve many of the numerous technological challenges associated with analog processing. It is precisely these precision circuits along with on-chip local intelligence that are needed to build precision analog systems which operate at high frequencies and which are economical, reliable and capable of performing on-line self-testing and/or self-correcting functions.

It is the goal of this overall research effort to develop the methodologies and architectures necessary to design precision reliable monolithic analog circuits which are useful for a wide range of applications which have the on-chip intelligence needed to implement self-testing and/or self correcting algorithms. A preliminary architecture of a versatile structure suitable for a wide range of applications is discussed in the following two sections followed by the specific objectives of the first year of this research effort.

1.2 DCASP ARCHITECTURE

A preliminary analog signal processing architecture which can be used for a wide range of applications over a large range of frequencies is shown in Fig. 1.2-1. This structure is inherently capable of compensating for the major factors which have limited the development of precision reliable monolithic continuous-time integrated circuits. Specifically, the structure compensates for nominal process parameter variations, statistical process parameter spreads, temperature coefficients, parasitic resistors and capacitors, passive and active component matching as well as device aging. The structure is amenable to adaptive applications as well as self-testing and/or self-correcting. The architecture utilizes a precisely controllable analog signal path and a sophisticated digital controller in a control loop and is termed a Digitally Controlled Analog Signal Processor (DCASP). Within a predetermined range, both the functional characteristics and specifications of the analog signal processor can be established via software input after silicon processing and packaging are complete. Details about operation of the DCASP structure are presented in the following section. The structure is applicable from low frequencies to very high frequencies. The DCASP is compatible with and scales with existing VLSI technologies.

The magnitude of the problem facing the designer attempting to implement precision continuous-time signal processing algorithms can be best appreciated by considering the typical magnitude of the major factors listed previously and repeated in Table 1.2-1 which limit circuit performance. For comparative purposes, emphasis will be placed on silicon MOS processes although similar phenomena are observed in other technologies.

Parameter variations from the design target associated with processing are quite large. $\pm 50\%$ variations in sheet resistances, $\pm 100\text{mv}$ variations in threshold voltages of MOSFETs and $\pm 10\%$ variations in oxide capacitor values are typical. Variations in the transconductance parameter K' ($K' = \mu C_{ox}$) of tens of percent are also common.

Chip level statistical parameter variations are somewhat smaller than the process parameter variations but are still significant. These variations are due to both local and global differences in the characteristics of silicon systems across the die. Variations (mean standard deviation) of threshold voltages are in the 1mv to 20mv range [1-4] and variations in K' range from 0.5% to 5% .

Temperature coefficients of passive and process parameters are significant. For example, the TCR of the sheet resistance of polysilicon is typically in the $0.1\%/^{\circ}\text{C}$ range.

Parasitic capacitors from plate to substrate associated with poly-poly capacitors are in the 1% to 30% range of the capacitor itself. Inherent parasitic resistors associated with poly strings, contacts and drain and source diffusions range upward from tens of ohms. Layout parasitics associated with interconnections are often somewhat larger. The parasitic capacitances associated with resistor strings are typically both distributed and voltage dependent.

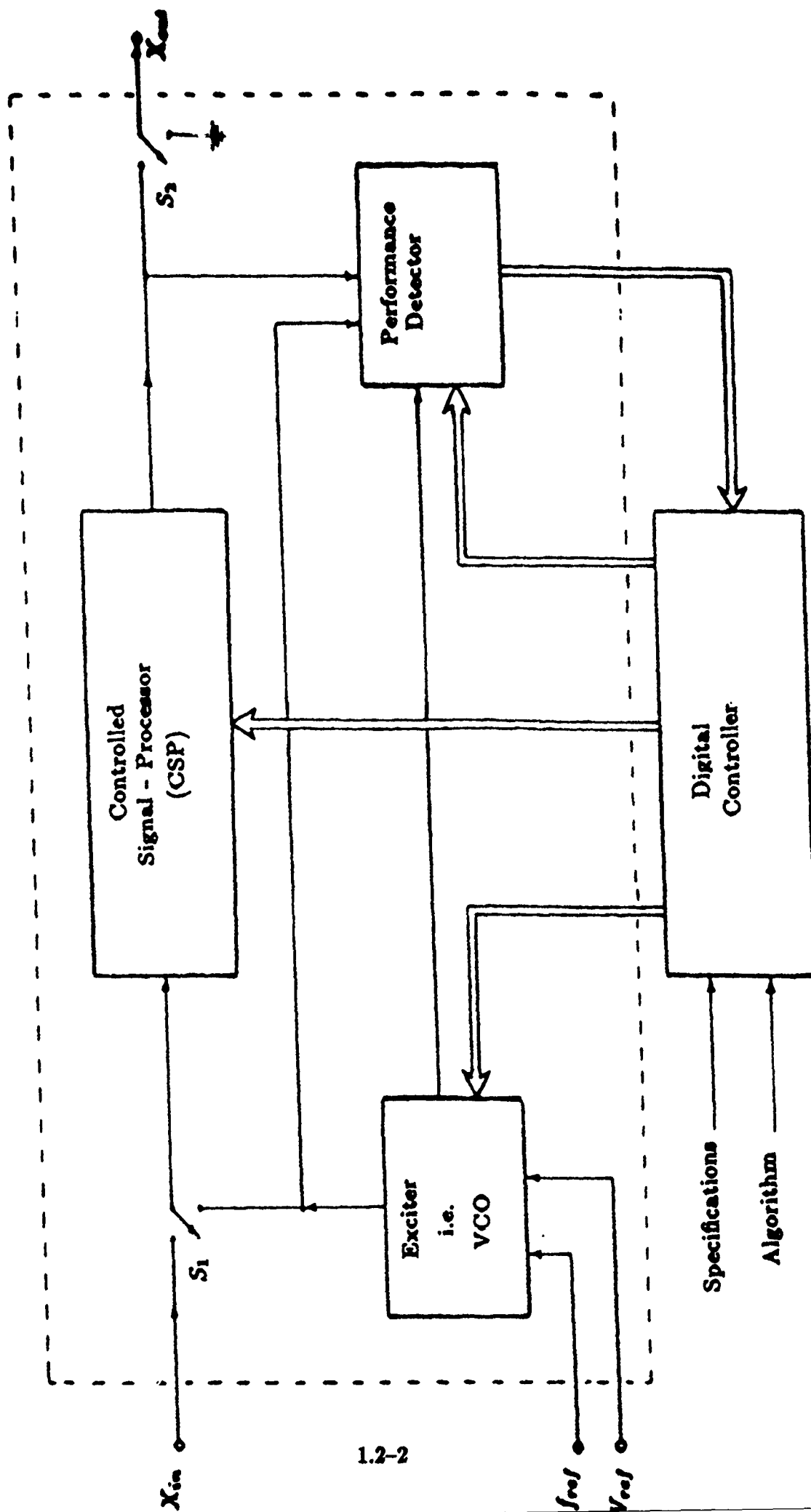


Fig. 1.2 1: DCASP Architecture

With considerable care in layout, ratio matching of capacitors to $\pm 0.1\%$ [3,5] is possible. Practical resistor ratio matching is in the $\pm 1\%$ to $\pm 2\%$ range (5 micron feature size) [6,7]. Accurate ratio matching of parasitic components is more difficult.

Active component matching is poorer than passive component matching. If the device of Fig. 1.2-2 or some derivative structure is used as a resistor, as has been suggested by several investigators working on continuous-time monolithic filters [8-11], the effective impedance (for small voltages) is approximated by

$$R_{FET} \simeq \frac{L}{WK'(V_{GS} - V_T)} \quad (1)$$

and hence the percent change in R_{FET} can be approximated by

$$\frac{\Delta R_{FET}}{R_{FET}} \simeq \frac{\Delta L}{L} - \frac{\Delta W}{W} - \frac{\Delta K'}{K'} + \frac{\Delta V_T}{V_{GS} - V_T} \quad (2)$$

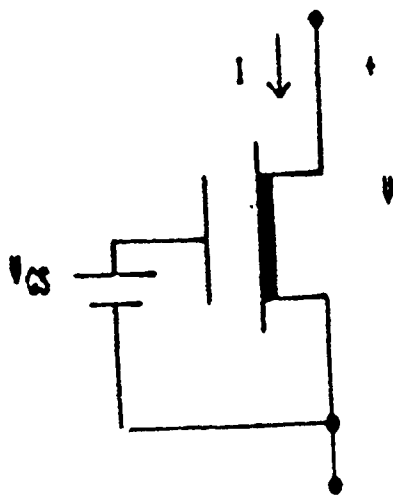
If all variables on the right hand side of (2) are assumed independently distributed, then the mean standard deviations of $\frac{\Delta R_{FET}}{R_{FET}}$ is approximately the square root of the sum of the individual variances of the terms on the right hand side of this equation. From the comments made above, it follows that even if $\frac{\Delta L}{L}$ and $\frac{\Delta W}{W}$ effects are neglected the standard deviation of $\frac{\Delta R_{FET}}{R_{FET}}$ is in the .6% to 6% range (for $V_{GS} - V_T \simeq 1v$).

The seriousness of the limitations of the factors in Table 1.2-1 can be appreciated only when one considers the specifications required in typical practical applications. Suffice it to say that many applications exist in all frequency ranges from low audio to several GHz if effective RC products or component ratios can be *practically controlled* to between 0.1% and 1% accuracy. For notational convenience, this will be termed the medium precision range. High precision will be denoted by corresponding accuracy requirements to better than 0.1% and low precision will be denoted by those applications requiring less than 1% accuracy. By practically controlled, it is meant that the cost of fabricating (including trimming if required) the die is low and the yield, as determined by faults and component variations due to both processing and temperature, is high. For example, if one expects to obtain a respectable yield in applications which require control of the standard deviation of RC products to within the 0.01% to 1% range, it is crucial that the individual parameter variances that determine the RC products and which contribute in approximately the root mean squared sense to the overall standard deviation are also constrained to this range or tighter.

None of the medium precision applications can be practically addressed without good compensation for nominal process parameter variations. Minimal practical impact can be anticipated in the medium precision range for design techniques which don't have inherent compensation for all factors listed in Table 1.2-1 with the possible exception of passive (capacitive) component matching. Applications in the high precision range require inherent compensation for *all* factors listed in Table 1.2-1.

1. Nominal Process Parameter Variations
2. Statistical Process Parameter Spreads
3. Large Temperature Coefficients
4. Parasitic Resistors and Capacitors
5. Passive Component Matching
6. Active Component Matching
7. Device Aging

Table 1.2-1: Major Passive Factors Limiting Performance of Monolithic Analog Circuits.



$$R_{FET} \approx \frac{L}{K'W(V_{GS} - V_T)}$$

Fig. 1.2-2. Active Resistor

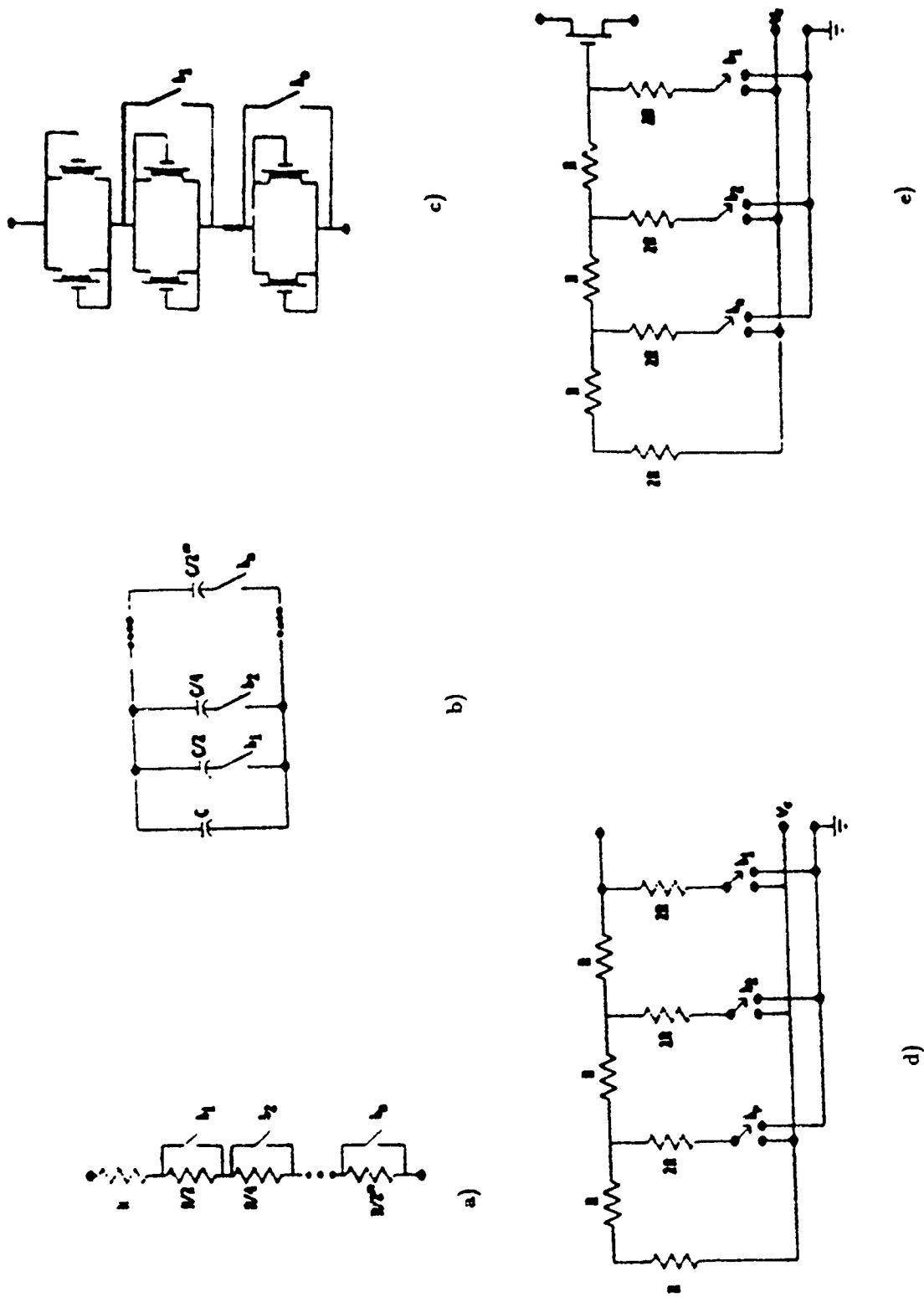


Fig. 1.3-1. Digitally Controlled Circuit Components a) Binary Resistor b) Binary Capacitor c) Active Resistor
d) R-2R Ladder e) Digitally Controlled MOSFET.

A discussion of alternative state of the art approaches to monolithic continuous-time signal processing can be found in [12] which is included in the Appendix along with comments about the inherent limitations of these techniques which have limited precision applications to low frequencies and essentially precluded the evolution of high-frequency structures.

1.3. DCASP OPERATION

The block diagram of the DCASP architecture of Fig. 1.2-1 contains four basic components, the Controlled Signal Processor (CSP), the Performance Detector, the Exciter, and the Digital Controller. The first three components enclosed in the dashed curves represent analog circuitry that will appear on a single substrate. The Digital Controller may also be on the same substrate or may be external. The switch, S_1 , allows either the input signal or the output of the Exciter to be applied to the Controlled Signal Processor itself.

The basic operation of the system is very simple. S_1 is initially connected to the Exciter output. In this mode the Digital Controller "identifies" the Controlled Signal Processor by simultaneously identifying the three analog blocks: The Exciter, the Performance Detector, and the Controlled Signal Processor. Once the CSP is identified, the controllable components in the CSP are adjusted and latched to optimize performance of the CSP relative to the given specifications. Following optimization, S_1 changes states allowing the input signal to be applied to the CSP. All signal processing then takes place in the optimized analog CSP. Comments about the operation of each of the blocks and the overall system follow.

The Controlled Signal Processor should be designed to allow for adjustment of a large number of key parameters and functions. Large adjustment range and fine resolution for all components is important. For example, if the CSP is designed to act as a filter, a group of multiple input lossy integrators in which the loss and the unity gain frequency associated with each input are all independently adjustable over a wide range might serve as the basis for the CSP. By appropriately interconnecting these devices via the Digital Controller and adjusting the components to optimize performance, a universal precision filter structure is possible. For audio frequency applications, the adjustable components might be binarily weighted resistors and capacitors or switched capacitors such as shown in Fig. 1.3-1. or higher-level programmable structures such as Operational Transconductance Amplifiers (OTAs) [13]. Continuously adjustable rather than quantized components are also possible. A typical grid (in the s -plane) depicting by intersection of grid lines the possible pole locations of a filter constructed using this technique with quantized component values is shown in Fig. 1.3-2. Methods of selecting the adjustable quantized components to obtain maximal resolution for specific applications are considered in [14].

The Exciter provides an excitation or sequentially, multiple excitations for the CSP during the identification state. Depending on the application, typically only f_{ref} or V_{ref} will be required. The exact value of these references is not critical but they must be known and stable. The identification and optimization problem simplifies if multiple inputs (but a fixed single reference) are sequentially applied by the Exciter. Considering again the filter example, the Exciter may consist only of a non-precision voltage-controlled oscillator (VCO). The Digital Controller is used to sequentially set the Exciter (i.e., VCO) operating frequency. The "exact" frequency of oscillation for each step in the VCO sequence is not critical but can be precisely determined with a modest amount of circuitry if f_{ref} is known.

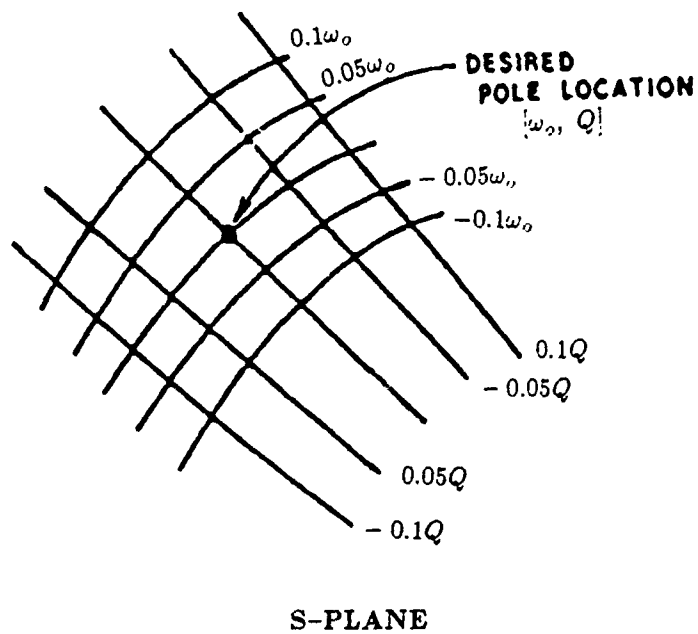


Fig. 1.3-2. Possible pole locations in a DCASP based active filter.

The Performance Detector is used to measure the performance of the CSP itself. If one were to attempt to identify only the CSP, the required specifications for the design of the Performance Detector would typically be quite challenging. By also identifying the Performance Detector and Exciter, the specifications required for these devices will be modest. For algorithmic simplicity, the Performance Detector may also be made to be tunable by the Digital Controller. Considering again the filter example, the Performance Detector may be no more than a voltage comparator or a generic analog to digital converter. Nonideal characteristics of the Performance Detector, such as offset voltages (as a function of common mode input) may be identified and/or adjusted by the Digital Controller. Slew rate and hysteresis effects may also be identified or, in some applications, ignored.

The Digital Controller is used to monitor the performance of the system during the identification or pretune state. Based upon the output of the Performance Detector for each excitation supplied by the Exciter, the system is adjusted to optimally meet the specifications established for the CSP. The desired specifications must be stored in nonvolatile memory. For high-volume applications, tuning algorithms may be fixed in hardware. Once tuned, the Digital Controller may either power-down or enter a standby state in which it monitors portions of the system. Since the Digital Controller is not in the signal path, it is not needed for real-time operation. Since the pretune speed is typically not critical, the size and capabilities of the controller can be quite modest. Tradeoffs between algorithmic tuning complexity and capabilities of the Digital Controller can be made.

Referring back to the technological limitations of Table 1.2-1 which plague the continuous-time IC designer, it should be apparent that if an acceptable tuning strategy can be developed, and if the CSP has sufficient range and resolution so that the domain of realizable specifications (henceforth termed the tuning domain) intersects with the desired specifications (henceforth termed the tuning domain), then the DCASP structure will be inherently unaffected by nominal process parameter variations, statistical process parameter spreads, parasitic resistors and capacitors as well as passive and active component matching.

If temperature changes after the initial trimming, several alternatives exist for temperature compensation. In those applications where the signal path can be periodically interrupted, the CSP structure can be re-calibrated. The Digital Controller can also monitor die temperature and make on-line corrections based upon nominal temperature characteristics of the devices. A dual signal path architecture in which the input signal is alternately applied to the two paths and in which the un-excited path is off-line calibrated is also possible.

1.4. APPLICATION OF THE DCASP TO FILTERING

A simple example may prove useful in demonstrating the principle of operation of the DCASP. Consider the desired magnitude and phase response of a filter with k adjustable elements as depicted in Fig. 1.4-1. The performance of the CSP would be measured via the Performance Detector at frequencies f_1, \dots, f_n . The exact values of these frequencies can be precisely determined from knowledge of f_{ref} . The simulated measured magnitude and phase characteristics at each of these frequencies as determined by the Performance Detector are also shown in the figure. Based upon the measured characteristics, the Digital Controller will then adjust the k (typically $n > k$) controllable elements in the CSP to optimize the filter performance relative to the user determined cost function.

Assuming each adjustable element in the CSP has r binary bit tuning capability, there are $N = (2^r)^k$ possible settings of the controllable elements. N increases very rapidly with k and r . It may well be the case that a large number of different settings will satisfy a given set of specifications. The tuning algorithm need not necessarily obtain the optimal setting. It should be observed from this example that the adjustments made by the Digital Controller need not be restricted to single-pass monotonic trims as is often the case for hybrid thick and thin film circuit trimming. A sequential bi-directional trim strategy may offer reduced trim complexity and quicker convergence than a single-pass scheme.

1.5. OBJECTIVES

The stated objectives of this research are to develop practical design methodologies and architectures for precision real-time monolithic analog circuit design which can be used to implement self-testing/self-correcting and in-field self-calibration algorithms.

The specific goals for this fiscal year as itemized in the Statement of Work are to focus on the experimental evaluation of the Controlled Signal Processor and on the design and experimental evaluation of a monolithic performance detector. Both of these goals were achieved and considerable progress towards meeting the stated objectives beyond the specific goals for this fiscal year was made.

Specifically, the first generation Controlled Signal Processor was experimentally evaluated. Basic performance was as predicted by simulations. A second generation Controlled Signal Processor was designed, fabricated and tested. This second generation structure offered significant improvements in both frequency adjustment range and Q adjustment range over the initial CSP. The resolution was also improved.

A subcomponent of the CSP which should also find applications well beyond this project was developed. Specifically, an operational transconductance amplifier with provisions for large input signal swings, wide g_m adjustment range and good high frequency performance was developed, fabricated and tested.

Architectures for the monolithic performance detector were investigated. A structure based upon a fast sample and hold and a low frequency A/D converter was selected. The key building blocks which comprise the performance detector were designed, fabricated and tested.

The tuning problem was investigated. Algorithms for measuring the system gain at fixed frequency points were developed. Methods of accurately determining key system performance parameters based upon measurements at a finite set of frequencies were investigated. Computer simulations suggest that tuning algorithms based upon using the predicted performance parameters which are applicable for a useful class of systems can be developed.

2.0 DISCUSSION

A block diagram of the basic DCASP architecture was shown in Fig. 1.2-1. of Sec. 1.2. The major effort during the past year focused on the design of the Controlled Signal Processor and the Performance Detector. Algorithms for gain determination and measuring performance characterization parameters were also investigated.

Section 2.1 concentrates on the design of the Controlled Signal Processor. The design of both the operational transconductance amplifiers and the capacitor arrays which comprise the CSP are discussed.

The Performance Detector is discussed in Sec. 2.2 This component is addressed from both the data interpretation and hardware implementation viewpoints.

A preliminary discussion of the tuning problem appears in Sec. 2.3. Several different approaches to tuning are characterized.

A preliminary discussion of a tuning host which comprises a portion of the digital controller in the basic DCASP architecture is presented in Sec. 2.4. This tuning host will be used as a vehicle for testing different tuning algorithms in the next phase of this research effort.

A discussion of the memory mapping between the digital control words and the CSP parameters appears in Sec. 2.5. The address mapping to each of the control latches is also discussed.

Finally, several basic functional blocks which are used in the design of the CSP and Performance Detector were designed, fabricated and tested. These are useful for determining the performance limitations of the CSP and Performance Detector as well as optimizing next generation designs. Some of these blocks are discussed in Sections 2.1 and 2.2 and the remainder are summarized in the discussion of experimental testing in Sec. 5.0.

2.1 Controlled Signal Processor (CSP)

As the name implies, the CSP is that portion of the DCASP chip which processes the input voltage signal, yielding an output signal which is related to the input by the transfer function, $H(s) = \frac{V_o(s)}{V_i(s)}$. As seen in the block diagram of Fig. 2.1-1, the CSP includes three cascaded biquad structures. Each biquad implements a second-order transfer function; thus, the CSP may implement sixth-order transfer functions.

The cascaded biquad approach was adopted to simplify the tuning procedure. The CSP structure contains analog switches which allow an external input signal to be directed to any of the three biquad inputs. The corresponding biquad output may be directed to the performance detector, allowing each biquad to be tuned individually. As will be seen in Section 2.3, the tuning of these second-order structures (biquads) is not a trivial problem. The problem of directly tuning a higher-order structure is even more involved. For this reason, the cascaded biquad approach was selected, even though alternate sixth-order structures might considerably simplify the circuitry. The cascaded biquad approach may be easily extended to implement higher-order structures.

In addition to the signal voltage, the CSP has as inputs the digital address, data, and control lines of the DCASP system bus. These allow for the reception of the digital data which set the biquad transfer functions and which set the appropriate analog switches to achieve the desired interconnections in the CSP.

Subdivisions of the CSP are discussed in the following sections, beginning with the filter biquad. The key block in the biquad is the controlled transconductance amplifier (CTA). The CTA is further divided into an operational transconductance amplifier (OTA) and a digital-to-analog converter (DAC). The biquad also includes programmable capacitor arrays (PCA's) and a buffer.

The basic architecture of the CSP is the same for both DCASP-1 and DCASP-2; i.e., all block diagrams presented in these sections are essentially the same for both DCASP implementations. However, significant design modifications were made to the OTA, DAC, and PCA. These changes greatly increase the range of transfer functions which can be realized by the biquad and, hence, by the CSP. Unless specifically stated to the contrary, it will be assumed that all discussions about the CSP and the building blocks comprising the CSP in this Section (Section 2.1) are in reference to DCASP-2.

2.1.1 Filter Biquad

The biquad is itself a controlled signal processor; a single biquad is capable of realizing

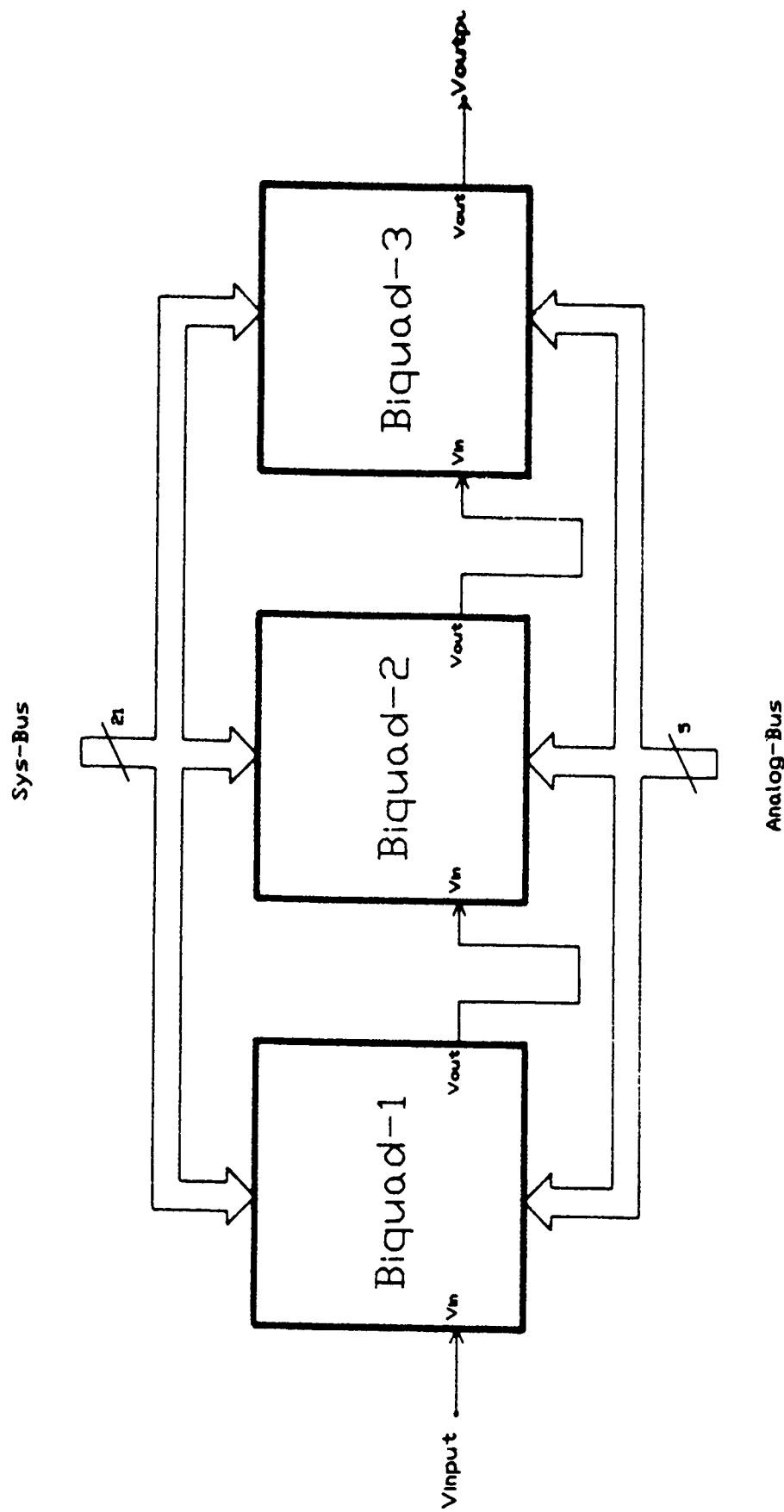


Fig. 2.1-1: CSP Block Diagram

second-order transfer functions of the form

$$\frac{V_{out}}{V_{in}} = \frac{s^2 + BW_z s + \omega_z^2}{s^2 + BW_p s + \omega_p^2} \quad (2.1 - 1)$$

where ω_p and ω_z are the pole and zero frequencies and $(BW)_p$ and $(BW)_z$ are the pole and zero bandwidths. Analog switches are provided which allow the biquad to realize any one of several common transfer functions by eliminating the s^2 , s^1 , or s^0 term(s) in the numerator of (2.1-1); for example, the s^2 and s^1 numerator terms may be eliminated to yield the transfer function of a lowpass filter.

A diagram of the biquad used in DCASP-1 and DCASP-2 is shown in Fig. 2.1-2. It contains five controlled transconductance amplifiers (CTA's), two programmable capacitor arrays (PCA's), an analog buffer, and several analog switches. The biquad is actually a modified two integrator loop structure with the integrators being comprised of an OTA loaded by a capacitor [15]. The transfer function may be written as

$$\frac{V_{out}}{V_{in}} = \frac{(B_{hp})s^2 + \left(\frac{g_{m4} - g_{m3}B_{bp}}{C_7}\right)s + \left(\frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7}\right)}{s^2 + \left(\frac{g_{m5}}{C_7}\right)s + \frac{g_{m2}g_{m3}}{C_6C_7}} \quad (2.1 - 2)$$

where the B variables can assume the value of either 0 or 1 depending upon the switch settings. Table 2.1-1 lists the switch settings and the conditions on the g_m which will result in the realization of various common transfer functions.

Comparison of (1) and (2) yields the following relationships:

$$\omega_p = \sqrt{\frac{g_{m2}g_{m3}}{C_6C_7}} \quad (2.1 - 3a)$$

$$(BW)_p = \frac{g_{m5}}{C_7} \quad (2.1 - 3b)$$

$$\omega_z = \sqrt{\frac{g_{m1}g_{m3} + g_{m2}g_{m3}B_{lp}}{C_6C_7}} \quad (2.1 - 3c)$$

$$(BW)_z = \frac{g_{m4} - g_{m3}B_{bp}}{C_7} \quad (2.1 - 3d)$$

Adjustment of these frequencies and bandwidths is accomplished by the adjustment of the appropriate g_m 's and/or capacitances. The CTA permits both a "fine" and a "coarse" adjustment of g_m , with the coarse g_m adjustment being capable of producing a much more significant (i.e., greater magnitude) change in g_m than the fine adjustment. Thus, fine and coarse control of the frequencies and bandwidths may be achieved by the fine and coarse adjustment of the g_m 's. The control of the frequencies and bandwidths via the adjustment of the capacitance of a PCA is also considered to be a coarse control, as the change produced in this way is generally more significant than the change obtained with the fine g_m adjustment.

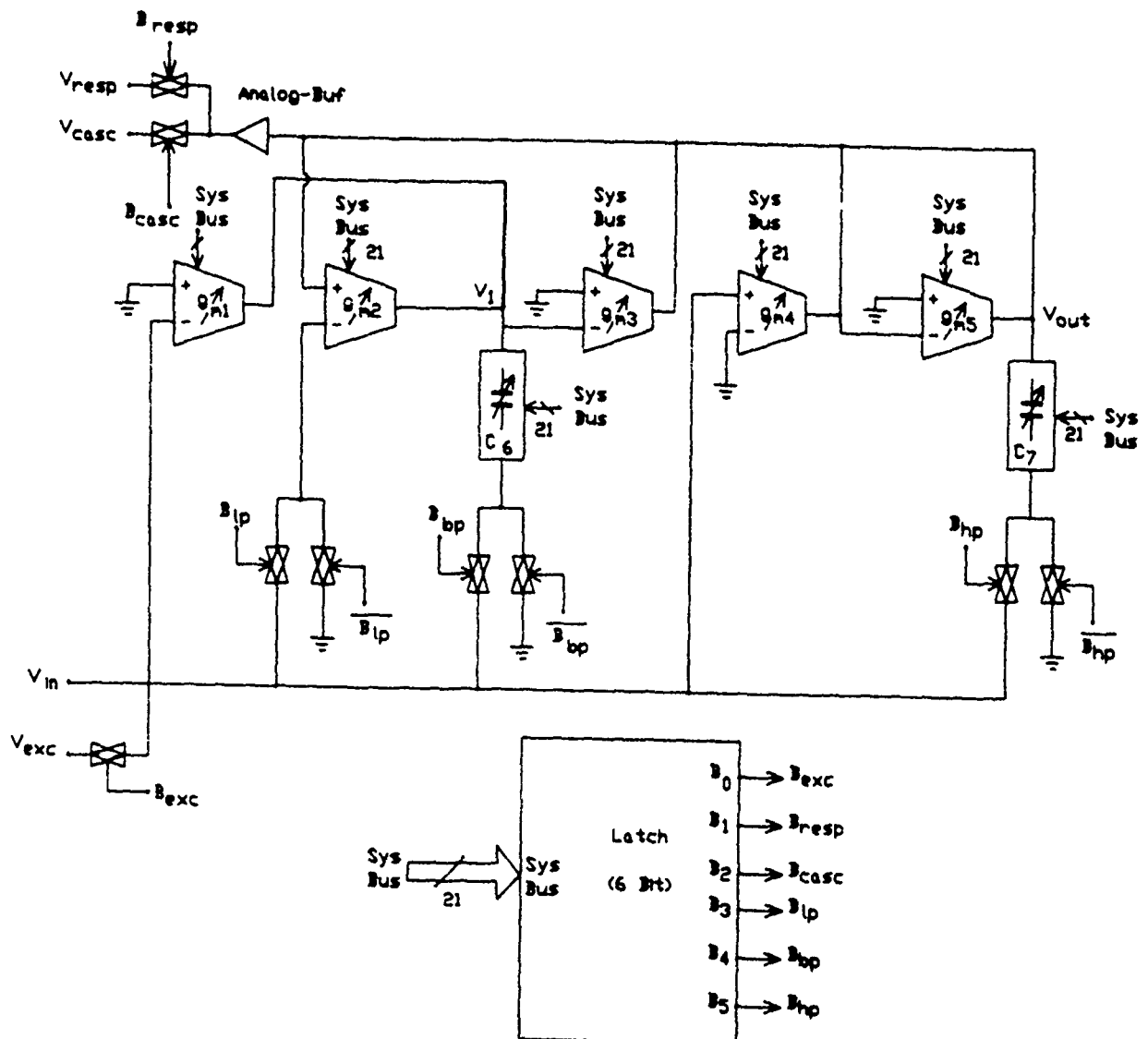


Fig. 2.1-2: Biquad Block Diagram

Table 2.1-1: Biquad settings for common transfer functions.

	B_{hp}	B_{bp}	B_{lp}	Special Conditions
Highpass(HP)	1	0	0	$g_{m1} = g_{m4} = 0$
Bandpass (BP)	0	0 or 1	0	$g_{m1} = 0$
Lowpass (AP)	0	0	0 or 1	$g_{m4} = 0$
Allpass (AP)	1	1	1	$g_{m1} = g_{m4} = 0$ $g_{m3} = g_{m5}$
Lowpass Notch (LPN)	1	0	1	$g_{m4} = 0$ $g_{m1} > g_{m2}$
Highpass Notch (HPN)	1	0	0	$g_{m4} = 0$ $g_{m1} < g_{m2}$

Note from (2.1-3) that the fine adjustment of g_{m5} will result in a fine adjustment of $(BW)_p$ without affecting $(BW)_z$, ω_p , or ω_z . Similarly, g_{m4} may be used to adjust $(BW)_z$ without affecting the other three parameters. For the case of the resonant frequencies, however, the situation is complicated by the fact that for $B_{lp} = 1$, both ω_p and ω_z are functions of g_{m2} and g_{m3} . The fine adjustment of these frequencies may be handled by first adjusting ω_p using g_{m2} , then adjusting ω_z using g_{m1} .

The coarse control of the g_m 's and capacitances is responsible for the wide range of frequencies and bandwidths which can be realized by the biquad. The g_m of the OTA used in the biquad is adjustable from $0.19\mu S$ to $43\mu S$ and the programmable capacitor can be adjusted from $2.39pF$ to $24.4pF$ for the specific implementation used in the DCASP-2 design. Fig. 2.1-3 shows the corresponding range of attainable pole frequencies and pole bandwidths for the biquad. The attainable pole frequency range is seen to be from less than 2kHz to greater than 2MHz; the attainable pole bandwidths range is essentially the same.

The points in Fig. 2.1-3 were generated simply by using (2.1-3a) and (2.1-3b) to calculate ω_p and $(BW)_p$ for all coarse values of g_{m2} , g_{m3} , g_{m5} , C_6 , and C_7 . However, due to signal amplitude saturation on an internal node in the biquad, it is not practical to implement transfer functions using some of these g_m and C combinations. Specifically, signal amplitudes at the output of g_{m1} and g_{m2} in Fig. 2.1-2 must be limited ($< 4V_{p-p}$) in order to prevent excessive distortion of the signal.

The voltage, V_1 , at the internal node is related to the input voltage by the following equation:

$$\frac{V_1}{V_{in}} = \frac{B_{bp}s^2 + \left(\frac{g_{m2}B_{hp} - g_{m2}B_{lp} - g_{m1}}{C_6} + \frac{g_{m5}B_{bp}}{C_7} \right) s + \left(\frac{g_{m2}g_{m4} - g_{m1}g_{m5} - g_{m2}g_{m3}B_{bp} - g_{m2}g_{m5}B_{lp}}{C_6C_7} \right)}{s^2 + \frac{g_{m5}}{C_7}s + \frac{g_{m2}g_{m3}}{C_6C_7}} \quad (2.1-4)$$

From (2) and (4), the voltage at the internal node is related to the biquad output voltage as

$$\frac{V_1}{V_{out}} = \frac{B_{bp}s^2 + \left(\frac{g_{m2}B_{hp} - g_{m2}B_{lp} - g_{m1}}{C_6} + \frac{g_{m5}B_{bp}}{C_7} \right) s + \left(\frac{g_{m2}g_{m4} - g_{m1}g_{m5} - g_{m2}g_{m3}B_{bp} - g_{m2}g_{m5}B_{lp}}{C_6C_7} \right)}{(B_{hp})s^2 + \left(\frac{g_{m4} - g_{m3}B_{bp}}{C_7} \right) s + \left(\frac{g_{m1}g_{m3} + g_{m2}g_{m5}B_{lp}}{C_6C_7} \right)} \quad (2.1-5)$$

One way to avoid distortion at the internal node, while maintaining the maximum output voltage range, is to stipulate that the magnitude $\left| \frac{V_1(s)}{V_{out}(s)} \right|$ be no greater than 1 throughout the frequency range of interest. Actually, we would prefer to stipulate that $|V_o(j\omega)|$ and $|V_1(j\omega)| \leq V_{REF}$ for all ω where V_{REF} is some acceptable peak signal amplitude.

Figures showing the attainable pole frequencies and pole bandwidths which satisfy the condition

$$\left| \frac{V_1(s)}{V_{out}(s)} \right|_{s=j\omega_p} \leq 1 \quad (2.1-6)$$

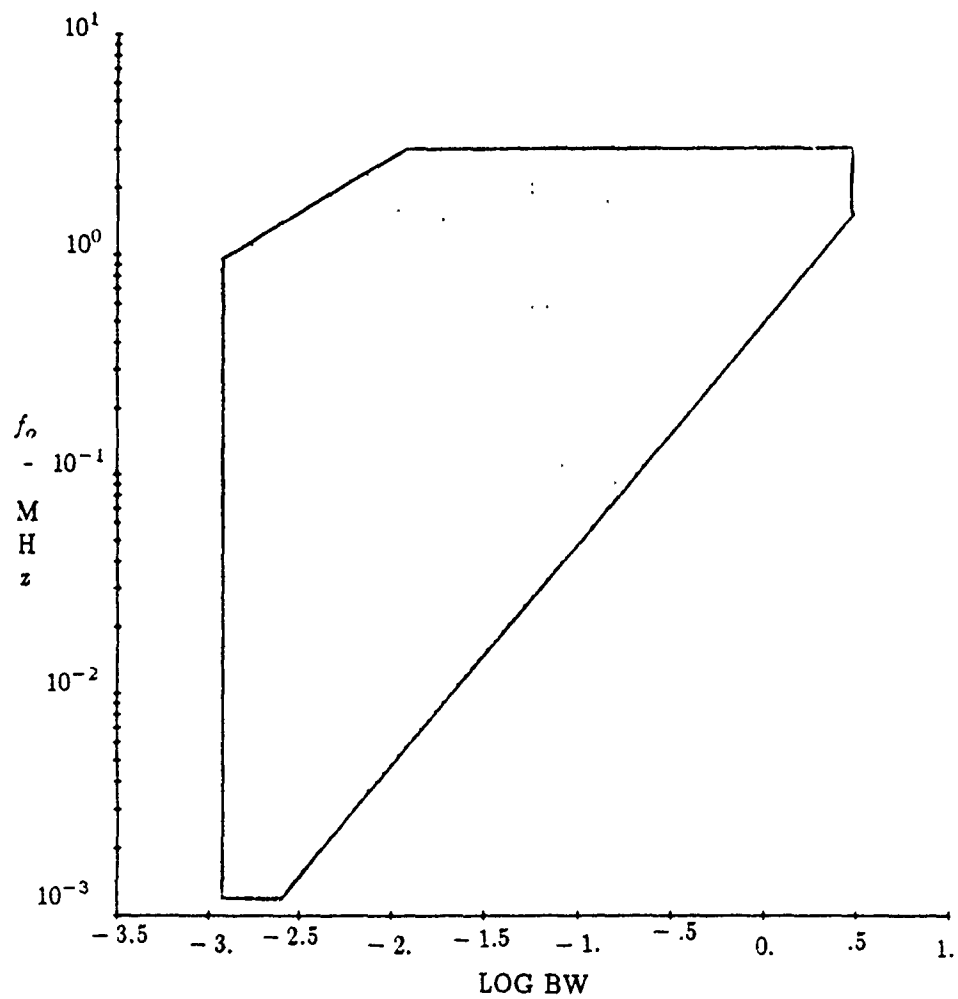


Fig. 2.1-3: Attainable pole frequencies and bandwidths for the biquad of DCASP-2

have been constructed to determine the effect of this limitation. Fig. 2.1-4 shows the range of ω_p and BW_p values for the lowpass, highpass and bandpass transfer functions with the signal amplitude limitation of (2.1-6) imposed. These ranges are slightly less than that depicted in Fig. 2.1-3 where no considerations were made for signal amplitude limitations; however, the ranges of attainable pole frequencies and bandwidths for these filter types still appear to be sufficient.

It can be readily shown that no allpass transfer functions can be implemented which satisfy (2.1-6). Allpass functions may be implemented only at the expense of dynamic range reduction; e.g., if the output voltage is restricted to $2V_{p-p}$, then a number of pole frequencies and bandwidths are possible which will not result in internal node voltages greater than $4V_{p-p}$. Figures 2.1-5(a) and (b) show the range of attainable pole frequencies and pole bandwidths for the allpass function subject to the conditions $\left| \frac{V_1(s)}{V_{out}(s)} \right|_{s=j\omega_p} \leq 2.0$ and $\left| \frac{V_1(s)}{V_{out}(s)} \right|_{s=j\omega_p} \leq 3.0$, respectively.

An analog buffer is included at the output of the biquad in order to give the biquad a low output impedance and the capability to drive the following biquad or other load. The CTA based integrators which comprise the biquad are not suitable for this task, since the CTA characteristically exhibits a high output impedance.

The CTA, PCA, and buffer are discussed further in the following sections.

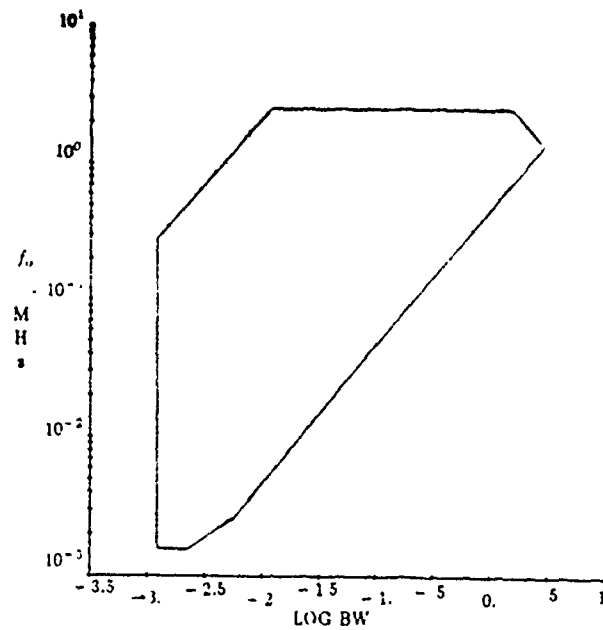
Note that in addition to the analog switches which affect the transfer function of the biquad, Fig. 2.1-2 shows one analog switch at the biquad input (set by B_{exc}) and two at the biquad output (set by B_{casc} and B_{resp}). These allow the biquad input to be connected either to the excitation line (V_{exc}) in the analog bus or to the output of the previous biquad, while the biquad output may be connected to the input (V_{casc}) of the following biquad or to the response line (V_{resp}) in the analog bus.

2.1.2 Controlled Transconductance Amplifier (CTA)

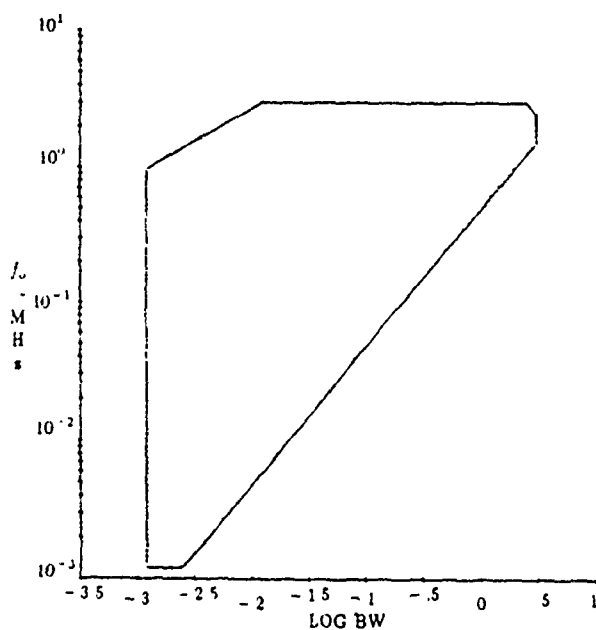
The function of the CTA is to provide a parameter (transconductance, g_m) which can be varied in order to achieve a desired biquad transfer function. As seen in Eq. (2.1-3), the expressions for the biquad's pole and zero frequencies and bandwidths each contain at least one g_m factor. A block diagram of the CTA used in this project is shown in Fig. 2.1-6. It consists of an operational transconductance amplifier (OTA), a digital-to-analog converter (DAC) and a 12-bit latch.

There are two ways in which to vary the g_m of the CTA. One results in coarse g_m adjustment and the other in a fine adjustment.

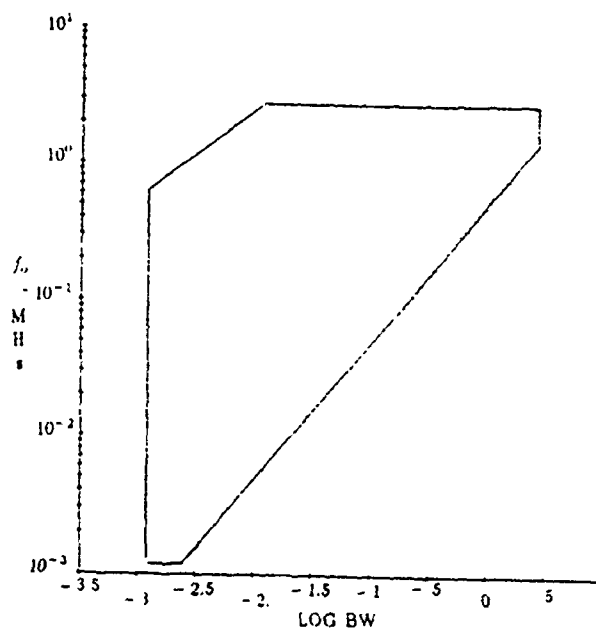
The coarse adjust is achieved by enabling any combination of the six differently sized



(a)

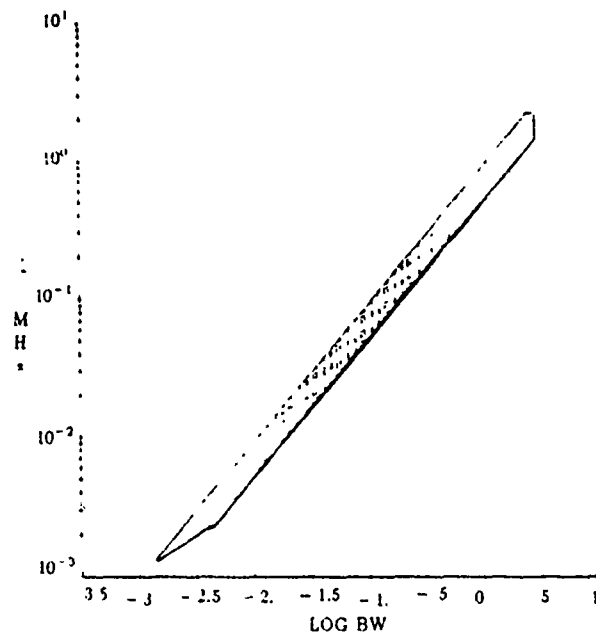


(b)

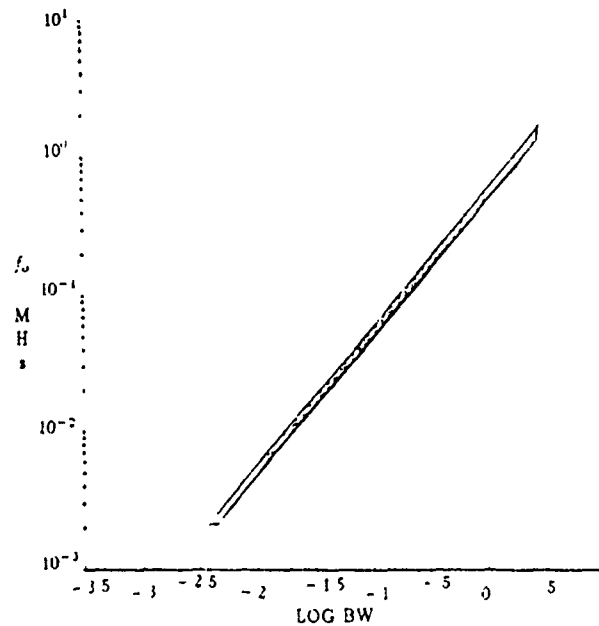


(c)

Fig. 2.1-4: Pole frequencies and bandwidths for the (a) lowpass, (b) highpass, and (c) bandpass configurations of the biquad of DCASP-2, restricted to those values for which $\left| \frac{V_1(s)}{V_{out}(s)} \right|_{s=j\omega_p} \leq 1.0$, where $V_1(s)$ and $V_{out}(s)$ are the internal and the output node voltages, respectively.



(a)



(b)

Fig. 2.1-5: Pole frequencies and bandwidths for the biquad of DCASP-2 in the allpass configuration, restricted to those values for which (a) $\left| \frac{V_1(s)}{V_{OUT}(s)} \right|_{s=j\omega_p} \leq 2.0$ and (b) $\left| \frac{V_1(s)}{V_{OUT}(s)} \right|_{s=j\omega_p} \leq 3.0$, where $V_1(s)$ and $V_{OUT}(s)$ are the internal and the output node voltages, respectively.

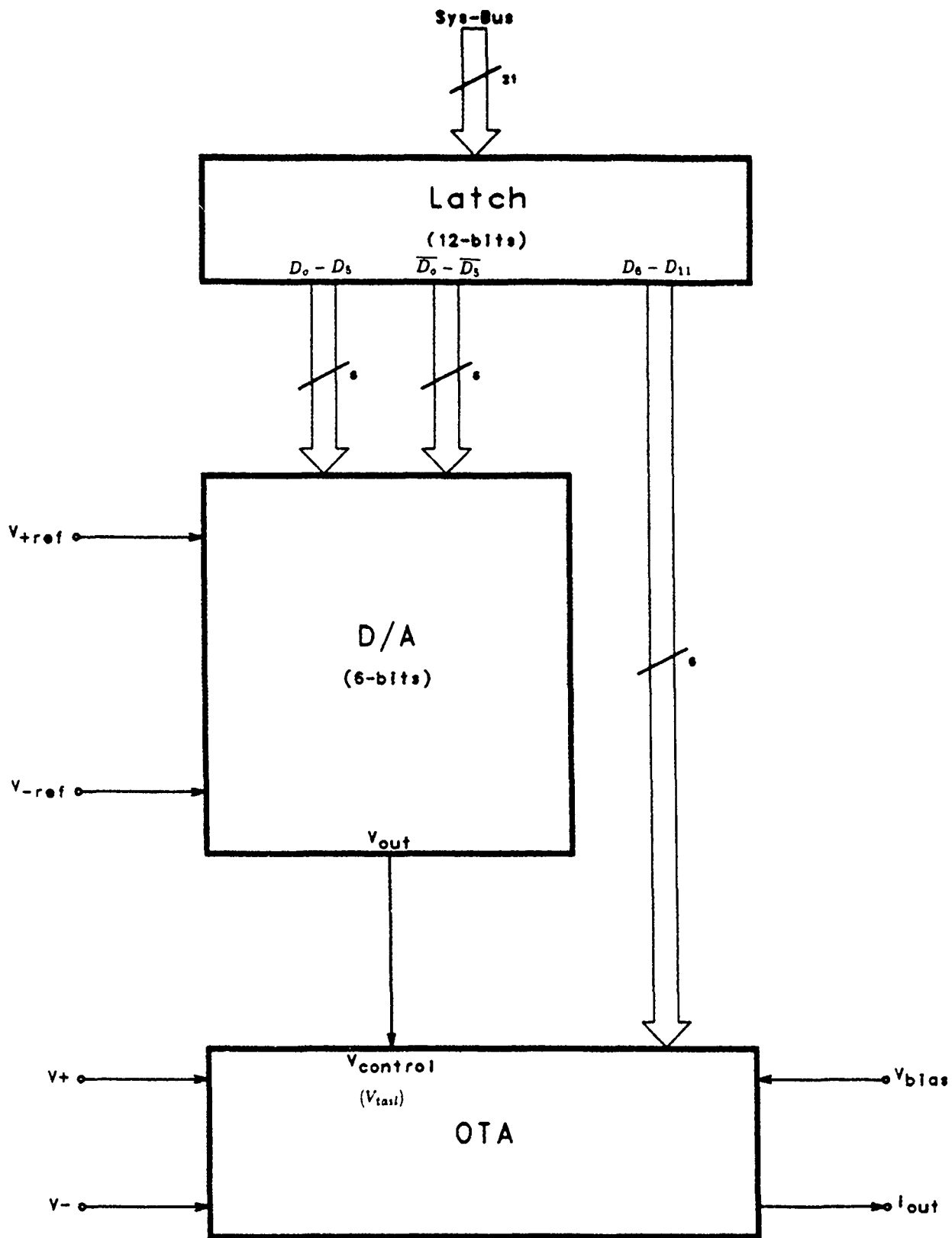


Fig. 2.1-6: CTA Block Diagram

output mirror stages of the OTA. This will result in an effective change in the mirror gain and, hence, a change in the g_m , since

$$g_m = A_M g_{md}, \quad (2.1 - 7)$$

where A_M is the current mirror gain and g_{md} is the transconductance gain of the differential input stage to the OTA. The OTA architecture will be discussed in more detail in the following section.

The second way in which to vary the g_m is to vary the digital input to the DAC. This will result in a change in the DAC output voltage, which is the OTA control voltage, V_{tail} . The V_{tail} adjustment constitutes the fine adjustment capability. The transconductance gain of the differential input stage, g_{md} , is dependent upon V_{tail} ; the relationship between the two may be approximated by the equation of a straight line,

$$g_{md} \cong mV_{tail} + b \quad (2.1 - 8)$$

where m and b are constants determined from a plot of g_{md} vs. V_{tail} . From (2.1-7) and (2.1-8), the overall transconductance gain of the OTA can be expressed as

$$g_m = A_M(mV_{tail} + b). \quad (2.1 - 9)$$

Six bits have been assigned to both the coarse adjustment and the fine adjustment. A 12-bit latch is used to hold this 12-bit control word. For notational purposes, the most significant 6 bits are used to control the output mirror stage and thus correspond to the coarse adjustment feature whereas the least significant bits are used to control V_{tail} which constitutes the fine adjustment. The mapping of these bits to the values of attainable g_m 's is discussed in the following sections.

The basic architecture of the CTA is identical in both DCASP-1 and DCASP-2; i.e., the block diagram of Fig. 2.1-6 applies to each. However, the CTA of DCASP-2 does include several modifications to the latch, the OTA, and the DAC. For one, the CTA latch of DCASP-1 required only 8-bits, as the OTA of DCASP-1 contained only two output stages compared to the six output stages of DCASP-2. Improvements in parameter adjustment range and resolution were obtained with DCASP-2 at the expense of requiring additional control bits and some additional circuit elements. The differences between the OTA and DAC of DCASP-1 and -2 are discussed in the following sections.

2.1.2.1 Operational Transconductance Amplifier (OTA)

The transconductance, g_m , of the OTA is one of the parameters which sets the pole and zero frequencies and bandwidths of the biquad, the other parameter being the capacitance

of the PCA. This is apparent from equation (2.1-3). Both a fine and a coarse adjustment of g_m are provided for in the OTA. The OTA of DCASP-2 contains modifications to the coarse g_m control which permit the biquad to realize a greater range of frequencies and bandwidths than does the biquad of DCASP-1.

The OTA of DCASP-2 is shown in Fig. 2.1-7. Device sizes are listed in Table 2.1-2. The circuit is a slightly modified version of a recently reported approach for designing CMOS OTA's [16]. It employs a linearized input stage consisting of a simple source-coupled pair M_1, M_2 biased dynamically by a compensating current component which is proportional to the square of the differential input voltage. This square-law compensating current (generated by $M_3 - M_6$) is used to counter the inherent quadratic nonlinearities of the source-coupled differential pair itself. By properly scaling the W/L ratios of the source-coupled pair and the cross-coupled devices, the nonlinearities of the input stage can be largely cancelled out over a wide input voltage range.

The control voltage V_{tail} sets the bias currents and determines the transconductance of the input stage. The fine adjustment of g_m is accomplished by the adjustment of this control voltage. This is further discussed in connection with the DAC in the following section. The differential drain currents, I_{D1} and I_{D2} , from the linearized input stage are amplified and subtracted using current mirrors to yield the OTA output current I_o .

The pole frequencies and pole bandwidths attainable with DCASP-1 are shown in Fig. 2.1-8. Note the undesirable gap in the attainable bandwidths for frequencies greater than 900 KHz. Also note that the minimum bandwidth is approximately 21 KHz; a smaller minimum bandwidth is preferable. Both increased g_m adjustment range and resolution are needed.

The OTA design of DCASP-1 permits a coarse control of g_m by a factor of either 1 or 0.1. There exists a gap in the attainable values of g_m , and this causes the undesirable gap in the attainable pole bandwidths noted earlier.

The OTA of DCASP-2 differs from the previous design in that it contains six output stages rather than two. The six output stages allow a coarse adjustment of g_m by a factor from 1 to less than 0.01. Furthermore, these output stages are designed such that there are no "gaps" in the attainable values of g_m in the geometric scale sense.

The W/L ratios of the six output stages were selected to allow g_m to be incremented by geometric factors of 1.618 from the minimum value of g_m to the maximum value of g_m .

For example, assume the gain of the first stage (M28-M33 in Figure 2.1-7) is $(1.618)^{-10}$. If the second stage (M34-M39) is enabled while all others are disabled, the gain is $(1.618)^{-9}$. If the first and second stages are enabled, the gain is $(1.618)^{-10} + (1.618)^{-9} = (1.618)^{-8}$. Table 2.1-3 shows the digital control sequence necessary to obtain 11 uniformly spaced (in the geometrical sense) g_m values with the 6 control bits.

Resolution based upon a geometric (logarithmic) scale rather than a linear scale was

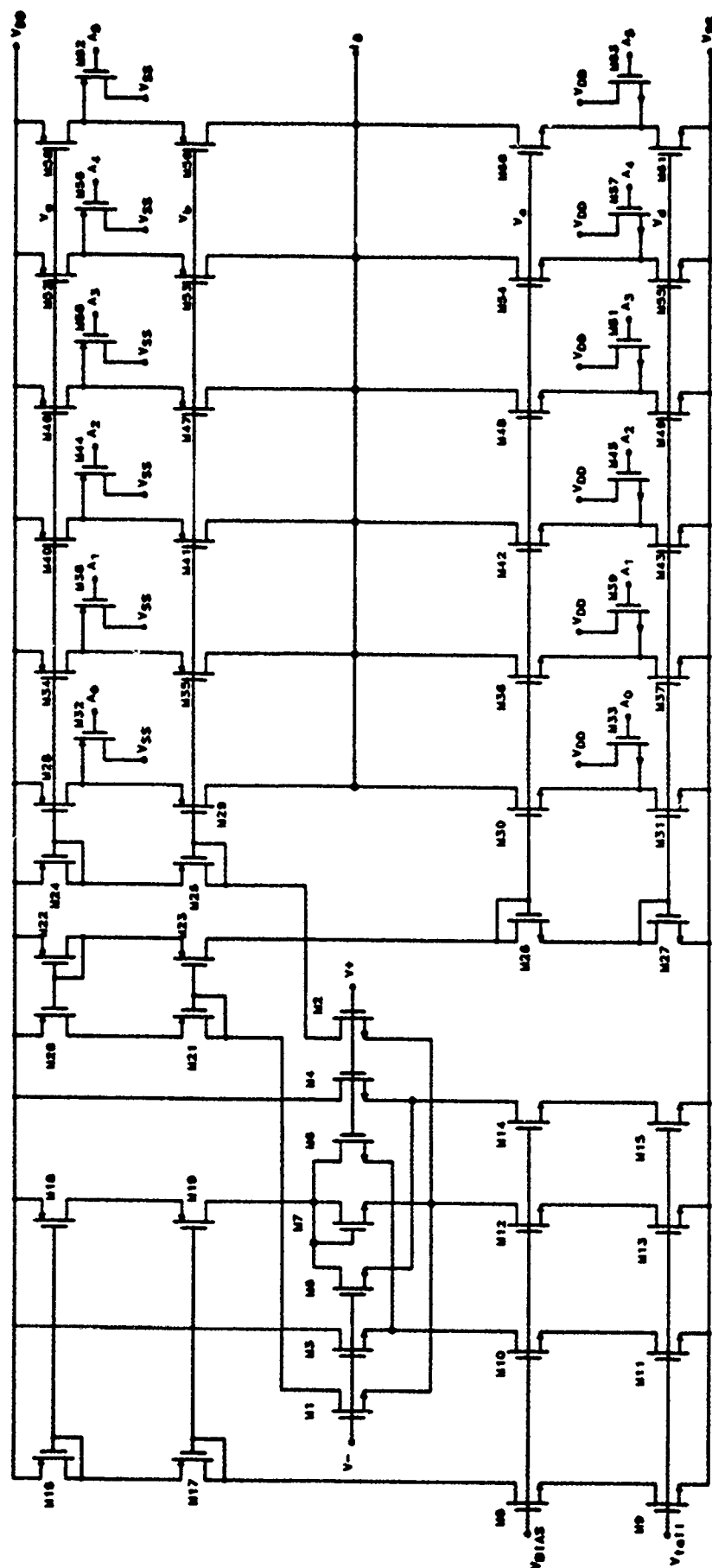


Fig. 2.1-7: OTA with 6-bit coarse control

Table 2.1-2: Device Sizing for OTA Structure of Fig. 2.1-7.

DEVICE	SIZE (microns)	
	W	L
M1-M2	8	5
M3-M4	16	5
M5-M6	8	5
M7	7	5
M8-M9	40	3
M10-M15	80	3
M16-M17	60	3
M18-M21	120	3
M22-M23	60	3
M24-M25	120	3
M26-M27	60	3
M28-M31	5	11
M32-M33	7	3
M34-M37	6	9
M38-M39	7	3
M40-M43	15	9
M44-M45	7	3
M46-M49	21	6
M50-M51	7	3
M52-M55	17	3
M56-M57	7	3
M58-M61	44	3
M62-M63	17	3

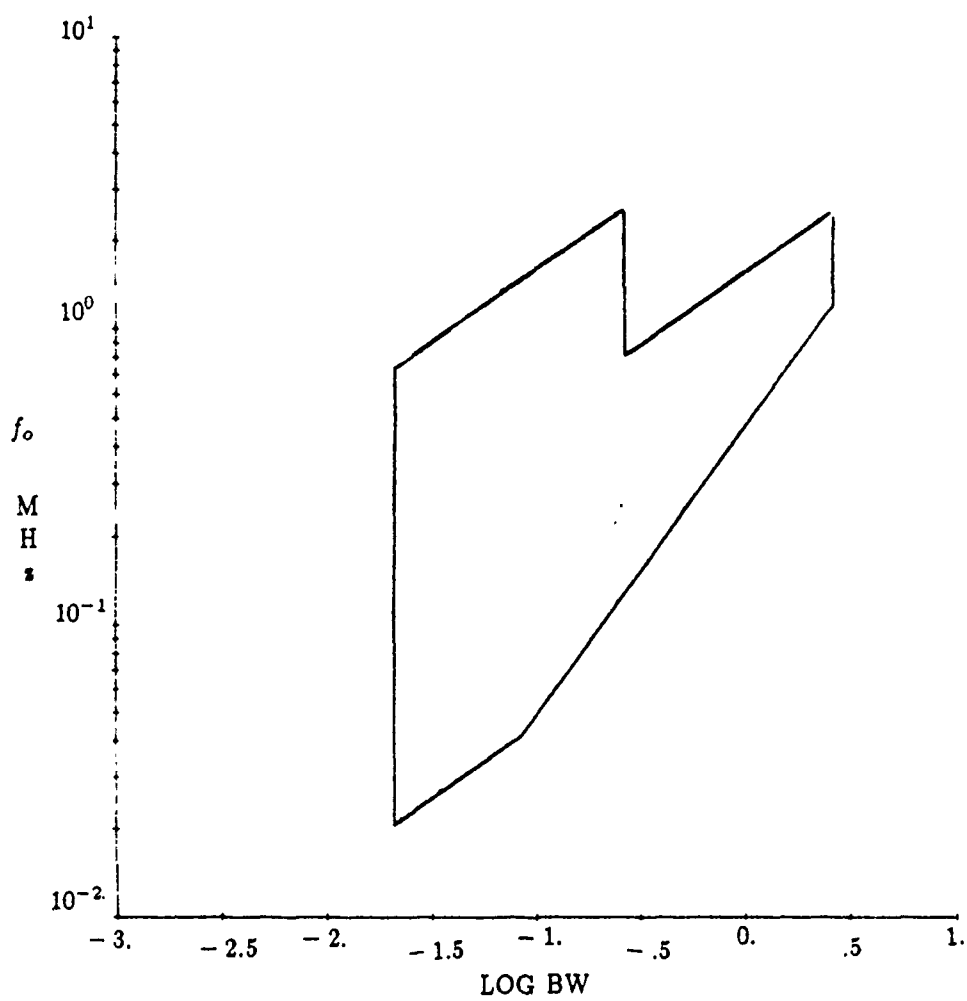


Fig. 2.1-8: Attainable pole frequencies and bandwidths for the biquad of DCASP-1.

Table 2.1-3: Gain of OTA as a function of coarse control digital input assuming gain of first stage is equal to $(1.618)^{-10}$.

A_5	A_4	A_3	A_2	A_1	A_0	Gain
0	0	0	0	0	1	$(1.618)^{-10} = .00813$
0	0	0	0	1	0	$(1.618)^{-9} = .01316$
0	0	0	0	1	1	$(1.618)^{-8} = .0213$
0	0	0	1	0	0	$(1.618)^{-7} = .0344$
0	0	0	1	1	1	$(1.618)^{-6} = .0557$
0	0	1	0	0	0	$(1.618)^{-5} = .0902$
0	0	1	1	1	1	$(1.618)^{-4} = .1459$
0	1	0	0	0	0	$(1.618)^{-3} = .236$
0	1	1	1	1	1	$(1.618)^{-2} = .382$
1	0	0	0	0	0	$(1.618)^{-1} = .618$
1	1	1	1	1	1	$(1.618)^0 = 1.000$

selected because it is thought that this will more realistically meet a larger portion of filtering needs. This is particularly important for structures which are capable of a large ω_p adjustment range. Note that when resolution is defined in the geometric (logarithmic) sense rather than the linear sense, a fixed % of resonant frequency resolution can be maintained throughout the domain of adjustment. With a linear rather than geometric scale, the effective resolution (% of resonant frequency) for wide ω_p adjustment ranges is much worse at low frequencies than at high frequencies.

The factor 1.618 is optimal in that it is a solution of the equation

$$X + X^2 = X^3 \quad (2.1 - 10)$$

Thus, gains such as $(1.618)^{-8}$ may be obtained by enabling the $(1.618)^{-10}$ and $(1.618)^{-9}$ stages rather than requiring a separate stage.

It can be noted from Table 2.1-3 that the 6 digital control bits allow for the uniform spacing in the geometric sense of 11 achievable gains. This is certainly much better than the 6 that would be achievable if each bit could select only one gain. Note also that this table lists only 11 of the possible $2^6 = 64$ codes for $A_0 - A_5$. The digital control words missing in Table 2.1-3 can also be used to provide 53 additional mirror gains distributed between the 11 listed in the table. Although this can provide significant improvements in resolution in some ranges, these points are not uniformly spaced and are bunched towards the unity gain end of the mirror gain range. In particular, none of these 53 points yield a gain between $(1.618)^{-9}$ and $(1.618)^{-10}$; hence, no improvement in the overall resolution is achieved by adding these points.

The fine control of g_m , provided by the voltage V_{tail} must allow the gain to vary by a factor greater than 1.618 to insure that there are no undesirable gaps in the obtainable values of g_m . As discussed in the following section, this factor was chosen to be approximately 1.87. It is believed that this will allow for compensation of mismatches in the mirror devices which could cause the coarse g_m adjustment to deviate from the factor of 1.618.

Recall from equation (2.1-9) the relationship between g_m and V_{tail} ,

$$g_m = A_M(mV_{tail} + b) \quad (2.1 - 11)$$

The mirror gain factor A_M is now seen to be a power of 1.618 (assuming only the 11 states listed in Table 2.1-3 are considered). Also, the constants m and b determined from an experimental plot of g_m versus V_{tail} are $61.8\mu S/V$ and $257.9\mu S$, respectively. Including these factors, the g_m of the CTA may be expressed as

$$g_m = (1.618)^{-i}(61.8V_{tail} + 257.9) \quad i = 0, 1, \dots, 10, \quad (2.1 - 12)$$

where V_{tail} is in volts and g_m is in μS .

Recall Fig. 2.1-3 shows the range of pole bandwidths and pole frequencies attainable with the biquad DCASP-2. Comparing Fig. 2.1-3 to Fig. 2.1-8, it is clear that in addition to the absence of gaps in the bandwidths, much smaller bandwidths can be attained in DCASP-2. The biquad of DCASP-2 permits a minimum bandwidth of 1.2 KHz, as opposed to the minimum bandwidth of 21 KHz for the biquad of DCASP-1.

The greatly expanded g_m adjustment range provided by the OTA design of DCASP-2 may eliminate the need for a programmable capacitor array, (PCA), in future DCASP implementations. Note from equation (2.1-3) that the pole and zero frequencies and bandwidths are determined by ratios of the form g_m/C . In DCASP-2, a coarse adjustment of this ratio is obtained by the coarse adjustment of g_m or the adjustment of the capacitance of the PCA. Considerable simplification of the circuitry may result if a fixed capacitor could replace the PCA; i.e., if the coarse g_m adjustment alone provided sufficient coarse adjustment of the pole and zero frequencies and bandwidths.

The method used to disable the output stages is also noteworthy. When a stage is disabled, the corresponding signal current is channeled through two auxiliary transistors rather than allowed to pass through to the output node. For example, when the first stage is disabled (by setting A_0 to logical 0), the signal current is channeled through M32 and M33 rather than allowed to pass through M29 and M30 (as it would normally do for $A_0 = 1$).

The point to be noted here is that the output stage always draws a dc current, and hence dissipates power, regardless of whether it is enabled or disabled. This results in constant power dissipation for all mirror gains or, correspondingly, a waste of power for all but the case where every output stage is enabled. Table 2.1-4 lists the dc current drawn by each stage when that stage is disabled; these numbers were obtained from SPICE analysis.

If desired, these losses may be reduced by using a structure such as the one shown in Fig. 2.1-9. Here, the stage is disabled by controlling gate voltages. When the stage is disabled ($A=0$), the gate voltages applied to M5 and M8 are V_{DD} and V_{SS} , respectively; thus, these two transistors are off and the stage draws no current. This structure may, however, exhibit undesirable characteristics due to such things as increased gate capacitance (due to the presence of M3 and M4) and nonlinearities associated with transmission gates M1 and M2.

2.1.2.2 Digital-to-Analog Converter (DAC) and Fine g_m Adjustment

The DAC generates the OTA control voltage V_{tail} which is used in the fine adjustment of g_m (see Fig. 2.1-7). The DAC of DCASP-2 was designed such that the resolution in g_m always remains better than 1%. The resolution here is defined as

$$\text{resolution} = \frac{\Delta g_m}{g_m} \quad (2.1 - 13)$$

Table 2.1-4: DC current drawn by disabled OTA output stages.
 $V_{DD} = +5V$; $V_{SS} = -5V$, $V_{BIAS} = -2.5V$, $V_{tail} = -3.4V$

Stage	Transistors	Current (μA)
1	M28-M33	.72
2	M34-M39	1.26
3	M40-M45	3.4
4	M46-M51	10.3
5	M52-M57	36.0
6	M58-M63	95.2

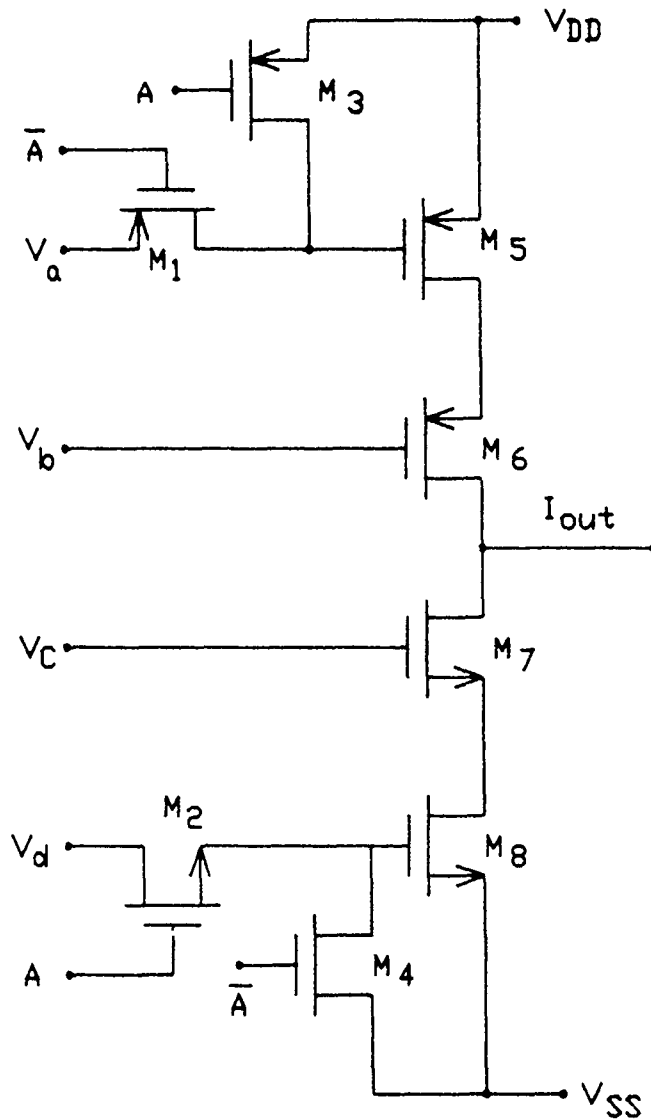


Fig. 2.1-9: Alternate OTA output stage structure which eliminates DC current when stage is disabled. (Node voltages V_a , V_b , V_c , V_d correspond to those in existing OTA structure of Fig. 2.1-7.)

where Δg_m is the change in g_m produced by one LSB transition of the DAC. The DAC of DCASP-2 also allows greater overlap of the coarse g_m ranges than would the DAC of DCASP-1. This is further discussed below. (Note: the g_m resolution is ultimately determined by the DAC rather than the output mirror stages of the OTA. Unless otherwise stated, it will be assumed throughout this section that the mirror gain, A_M in equation 2.1-9, is constant and equal to 1.)

Consider first the use of a linear DAC as in DCASP-1. Since g_m is proportional to V_{tail} (see equation 2.1-9), the Δg_m is a constant. In order to maintain a resolution of $\leq 1\%$ for the largest possible range of adjustment of g_m , it follows from (2.1-13) that the value of Δg_m must be

$$\Delta g_m = .01 g_{m_{MIN}}. \quad (2.1-14)$$

For the i th state, the value of g_m is then

$$g_m = g_{m_{MIN}} + i \Delta g_m \quad i = 0, 1, \dots, 2^N - 1, \quad (2.1-15)$$

where N is the number of bits in the DAC. For a 6-bit linear DAC, the maximum value of g_m is

$$g_{m_{MAX}} = g_{m_{MIN}} + (2^6 - 1) \Delta g_m = 1.63 g_{m_{MIN}} \quad (2.1-16)$$

Recall that the output stages of the OTA allow for a coarse adjustment of g_m by a factor of 1.618. The fine adjustment of g_m by a factor of up to 1.63, suggested by (2.1-16), is deemed to provide insufficient overlap of the coarse ranges.

Consider now the use of a DAC which allows Δg_m to be larger for larger values of g_m in order that the ratio $\frac{\Delta g_m}{g_m}$ remain constant. For a resolution of 1%, it follows from (2.1-13) that

$$\Delta g_{m_i} = .01 g_{m_i} \quad (2.1-17)$$

and

$$g_{m_{i+1}} = 1.01 g_{m_i} \quad (2.1-18)$$

The value of g_{m_i} is related to the minimum value by

$$g_{m_i} = (1.01)^i g_{m_{MIN}} \quad i = 0, 1, \dots, 2^N - 1 \quad (2.1-19)$$

For a 6-bit DAC, the maximum value of g_m is

$$g_{m_{MAX}} = (1.01)^{63} g_{m_{MIN}} = 1.87 g_{m_{MIN}} \quad (2.1-20)$$

Thus, this constant g_m -resolution DAC allows a fine adjustment of g_m by a factor of up to 1.87; this is the maximum factor that can be attained using a 6-bit DAC and maintaining a resolution of at least 1%.

The DAC implemented in DCASP-2 is such that successive voltage increments are related by a constant factor, i.e.,

$$\Delta V_{i+1} = C \Delta V_i \quad i = 0, 1, \dots, 61, \quad (2.1-21)$$

where V_i is the output voltage of the DAC corresponding to the 6-bit digital input expressed in decimal form as i , C is a positive constant and

$$\Delta V_i = V_{i+1} - V_i \quad i = 0, 1, \dots, 62 \quad (2.1 - 22)$$

It follows from (2.1-21) and (2.1-22) that

$$\Delta V_i = C^i \Delta V_0 \quad i = 0, 1, \dots, 62 \quad (2.1 - 23)$$

This has been termed a logarithmic DAC since, for $C \neq 1$, the incremental voltage changes are equally spaced on a logarithmic scale. (Note that a linear DAC results when $C=1$). The output voltage for the i^{th} state may be written

$$V_i = V_0 + \Delta V_0 \sum_{k=0}^{i-1} C^k \quad i = 1, 2, \dots, 63 \quad (2.1 - 24)$$

or, for $C \neq 1$,

$$V_i = V_0 + \frac{\Delta V_0(1 - C^i)}{1 - C} \quad i = 1, \dots, 63 \quad (2.1 - 25)$$

An expression for the resolution in g_m as a function of the constant C will now be determined for the case of the logarithmic DAC. In equation (2.1-9), the g_m of the OTA was expressed as a linear function of the DAC voltage. In terms of the i^{th} state of the DAC,

$$g_{m_i} = (mV_i + b)A_M, \quad (2.1 - 26)$$

where m and b are the slope and intercept of the g_{m_d} vs. V_i curve and the output voltage of the DAC, V_i , is assumed to be the tail voltage, V_{tail} , in the OTA structure of Fig. 2.1-7. (Note: the mirror gain, A_M , is included in equation (2.1-26) to demonstrate that it need not be equal to 1, but may be any constant.) The incremental change in g_m due to one LSB transition of the DAC is then

$$\Delta g_{m_i} = g_{m_{i+1}} - g_{m_i} = A_M m \Delta V_i \quad (2.1 - 27)$$

From (2.1-23), it follows that

$$\Delta g_{m_i} = C^i A_M m \Delta V_0 = C^i \Delta g_{m_0} \quad (2.1 - 28)$$

and

$$g_{m_i} = \Delta g_{m_0} \frac{(1 - C^i)}{1 - C} + g_{m_0} \quad (2.1 - 29)$$

Combining (2.1-28) and (2.1-29), the resolution in g_m is

$$\frac{\Delta g_{m_i}}{g_{m_i}} = \frac{C^i \Delta g_{m_0}}{\Delta g_{m_0} \frac{(1 - C^i)}{1 - C} + g_{m_0}} = \frac{C^i \frac{\Delta g_{m_0}}{g_{m_0}}}{\frac{\Delta g_{m_0}}{g_{m_0}} \frac{(1 - C^i)}{(1 - C)} + 1} \quad (2.1 - 30)$$

This last equation relates the g_m resolution for the i^{th} state in terms of the constant C and the resolution of the $zero^{th}$ state. Of special interest is the case where the DAC is designed such that

$$\frac{\Delta g_{m_o}}{g_{m_o}} = C - 1 \quad (2.1 - 31)$$

For this case, (2.1-30) simplifies to

$$\frac{\Delta g_{m_i}}{g_{m_i}} = \frac{\Delta g_{m_o}}{g_{m_o}}, \quad (2.1 - 32)$$

and the resolution is seen to be constant and equal to $C - 1$. This situation, then, describes the constant g_m resolution DAC discussed earlier.

A schematic of the 6-bit parallel switching array DAC used in DCASP-2 is shown in Fig. 2.1-10. This structure is based upon a $(2^6 - 1)$ 63-element resistive polysilicon string which is tapped by a pyramidal switching array. The array of switches provides a single conductive path to a specific tap on the resistor string depending on the digital input to the DAC. This approach does not require any decoding logic and thus has a much smaller active area ($0.20mm^2$) than the classical approach used in DCASP-1 ($1.22mm^2$).

The use of a resistor string is suitable for realizing the linear DAC of DCASP-1 or the logarithmic DAC of DCASP-2. For either case, the voltage, V_i , between the i and $i+1$ resistors may be written as

$$V_i = V_o + \frac{\sum_{j=1}^i R_j}{\sum_{k=1}^{63} R_k} (V_{63} - V_o) \quad i = 1, 2, \dots, 63 \quad (2.1 - 33)$$

where V_o and V_{63} are the voltages present at the two ends of the resistor string. (Note: The voltages V_{ref+} and V_{ref-} indicated in Fig. 2.1-10 are the voltages which are actually applied to the input pins on the chip. However, due to parasitic resistances R_{p1} and R_{p2} , the voltages V_o and V_{63} differ slightly from the applied voltages V_{ref+} and V_{ref-} .)

A linear DAC results when the value of all resistors is the same. Under this condition, (2.1-33) becomes

$$V_i = \frac{i}{63} (V_{63} - V_o) + V_o \quad (2.1 - 34)$$

A logarithmic DAC results when the value of adjacent resistors differs by a constant factor other than unity, i.e., when

$$R_i = C R_{i-1} \quad i = 2, \dots, 63 \quad (2.1 - 35)$$

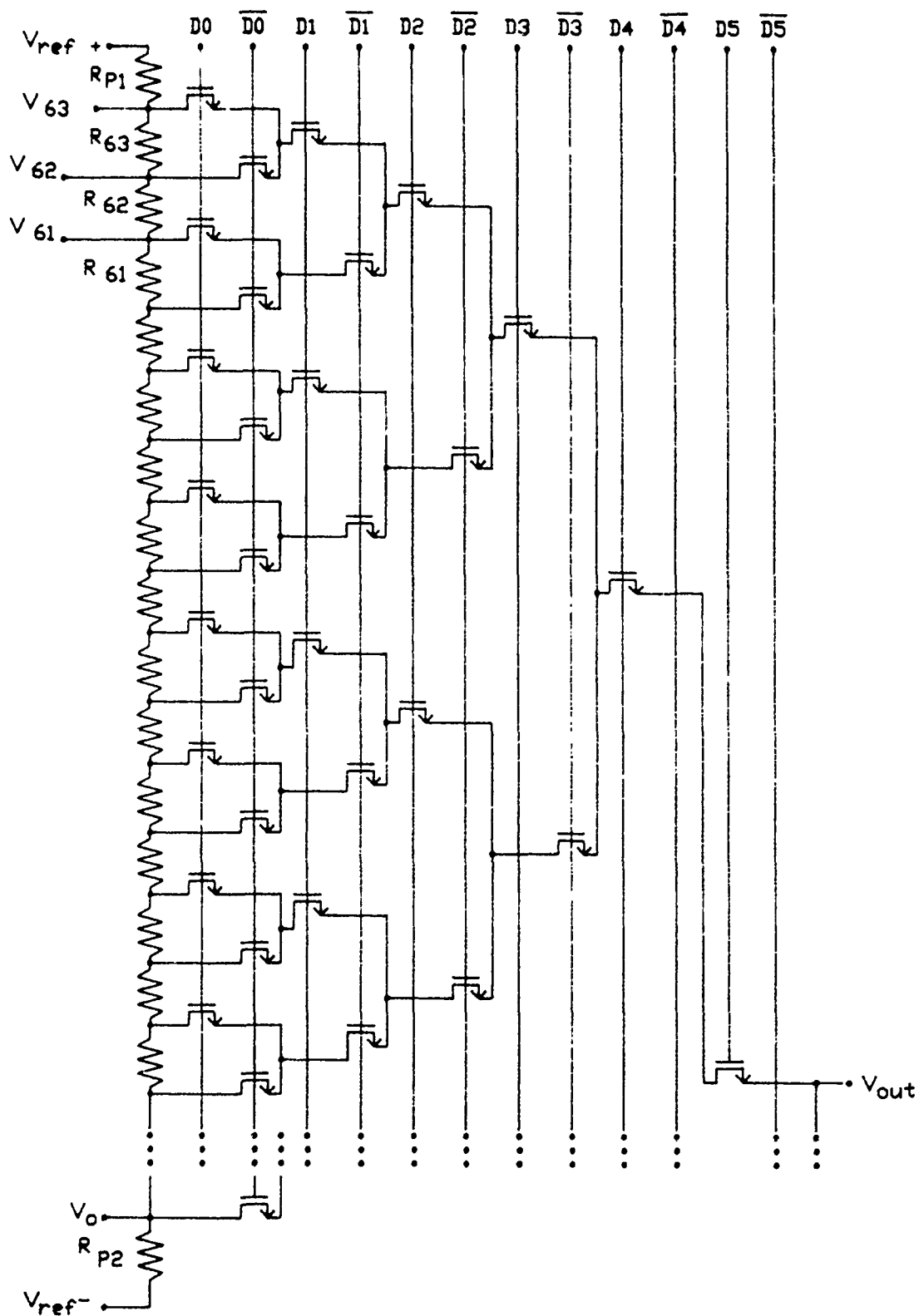


Fig. 2.1-10: Parallel Switch Array DAC

or

$$R_i = C^{i-1} R_1 \quad i = 1, \dots, 63 \quad (2.1 - 36)$$

for $C \neq 1$. Under these conditions, (2.1-33) becomes

$$V_i = V_o + \frac{\sum_{j=1}^i C^{j-1}}{\sum_{k=1}^{63} C^{k-1}} (V_{63} - V_o) \quad , \quad (2.1 - 37)$$

and equations (2.1-21) through (2.1-32) are satisfied. Note that, from (2.1-37),

$$\Delta V_o = V_i - V_o = \frac{1}{\sum_{k=1}^{63} C^{k-1}} (V_{63} - V_o) = \frac{1 - C}{1 - C^{63}} (V_{63} - V_o). \quad (2.1 - 38)$$

Thus, ΔV_o , and hence Δg_{m_o} , can be made as small as desired by proper choice of the constant C and applied voltages V_{63} and V_o . A more exact expression for the voltage of the i^{th} state follows from (2.1-25) and (2.1-38),

$$V_i = V_o + \frac{1 - C^i}{1 - C^{63}} (V_{63} - V_o) \quad (2.1 - 39)$$

It should be obvious that the maximum g_m adjustment range, resolution and digital control word length are related. This relationship is, from (2.1-29) and (2.1-31).

$$g_{m_{MAX}} - g_{m_{MIN}} = (1 + \eta)^{2^N - 1} \quad , \quad (2.1 - 40)$$

where η is the resolution and N is the length of the digital control word.

To summarize, the DAC of DCASP-2 was designed to maintain a g_m resolution of $\leq 1\%$ while permitting a fine adjustment of g_m over a wider range than possible with a linear DAC. Furthermore, the logarithmic DAC described above can be used to maintain a fixed g_m resolution by choosing the constant C in (2.1-35) to satisfy (2.1-31). For the case of a fixed 1% g_m resolution, this would result in a fine adjustment of g_m by a factor of 1.87 for a 6-bit logarithmic DAC, as opposed to a factor of 1.63 for the case of a linear 6-bit DAC which maintains a g_m resolution of $\leq 1\%$. As the number of bits increases, the difference between the g_m adjustment range attainable with a logarithmic DAC and that attainable with a linear DAC for fixed resolution also increases.

Practical considerations make it difficult to exactly satisfy the constraint of (2.1-35) since the fabrication process used in DCASP-2 allows length variations only by integral numbers of microns. For example, assuming $C = 1.01$ and assuming that the resistors

are to be single lengths of polysilicon (as opposed to having corners), R_1 would have to be $100\mu m$ long in order that R_2 could be made $101\mu m$ long and hence satisfy (2.1-35). The 63 element resistor string, assuming the width of the string remained constant, would require a length of $8,717\mu m$.

Rather than using such single length polysilicon resistors, an alternate approach is to include corners in the resistor, achieving the desired resistance variation by varying the dimensions of the resulting polysilicon segments. This is shown in Fig. 2.1-11, from which the number of squares of polysilicon in the resistor can be approximated by the equation

$$\#squares \simeq \frac{x}{4} + \frac{x}{9-y} + \frac{y}{z} + 4(.55) \quad (2.1-41)$$

The factor of .55 in (2.1-41) is an estimate for the equivalent number of squares represented by a corner. Table 2.1-5 lists the dimensions of the 63 resistors used in the DAC of DCASP-2.

Also listed in Table 2.1-5 are the ratios of adjacent resistors in the string. Recall from (2.1-35) that, ideally, these ratios should all be equal to the constant $C = 1.01$. This design goal was outweighed by practical considerations of device size and the inaccuracies of equation (2.1-41) (i.e., the factor of .55 squares as an estimate for the corners is not exact). Since the adjacent resistor ratios are not a constant 1.01, the g_m resolution in DCASP-2 is not exactly a constant 1%. However, the reference voltages applied to the resistor string may still be selected such that the g_m resolution is always $\leq 1\%$. While this does not yield the maximum fine adjustment of g_m by a factor of 1.87, it is still an improvement over the linear DAC; i.e., the range of the fine adjustment of g_m is increased in DCASP-2 by using varying-sized resistors, as opposed to using identically-sized resistors as in DCASP-1. For the resistor values listed in Table 2.1-5, it is estimated that the DAC of DCASP-2 will allow a fine adjustment of g_m by a factor of 1.83 while maintaining a g_m resolution of $\leq 1\%$.

2.1.3 Programmable Capacitor Array

The programmable capacitor array was designed to provide a coarse control of the poles and zeros for the biquad of DCASP-1. As stated earlier, with the modifications in the output stage of the OTA of DCASP-2, the capacitor array may be dispensable, with a fixed capacitor taking its place. If this were done, the coarse control of the poles and zeros would be provided instead by the coarse control of the g_m 's. The capacitor array was included in DCASP-2, allowing both methods of coarse control to be examined.

The array of DCASP-2 differs from that of DCASP-1 in that the effect of parasitic capacitances is better accounted for. This is discussed below. Also presented are two alternate implementations of capacitor arrays which may find application in future designs.

The pole and zero frequencies (and bandwidths) of the biquad are determined by

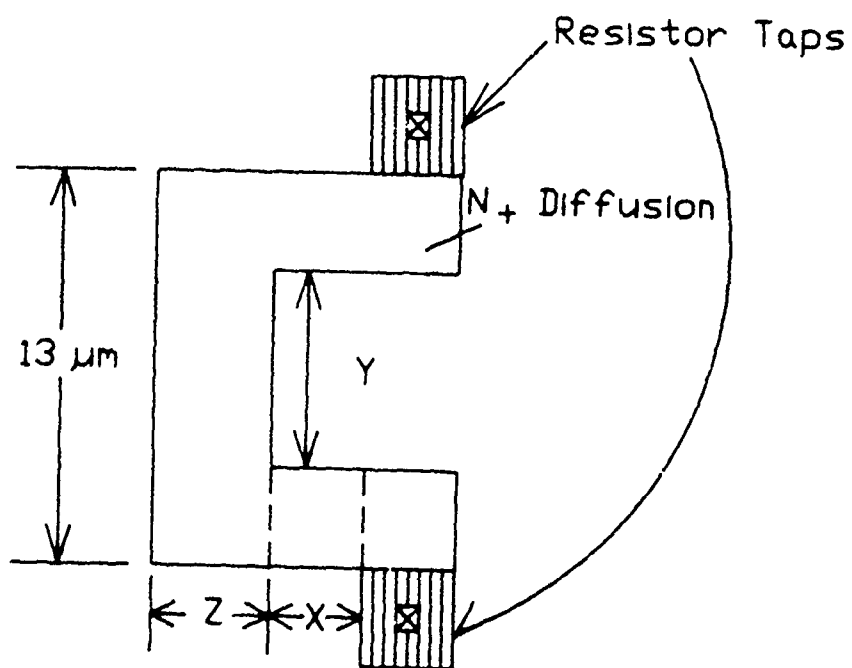


Fig. 2.1-11: Structure used to implement resistors of DAC of LCASP-2.

Table 2.1-5: Resistor Values Used in DAC Resistor String of DCASP-2. X, Y, Z refer to the dimensions in Fig. 5.12-6.

N	X (μm)	Y (μm)	Z (μm)	# Squares	R_N (Ω)	$\frac{R_N}{R_N - 1}$
1	7	4	9	5.794	231.8	-
2	7	4	8	5.850	234.0	1.010
3	6	4	4	5.900	236.0	1.009
4	5	5	4	5.950	238.0	1.008
5	8	4	19	6.010	240.4	1.010
6	7	5	14	6.057	242.3	1.008
7	8	4	13	6.108	244.3	1.008
8	8	4	11	6.164	246.6	1.009
9	8	4	10	6.200	248.0	1.006
10	7	5	9	6.255	250.2	1.009
11	7	5	8	6.325	253.0	1.011
12	8	4	7	6.371	254.8	1.007
13	8	5	21	6.438	257.5	1.011
14	8	5	17	6.494	259.8	1.009
15	8	5	14	6.557	262.3	1.010
16	8	4	5	6.600	264.0	1.007
17	8	5	11	6.655	266.2	1.008
18	7	5	5	6.700	268.0	1.007
19	8	5	9	6.755	270.2	1.008
20	8	5	8	6.825	273.0	1.010
21	10	4	20	6.900	276.0	1.011
22	10	4	16	6.950	278.0	1.007
23	9	5	16	7.012	280.5	1.009
24	9	5	13	7.085	283.4	1.010
25	10	4	9	7.144	285.8	1.008
26	10	4	8	7.200	288.0	1.008
27	9	5	9	7.255	290.2	1.008
28	9	5	8	7.325	293.0	1.010
29	11	4	17	7.385	295.4	1.008
30	10	5	20	7.450	298.0	1.009

N	X (μm)	Y (μm)	Z (μm)	# Squares	R_N (Ω)	$\frac{R_N}{R_N - 1}$
31	11	4	11	7.514	300.6	1.009
32	10	5	13	7.585	303.4	1.009
33	11	4	8	7.650	306.0	1.009
34	11	4	7	7.721	308.8	1.009
35	10	5	9	7.755	310.2	1.004
36	12	4	16	7.850	314.0	1.012
37	10	5	7	7.914	316.6	1.008
38	11	5	17	7.994	319.8	1.010
39	11	5	14	8.057	322.3	1.008
40	11	5	12	8.117	324.7	1.007
41	10	5	5	8.200	328.0	1.010
42	11	5	9	8.255	330.2	1.007
43	13	4	14	8.336	333.4	1.010
44	13	4	11	8.414	336.5	1.009
45	12	5	17	8.494	339.8	1.010
46	12	5	14	8.557	342.3	1.007
47	13	4	7	8.621	344.8	1.007
48	13	4	6	8.716	348.6	1.011
49	14	4	14	8.786	351.4	1.008
50	14	4	11	8.864	354.6	1.009
51	14	4	9	8.944	357.8	1.009
52	13	5	16	9.012	360.5	1.008
53	13	5	13	9.085	363.4	1.008
54	13	5	11	9.154	366.2	1.008
55	13	5	9	9.255	370.2	1.011
56	13	5	8	9.325	373.0	1.008
57	13	5	7	9.413	376.5	1.009
58	14	4	4	9.500	380.0	1.009
59	14	5	13	9.585	383.4	1.009
60	14	5	11	9.654	386.2	1.007
61	15	4	5	9.750	390.0	1.010
62	14	5	8	9.825	393.0	1.008
63	14	5	7	9.914	396.6	1.009

ratios of the form $\frac{C_i}{C_0}$. DCASP-1 allowed a fine control of g_m , and thus a fine control of the frequency, by a factor of 20%. To insure that there are no gaps in the attainable frequencies, the coarse control of C provided by the capacitor array must be by a factor less than 20%. A factor of 13% was chosen, resulting in capacitor values of

$$C_i = C_0(1.13)^i, \quad i = 0, 1, \dots, N-1, \quad (2.1-42)$$

where C_0 is the minimum capacitance and N is the number of capacitors in the array.

In order to reduce the silicon area required by the array, only the incremental changes in capacitance were realized. For example, the value of the second capacitor in the array is $0.13C_0$; the desired capacitance is then achieved by switching this capacitor in parallel with the capacitor C_0 , giving a total of $1.13C_0$. Higher values of capacitance are achieved by switching additional capacitors one by one in parallel. The value of each capacitor in the array is given by

$$C_i = 0.13C_{i-1}, \quad i = 1, \dots, N-1 \quad (2.1-43)$$

and the total capacitance in the M^{th} state is

$$C_M = C_0 + \sum_{i=1}^M C_i, \quad M = 0, 1, \dots, N-1 \quad (2.1-44)$$

A value of $C_0 = 2.39 \text{ pF}$ was chosen in order to give an upper frequency limit of approximately 2MHz at the maximum value of $g_m (\cong 43 \mu\text{S})$. A value of $N=20$ was chosen in order to allow a tuning range of one decade ($f_{\text{max}} = (1.13)^{20} f_{\text{min}} \cong 10 f_{\text{min}}$).

A block diagram of the programmable capacitor array is shown in Fig. 2.1-12. The array is programmed by a 5-bit digital word which is provided by the system bus, stored in a 5-bit latch, and decoded by the cap-predecode and cap-decode logic. The resulting 38 control lines (19 switch control signals and their complements) drive the 19 analog switches in a manner such that for the M^{th} state the first M switches are closed while the remaining switches are open. Note that C_0 is always connected.

In the capacitor array of DCASP-1, the effect of parasitics was not accounted for. There are three parasitic capacitances of concern; these are indicated in Fig. 2.1-13. All three of these are diffusion capacitances; they are the capacitances which result from the reverse biasing of the p-n junction formed by the diffused region and the bulk. One such parasitic capacitance is present at the output of each OTA. A second parasitic appears at the input (the OTA side) of each analog switch. The third is the parasitic capacitance at the output (the capacitor side) of each analog switch. This last is of concern only when a switch is closed, while the other two parasitics are always present.

Approximate values of these parasitic capacitances have been calculated and are listed in Table 2.1-6. All of these parasitics may be considered as connected in parallel with the capacitors of the array. Because these were not accounted for in the array of DCASP-1, the

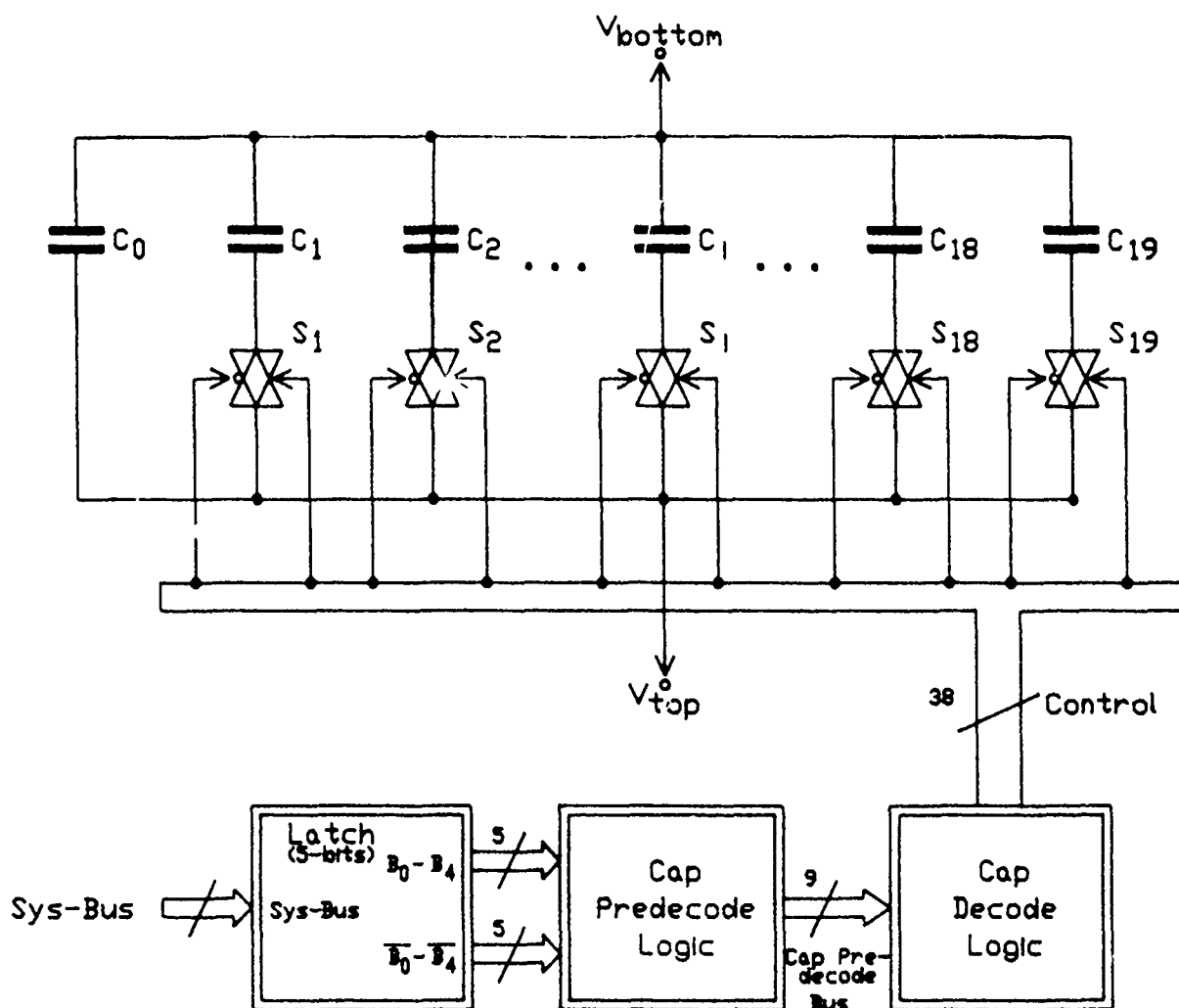


Fig. 2.1-12: Capacitor Array Block Diagram

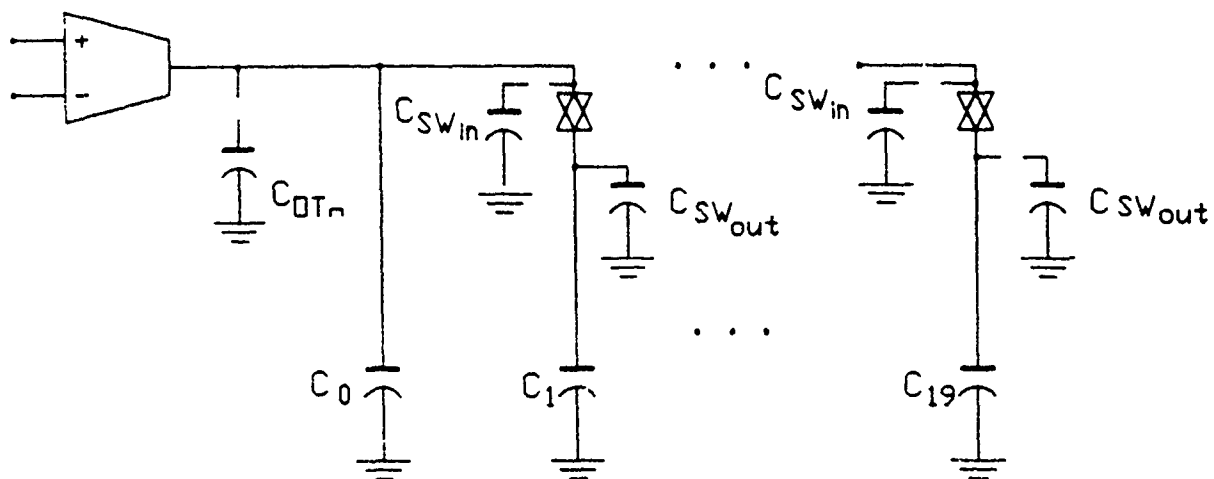


Fig. 2.1-13: Parasitic Capacitances Associated with Programmable Capacitor Array

Table 2.1-6: Estimates of parasitic capacitances affecting programmable capacitor array

Description	p-Type Diffusion Capacitance (fF)	n-Type Diffusion Capacitance (fF)	Total Diffusion Capacitance fF
OTA Output	186.4	216.0	402.4
Analog Switch Input	25.69	21.06	46.75
Analog Switch Output	25.69	21.06	46.75

maximum attainable frequency was lower than anticipated, while the minimum attainable bandwidth was higher.

The parasitics were accounted for in DCASP-2 by subtracting the appropriate value from the desired value of capacitance. The parasitic capacitance of 1.909pF due to "2.5" OTA's and 19 analog switch inputs is always present; subtracting from the desired ever-present 2.39pF leaves a value of 0.48pF to be implemented as C_o . (Note: The biquad contains two capacitor arrays, one of which is connected to two OTA outputs, while the other is connected to three OTA outputs. In DCASP-2, rather than making two different arrays, one based on two OTA outputs and one based on three OTA outputs, both arrays were made identical, and the parasitic capacitance of 1.909pF was based on an assumed load equivalent to that of "2.5 OTA" outputs. It follows that the actual range of capacitance will differ from the designed range by approximately 0.5 times the parasitic capacitance of one OTA output; this is deemed acceptable). For capacitors $C_1 - C_{19}$, only the parasitic capacitance of 46.8fF due to one analog switch output must be subtracted. Table 2.1-7 lists the capacitor values and sizes implemented in the array of DCASP-2, along with the values which were implemented in DCASP-1.

It should be noted that p-n junction capacitances are inherently non-linear. This problem is alleviated to a large extent in DCASP-2 by making the p- and n- type diffusions of the OTA equal-sized and the p- and n-type diffusions of the analog switches equal-sized. The effect is shown in Fig. 2.2-17 and repeated as Fig. 2.1-14; the capacitance due to a parallel combination of equal size p- and n-type diffusions is clearly more nearly constant than the capacitance due to either the p-type or the n-type diffusion alone. (See Sec. 2.2.2.3a for a further explanation of the diffusion capacitor nonlinearities.)

The presence of parasitic capacitances other than the three discussed previously should also be noted. For example, some parasitic capacitance exists due to the metal interconnections between the OTAs and capacitor array. Also, in addition to the bottom plate of capacitors $C_1 - C_{19}$ being connected to the 19 analog switches discussed previously, the top plates of all capacitors are connected to two analog switches which help determine the filter type (see Fig. 2.1-2: Biquad Block Diagram); each switch contributes a parasitic capacitance. A parasitic capacitance also exists from the bottom plates of the capacitors $C_o - C_{19}$ to the bulk, but this is negligible since the bottom plates are connected to a low impedance node. These parasitic capacitances were not accounted for in the array of DCASP-2.

This problem of parasitic capacitance is one of the reasons for considering eliminating the capacitor array, using instead a fixed capacitor and performing the coarse tune by using only the coarse g_m control of the OTAs (see Section 2.1.2.1). This will eliminate the parasitics due to the analog switches; however, the additional output stages increase the parasitic capacitances due to the OTAs. The best structure to minimize the impact of the parasitic capacitors remains to be determined.

If the programmable capacitor array is found to be necessary or desirable in future

Table 2.1-7: Capacitor values implemented in the programmable capacitor arrays of DCASP-1 and DCASP-2. Assume $0.46 fF/\mu^2$.

N	DCASP-1 Capacitor Value $C_N(pF)$	DCASP-2 Capacitor Value $C_N(pF)$	DCASP-2 Capacitor Area (μ^2)
0	2.39	0.48	1046
1	0.31	0.26	5.65
2	0.35	0.30	652
3	0.40	0.35	761
4	0.45	0.40	870
5	0.51	0.46	1000
6	0.57	0.52	1130
7	0.65	0.60	1304
8	0.73	0.68	1478
9	0.83	0.78	1696
10	0.93	0.88	1913
11	1.05	1.00	2174
12	1.19	1.14	2478
13	1.35	1.30	2826
14	1.52	1.47	3196
15	1.72	1.67	3630
16	1.94	1.89	4109
17	2.20	2.15	4674
18	2.48	2.43	5283
19	2.80	2.75	5978

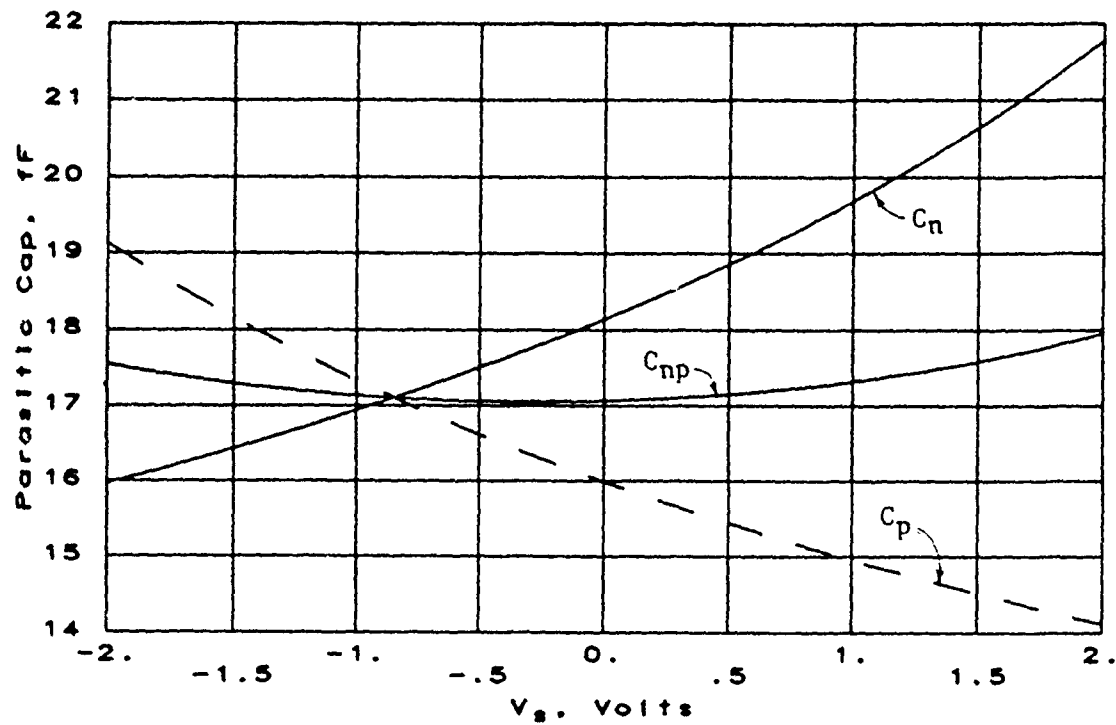


Fig. 2.1-14: Simulated small-signal capacitance for diffusion junction capacitors as a function of the DC potential, V_s , of the diffusion region relative to ground with the bulks at $\pm 5V$. ($C_n \Rightarrow n^+$ diffusion, $C_p \Rightarrow p^+$ diffusion, $C_{np} \Rightarrow \frac{C_n C_p}{C_n + C_p}$).

designs, alternative implementations may be considered. Two such implementations are discussed below.

First, consider the possibility of using capacitances which vary by factors of 1.618, i.e.,

$$C_i = C_o(1.618)^i \quad i = 0, 1, \dots, N-1 \quad (2.1-45)$$

Note the similarity to the coarse g_m control discussed in a previous section. This should offer improvements in resolution over what is obtainable with the present structure. To maintain the desired frequency range of one decade, four capacitors must be fabricated,

$$\begin{aligned} C_o &= C_u = 2.39pF \\ C_1 &= C_o(1.618) = 3.867pF \\ C_3 &= C_o(1.618)^3 = 10.124pF \\ C_5 &= C_o(1.618)^5 = 26.50pF \end{aligned} \quad (2.1-46)$$

where C_u represents a unit capacitance which is assumed to be 2.39pF. The capacitances $C_2 = C_o(1.618)^2 = C_o + C_1$, $C_4 = C_o(1.618)^4 = C_o + C_1 + C_3$ and $C_6 = C_o(1.618)^6 = C_o + C_1 + C_3 + C_5$ may be realized by switching on combinations of the four capacitors, just as was described for the coarse g_m control of the OTA. A total capacitance of 42.88pF is required to realize these four capacitors with the 2.34 pf unit capacitance. The actual range (C_6/C_o) is 17.94, which is somewhat larger than one decade.

The advantages of this technique are that the number of capacitors, the size and complexity of the digital logic circuitry, and the parasitic capacitance due to the analog switches (since fewer switches are used), are all reduced. This technique assumes, however, that the fine g_m control provides an adjustment by a factor greater than 61.8%, in order that there be no gaps in the attainable values of the ratio g_m/C .

A second possible implementation of the programmable capacitor array would have

$$C_i \leq 1.13C_{i-1} \quad (2.1-47)$$

Seven capacitors may be fabricated,

$$\begin{aligned} C_o &= 2.39pF \\ C_1 &= (1.13)C_o = 2.70pF \\ C_2 &= (1.13)C_1 = 3.05pF \\ C_3 &= (1.13)C_2 = 3.44pF \\ C_4 &= (1.13)C_3 = 3.89pF \\ C_5 &= (1.13)C_4 = 4.40pF \\ C_6 &= (1.13)C_5 = 4.97pF \end{aligned} \quad (2.1-48)$$

The remaining values of capacitance necessary to attain the desired frequency range of one decade may be realized by switching on combinations of these seven capacitors. For example, the frequency range covered by a capacitance of $(1.13)^{11}C_0 = 8.113pF$ could certainly be covered by capacitances of $C_3 + C_5 = 7.84pF$ and $C_4 + C_5 = 8.29pF$. While the corresponding frequencies would no longer be uniform on a logarithmic scale, the desired range of frequencies would still be adequately covered.

This second alternate implementation has, like the first, reduced complexity and reduced parasitic capacitance relative to the array of DCASP-2. This second implementation may also be superior for factors other than 1.13 in (2.1-47).

Table 2.1-8 provides a brief summary and comparison of the two alternate programmable capacitor array implementations and the array of DCASP-2.

2.1.4 CMOS ANALOG BUFFER

An analog buffer is needed to interface each biquadratic filter with the response and excitation busses since the OTA integrators used in the filters exhibit high output impedance. This buffer must have the ability to drive a capacitive load while exhibiting unity gain, good frequency response and high input-output linearity. Fig. 2.1-15 shows a circuit diagram of the buffer employed here. The circuit uses a simple differential pair, M_1, M_2 , followed by a Wilson current mirror, $M_3 - M_6$ having a gain m . Overall negative feedback is applied from the output to one of the differential inputs to provide a closed-loop gain that is close to unity and highly linear. The feedback also results in a low output impedance approximately equal to $1/(mg_{mi})$, where g_{mi} is the transconductance of the input pair. For the buffer implemented here, a value of $m = 5$ was used. The remaining devices are used to generate the proper input and output bias currents from the biasing voltage V_B . Device sizing information is given in Table 2.1-9.

Fig. 2.1-16 shows the simulated input-output transfer characteristic of the proposed buffer. A plot of the nonlinearity in this characteristic is shown in Fig. 2.1-17. It is evident from these figures that the buffer exhibits good linearity for input voltages within $\pm 2.5V$ (which includes the linear range of the OTAs). For positive input voltages the output saturates at approximately $+3V$ due to the two gate-source potential drops across the output mirror devices. For negative input voltages below $-3V$, the tail current devices M_{12} and M_{13} begin to turn off, which in turn causes the output mirror to turn off. This results in the sudden dip in the output voltage evident in Fig. 2.1-16. The simulated frequency response of the buffer is shown in Fig. 2.1-18 for a load capacitance of $10pF$. This plot indicates a 3-dB cutoff frequency of approximately $14MHz$. At low frequencies, the simulated buffer exhibits a gain of 0.995 and an output resistance of $1.3k\Omega$.

Table 2.1-8: Comparison of Programmable Capacitor Array Implementations.

Description	#Capacitors*	Capacitance Range (pF)	# Analog Switches	Parasitic Switch Capacitance (pF)
$C_i = (1.618)^i$	4	2.39-42.88	4	0.187
$C_i \leq 1.13C_{i-1}$	7	2.39-24.53	7	0.327
$C_i = 1.13C_{i-1}$ (DCASP-2)	20	2.39-24.37	19	0.888

* This is the number of capacitors required to allow a coarse tune of the frequency by at least one decade with no gaps (in the geometric sense) in the attainable frequencies.

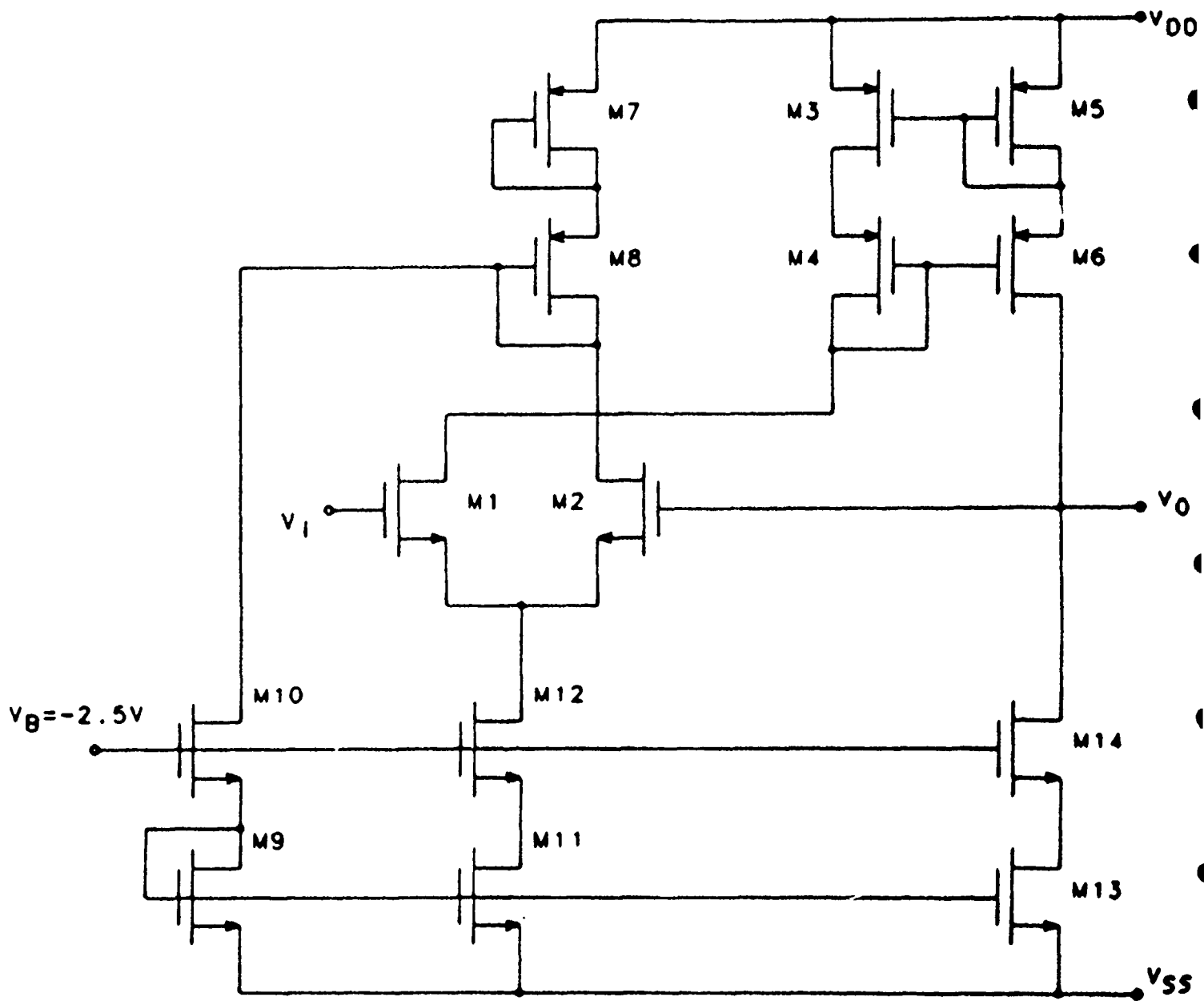


Fig. 2.1-15: Analog CMOS buffer.

Table 2.1-9: Device sizing for the buffer of Fig. 2.1-15.

DEVICE	SIZE (microns)	
	W	L
M1-M2	50	3
M3-M4	60	3
M5-M6	300	3
M7-M8	60	3
M9	4	40
M10	40	3
M11-M12	60	3
M13-M14	150	3

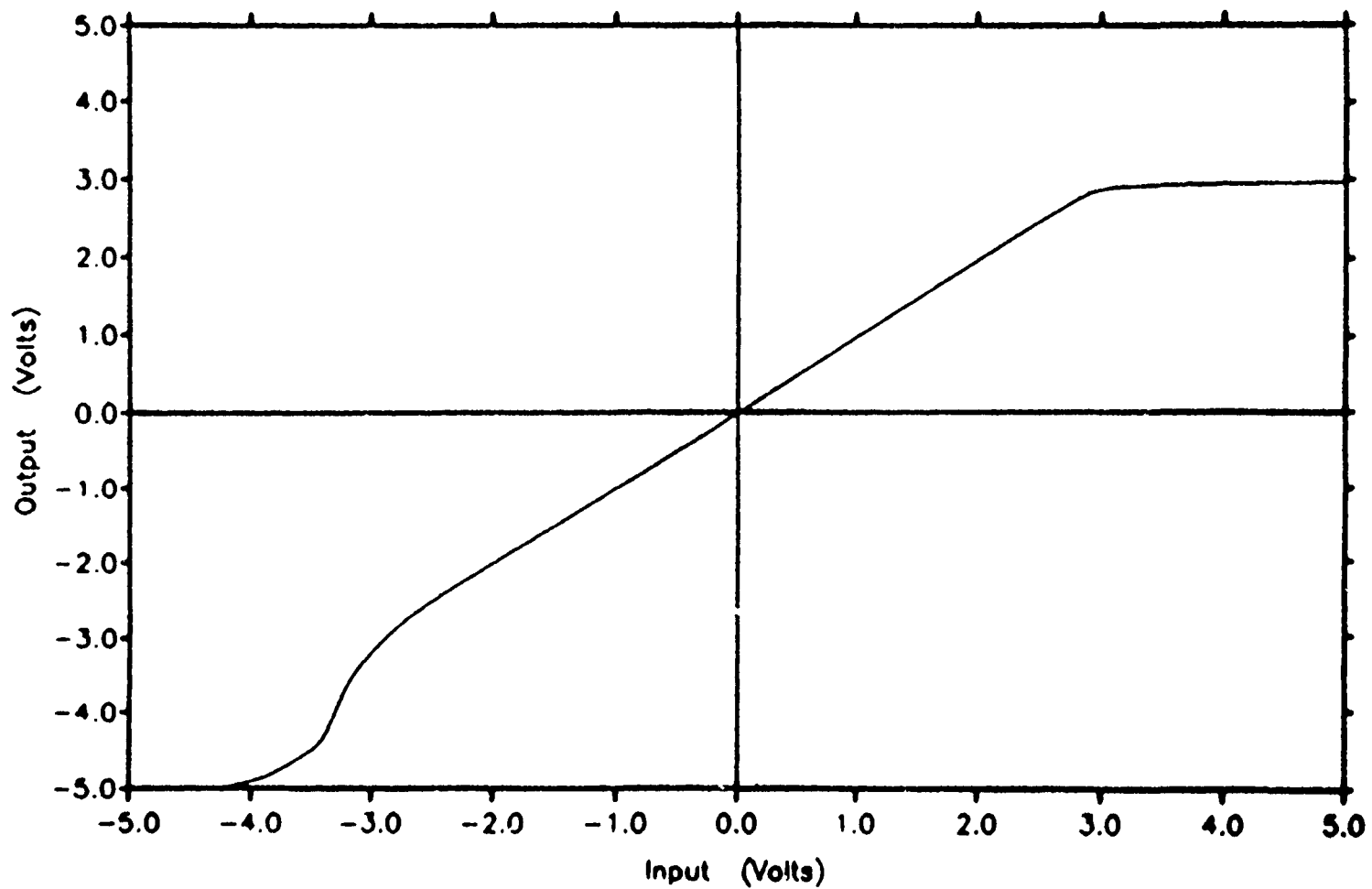


Fig. 2.1-16: Buffer transfer characteristics.

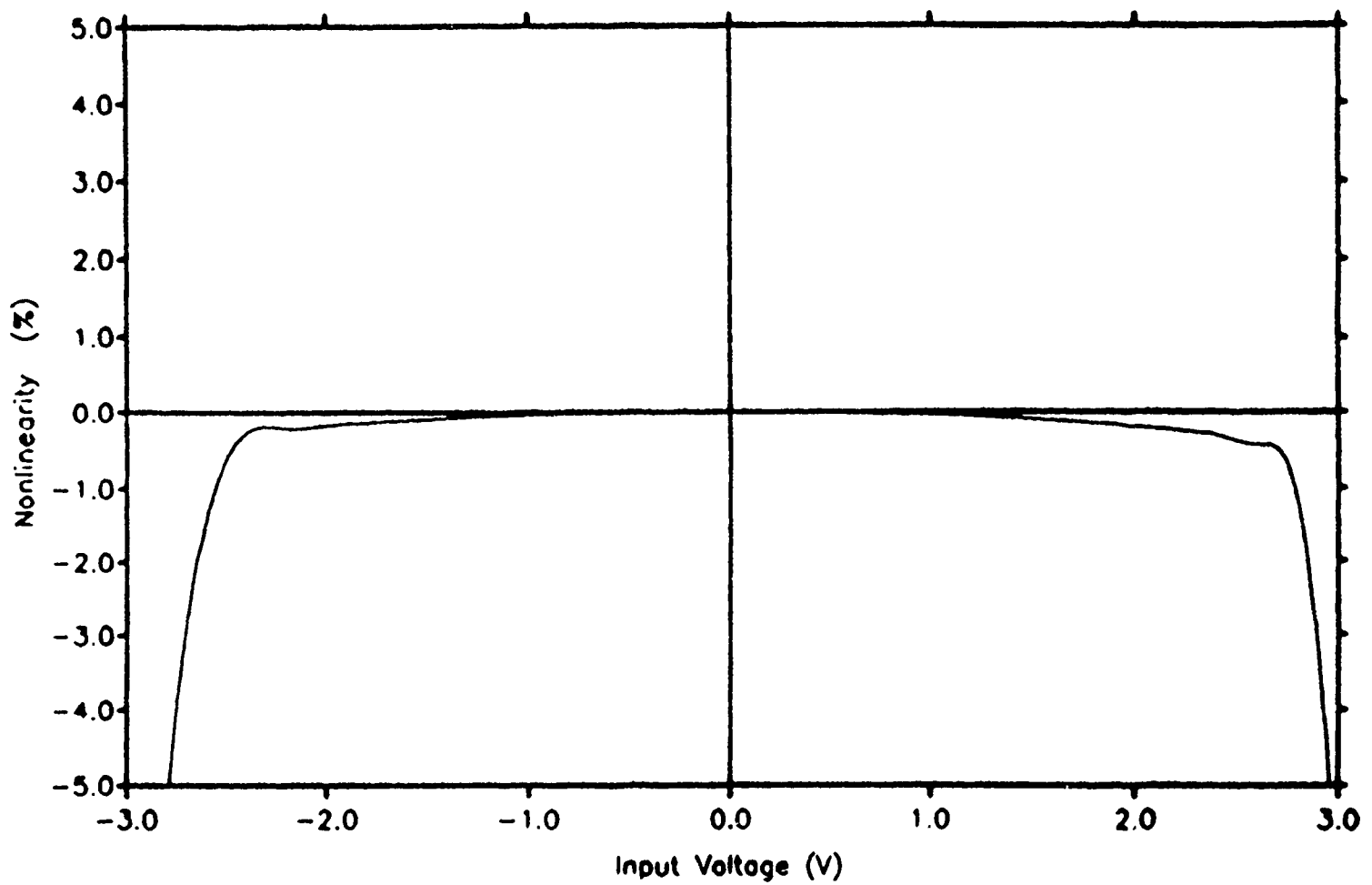


Fig. 2.1-17: Nonlinearity in buffer transfer characteristics.

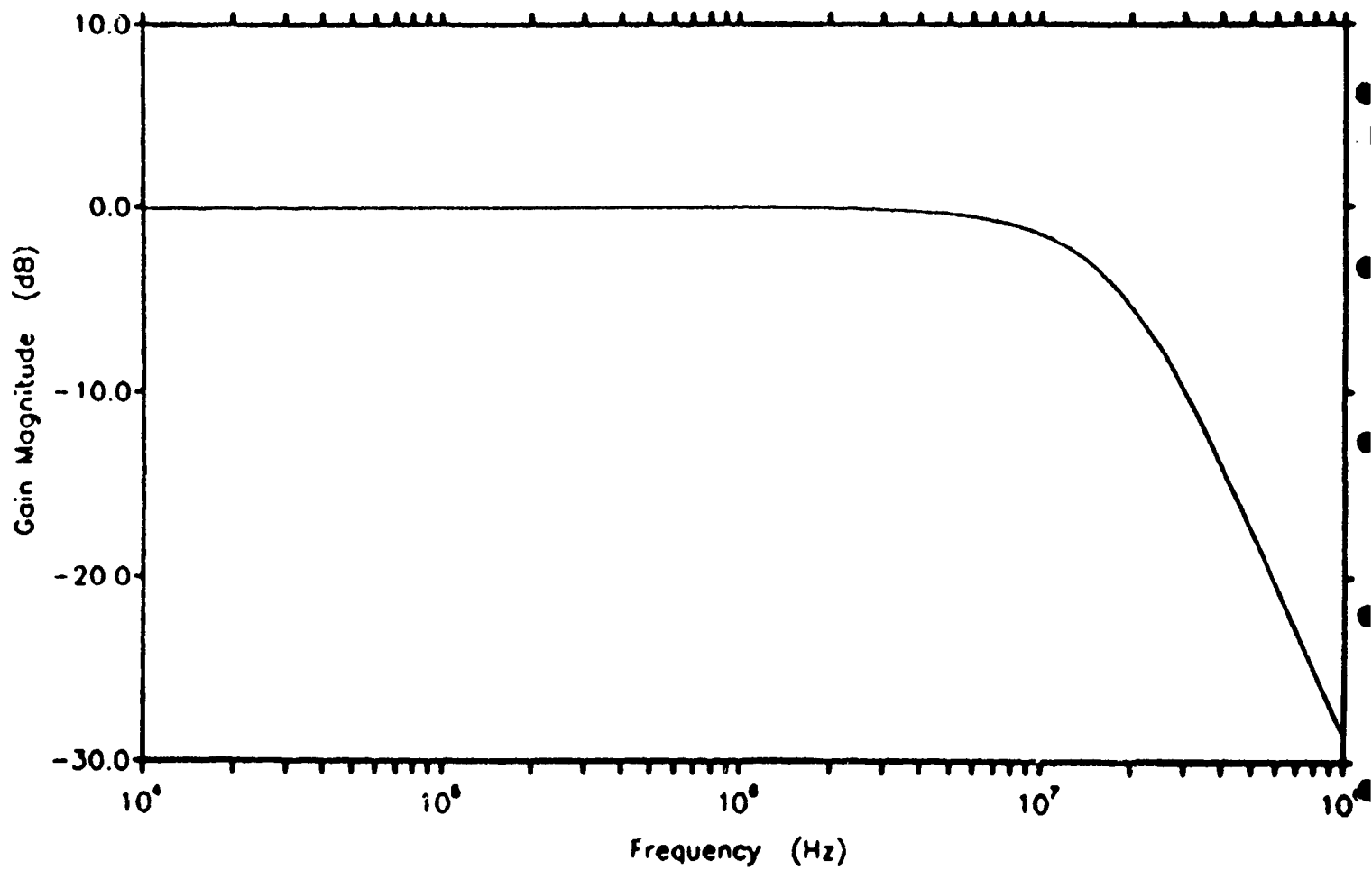


Fig. 2.1-18: Frequency response of buffer ($C_{load} = 10pF$).

2.2 Performance Measurement System

Because the DCASP architecture is dependent upon a tuning mechanism to meet system specifications in the presence of global and statistical IC process parameter variation, the overall attainable accuracy of this system is limited by the accuracy of the performance measurement or characterization system. The hardware focal point of the performance measurement system is the performance detector of the general DCASP architecture of Fig. 1.2-1. In addition to the performance measurement system is the interface between the analog Controlled Signal Processor (CSP) or filter and the tuning algorithm, as shown in Fig. 2.2-1. The role of the Performance Detector is to act as a slave to the tuning host (termed Digital Controller in Fig. 1.2-1) by providing this system with the requested measurement results. These results may range from transfer function frequency responses depicted as an array of discrete gain and phase measurements, to higher-level system specifications, such as center frequency, bandwidth, ripple, maximum gain, Q , and/or $3dB$ points.

The physical measurement consists of generating an analog excitation(s) (e.g., sinusoidal voltage source) as an input to the CSP and then recording both the excitation and corresponding response from the CSP. This excitation system is typically a programmable function generator, in which both the amplitude and frequency of the input waveform can be controlled from a digital interface. Because the actual excitation may differ from the desired excitation, this signal must be supplied to the Performance Detector hardware for characterization along with the response signal, as shown in Fig. 2.2-2. Both the excitation hardware and Performance Detector are controlled by a central performance measurement controller, which comprises a portion of the Digital Controller of the DCASP structure.

The performance measurement system can be conveniently broken into two parts,

- (1) Data Collector.

The Data Collector is responsible for making electrical measurements. These may include measuring gain and/or phase of the system transfer function at a discrete number of frequencies.

- (2) Data Interpreter.

The data interpreter is responsible for the interpretation of the data measurement results into system level specifications such as center frequency (ω_0), maximum gain (H_{max}), bandwidth (BW), Q , and/or $3dB$ points.

A discussion of data interpretation is presented next followed by a discussion of data collection hardware.

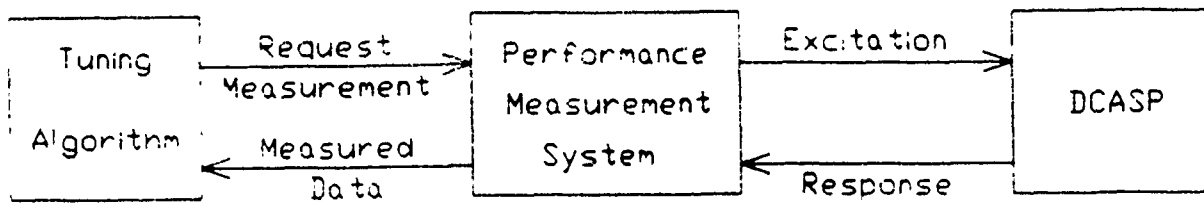


Fig. 2.2-1. Block diagram of intended performance measurement system usage in a typical tuning environment.

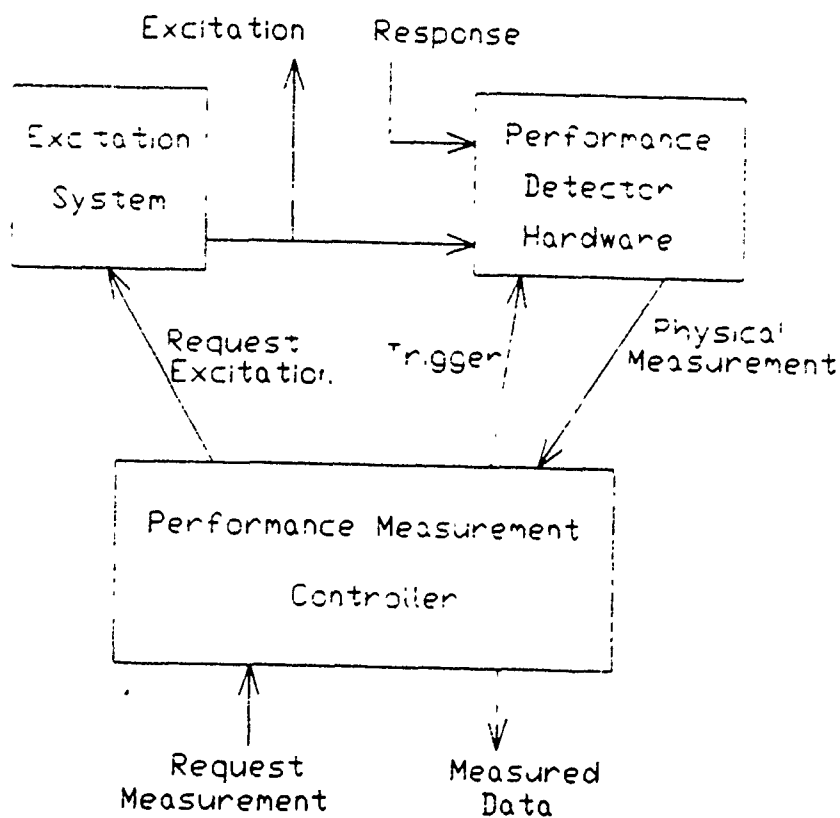


Fig. 2.2-2. Block diagram of performance measurement system.

2.2.1 Data Interpretation

In each step of the performance measurement process, (collection and interpretation) the accuracy of the input data must be known and the corresponding accuracy of the results must be computed and/or an error budget bounding the worst-case resultant error must be evaluated. The tuning algorithm depends upon accurate and consistent data.

In this section an algorithm for computing the gain and phase response from discrete time samples will be discussed. This will be followed by an investigation of a SPLINE fitting algorithm which is used to interpret measurement data and give good estimates of system transfer function characterization parameters such as peak gains, band edges and bandwidths. These discussions will be restricted to a system transfer function which closely approximates a standard second-order bandpass characteristic.

2.2.1.1 Discrete Time Sampling Algorithm

There are many different approaches for characterizing the frequency response of an unknown system transfer function, $T(s)$. These include peak detector structures, rms integrator structures and instantaneous sampling techniques. One of the most straight forward and common methods of gathering data involves using a high speed sample and hold to "grab" the data followed by a lower frequency analog to digital converter which is used to convert the sampled data to a digital representation of the signal amplitude. A method of obtaining the magnitude and phase of a system transfer function based solely upon a finite number of time domain samples of the input and output is discussed in this section. This technique relies on the post-processing of the digitized instantaneous time-domain voltage samples to obtain a single gain and phase measurement at a specific frequency. It will be initially assumed that the input and output waveforms are distortionless sinusoids of known frequency and that the system is operating in the sinusoidal steady state. If the frequency is not known, it will need to be determined independently either with the aid of the necessary hardware (e.g., frequency counter) or software. Since the reference frequency is assumed available, an accurate determination of the frequency of the excitation should not prove difficult.

A major problem to address in a time-domain based algorithm is the timing jitter involved in taking precise time-domain measurements of high-frequency signals at exact specific time instances. This timing-jitter problem can be quantitized by doing a simple worst-case sensitivity analysis of a sinusoidal waveform, $v(t)$ as a function of the timing-jitter, Δt . For the signal, $v(t) = V_m \sin(\omega t)$, it can be readily shown that the worst-case normalized deviation of an instantaneous value of $v(t)$ from its actual value satisfies the inequality

$$\frac{\Delta v(t_i)}{V_m} \leq \omega \Delta t \quad \forall t_i, \quad (2.2 - 1a)$$

where

$$\Delta v(t_i) \stackrel{\text{def}}{=} |v(t_i) - v(t_i + \Delta t)| \quad \text{and} \quad \omega \stackrel{\text{def}}{=} 2\pi f. \quad (2.2 - 1b)$$

- The impact of this problem is quantitized in Table 2.2-1. Even for relatively low frequency applications, the maximum acceptable timing jitter for 1% accuracy in function measurement is under 2η sec. In a 3μ CMOS process, gate delays, which are the major source of the timing jitter, are typically in the range of $5 - 10\eta$ s. This makes sampling at precise instances of time extremely challenging.

The following time-domain sampling algorithm minimizes the effects of the timing-jitter problem by restricting the sampling technique to simultaneous sampling of the input and output waveforms at random time intervals, thus reducing the problem to timing-jitter induced by processing mismatches or voltage dependence between two identical sample and hold circuits controlled by a common trigger signal. A description of this algorithm follows.

Consider a linear system with a sinusoidal excitation,

$$v_i(t) = V_{i_m} \sin(\omega t) \quad (2.2 - 2a)$$

The system response is of the form

$$v_o(t) = V_{o_m} \sin(\omega t + \theta) = V_{o_m} [\sin(\omega t) \cos \theta + \cos(\omega t) \sin \theta] \quad (2.2 - 2b)$$

where θ is the phase shift of the output relative to the excitation and V_{o_m} is the amplitude of the output sinusoid. Eliminating ω and the absolute time dependence, t , from the two above equations by solving simultaneously for the ωt product yields the expression

$$v_o(t) = \frac{V_{o_m}}{V_{i_m}} [v_i(t) \cos \theta + \sqrt{V_{i_m}^2 - v_i(t)^2} \sin \theta] \quad (2.2 - 3)$$

where $v_o(t)$ and $v_i(t)$ are the input and output samples which are simultaneously measured at time t . There are three unknowns in this expression; the maximum input and output amplitudes (V_{i_m} , V_{o_m}), and the phase (θ). Equivalently, the parameters V_{i_m} , gain ($H = \frac{V_{o_m}}{V_{i_m}}$), and θ can be considered as the unknown parameters. Thus, if 3 independent samples are taken in the time domain at a fixed frequency, the resulting 3 nonlinear equations can be simultaneously solved for the gain (H), phase (θ), and input signal amplitude (V_{i_m}). A solution of these three simultaneous equations for H and θ is given in (2.2-4). The expression for V_{i_m} is not given because it is not of interest at this point.

$$H = \sqrt{\frac{k_{oo}(3,2)k_{oi}(2,1) - k_{oo}(2,1)k_{oi}(3,2)}{k_{ii}(2,1)k_{oi}(3,2) - k_{ii}(3,2)k_{oi}(2,1)}}} \quad (2.2 - 4a)$$

$$\cos \theta = \frac{H^2 k_{ii}(3,2) + k_{oo}(3,2)}{2k_{oi}(3,2)H} \quad (2.2 - 4b)$$

where,

$$\begin{aligned} k_{ii}(n,m) &= v_{i_n}^2 - v_{i_m}^2 \\ k_{oi}(n,m) &= v_{o_n} v_{i_n} - v_{o_m} v_{i_m} \\ k_{oo}(n,m) &= v_{o_n}^2 - v_{o_m}^2 \end{aligned} \quad (2.2 - 4c)$$

Table 2.2-1. Timing-Jitter effects on sampling high-frequency sinusoidal waveforms.

f	$\frac{\Delta v(t_i)}{V_m}$	Δt	f	$\frac{\Delta v(t_i)}{V_m}$	Δt
2MHz	1%	1.6ns	5MHz	1%	640ps
2MHz	.5%	800ps	5MHz	.5%	320ps
2MHz	.2%	320ps	5MHz	.2%	130ps
2MHz	.1%	160ps	5MHz	.1%	64ps

and where $v_{i_n} \stackrel{\text{def}}{=} v_i(t_n)$, $v_{o_n} \stackrel{\text{def}}{=} v_o(t_n)$ for independent time instances, t_1 , t_2 , and t_3 . From (2.2-4) it is apparent that the magnitude and phase of $T(s)$ can be readily determined with a modest amount of post-processing entirely from the measured input and output amplitudes at three randomly spaced points in time.

The key assumptions in the above formulation are repeated below.

- (1) The input signal is an undistorted sinusoid which is stable in frequency, amplitude, and phase.
- (2) The system has reached steady-state and the output signal is undistorted and offset free.
- (3) Input and output signals are sampled simultaneously.
- (4) The Performance Detector (amplitude measurement circuit) is of infinite precision and accuracy.
- (5) The samples t_1 , t_2 and t_3 are independent in the sense that the three equations of the form of (2.2-3) are independent equations.

In actuality, the performance measurement system will not be ideal and minor violation of all five key assumptions can be expected. It is important that the errors induced by these effects be quantitized and bounded.

Item (1) and (2) above can be handled by incorporating these nonidealities, such as DC offsets, harmonic distortion, slewing, etc. into the overall system model, at the expense of requiring additional samples and increased computational complexity. The inaccuracies of item (4) above, may very well require modeling and characterization of the Performance Detector's nonidealities, such as voltage dependent nonlinearities. If the independence of temporal samples is difficult to guarantee, oversampling and smoothing techniques can be used. Additional simulations of the affects of these nonidealities are under investigation; however, it is not anticipated that these affects will be too problematic.

2.2.1.2 Functional Filter Parameter Determination

In the previous section, an algorithm and architecture was proposed for collecting a series of discrete data points relating gain and phase measurements to a measured excitation frequency. Motivated by the tuning algorithm, this set of data needs to be interpreted or related to the functional design parameters of the filter being characterized and tuned. In this section, the interpretation problem will be properly formulated, and several potential solutions presented.

2.2.1.2a Problem formulation.

Assume a set of gain measurements representing points the frequency response of an unknown system transfer function, $T_{ACT}(s)|_{s=j\omega}$ has been obtained. For example, these frequencies may be $\{H(\omega_i) \stackrel{\text{def}}{=} |T_{MEAS}(j\omega_i)|, \text{ for } i = 1, 2, \dots, n\}$, where ω_i represents a series of discrete frequencies and T_{MEAS} denotes the measured value of the transfer function $T_{ACT}(s)$ of $s = j\omega_i$. Assume further that we wish to extract information about T_{ACT} , such as pole Q , peak gain (H_{max}), bandwidth (BW), center frequency (ω_o), ripple, 3dB points, etc., from the measured data points that would normally characterize the performance of that particular filter.

Several factors make the determination of the characterizing performance parameters non-trivial. First, only a finite set of measured data points is usually available and even this set may be small. The characterization parameters of interest are often not the measured data points nor some simple function of the data points. Furthermore, there are usually measurement errors associated with the measured data points.

The characterization of a network for the purpose of satisfying an existing need can often be made in more than one way resulting in differing characterization parameters. Some characterizations may make the determination of these parameters much easier than others.

One obvious approach to the problem is to use the measured data points to obtain a rational fraction approximation, $\tilde{T}(s)$, of $T_{ACT}(s)$. This is motivated by the fact that $T_{ACT}(s)$ is, itself, assumed to be a rational fraction providing potential for $\tilde{T}(s)$ to be a very good approximation of $T_{ACT}(s)$. This is further motivated by the fact if the functional form of $\tilde{T}(s)$ is known, then optimization algorithms such as a least squares curve fit may be used for determining the values of the coefficients of $\tilde{T}(s)$ from the measured data points. Once $\tilde{T}(s)$ is known, most characterization parameters of interest can be readily obtained from $\tilde{T}(s)$.

This approach is complicated by two factors. First, since the exact functional form of $T_{ACT}(s)$ is unknown, a fit of the data of $\tilde{T}(s)$ may result in a $\tilde{T}(s)$ which differs considerably from $T_{ACT}(s)$. Second, optimization algorithms which fit data to rational fractions tend to be computationally intense and tend to converge to local minimums which may differ considerably from the global minimums. This is in contrast to algorithms which fit data to polynomials which are often well behaved.

The major purpose of the above approach was the determination of the rational fraction $\tilde{T}(s)$ from which the characterization parameters of interest could be readily determined. This determination will be made by a digital computer. Although the system itself is actually characterized by the rational fraction, $T_{ACT}(s)$, it is not the rational fraction form of $\tilde{T}(s)$ that makes the determination of the parameters of interest straightforward but rather the continuity of $\tilde{T}(s)$ which is inherent in any rational fraction. With the realization that it is the continuity rather than the rational fraction nature of $\tilde{T}(s)$ that

is of interest, other approximations of $T_{ACT}(s)$ or its magnitude or phase may also be considered.

With these observations, the problem will be approached as follows

1. The performance characterization parameters will be restricted to those parameters which can be readily determined from $|T_{ACT}(j\omega)|$. This includes such parameters as bandwidth, band edge, peak gain and resonant frequency but practically excludes parameters such as pole locations and pole Q .
2. A continuous approximation $\hat{H}(\omega)$ of $|T_{ACT}(j\omega)|$ will be made based upon the sampled data points.
3. The performance characterization parameters will be obtained from $\hat{H}(\omega)$.

The restriction to magnitude functions is made primarily for notational convenience and the fact that in most applications, the performance characterization parameters of interest are based upon $|T_{ACT}(j\omega)|$. It is thought that inclusion of phase parameters will not significantly complicate the above approach.

This can best be illustrated with an example, as follows:

Example:

Consider a 2nd-order bandpass filter, characterized by the bandwidth (BW), center frequency (ω_o), and the maximum gain (A_{maz}), as defined below.

$$\begin{aligned} A_{maz} &\stackrel{\text{def}}{=} \max_{\omega} |T_{ACT}(j\omega)| \\ BW &\stackrel{\text{def}}{=} \omega_{3dB_2} - \omega_{3dB_1} \\ \omega_o &\stackrel{\text{def}}{=} \sqrt{\omega_{3dB_1} \omega_{3dB_2}} \end{aligned} \quad (2.2-5)$$

For this system the extraction procedure would be as follows:

- (1) collect a series of gain measurements from the performance detector hardware, as depicted in Fig. 2.2-3a;
- (2) fit a function, $\hat{H}(\omega)$, or curve to these data points, as shown in Fig. 2.2-3b;
- (3) locate A_{maz} , compute $A_{maz} - 3dB$ and locate the 3dB points of the filter's frequency response, as shown in Fig. 2.2-3c.

This simple example illustrates the basic steps involved in characterizing a filter's observable design parameters. The real problem is much more complicated than this: (1) the curve fitting algorithm must tolerate quantization effects

and measurement errors associated with the performance detector, and slight variation in the number of data points in the passband and/or their locations; (2) both the extraction and tuning algorithm must tolerate and/or model curves with multiple inflection points as found in higher-ordered systems, as shown in Fig. 2.2-3d.

Since there are many different types of filter responses (e.g., bandpass, lowpass, lowpass-notch, etc.) with each type of filter having its own set of typical design classification parameters, the scope of the problem is large. At this stage, the problem shall be limited to the bandpass filters realizable by DCASP-2, which are ideally second-order. Besides limiting the class of filters and the range of possible Q and ω_o , it also limits the effects of the parasitic over-ordering to systems that are predominately 2nd-order. More specifically, this guarantees that the parasitic poles and zeros are well beyond the passband of the bandpass filter. This simplifies step (3) of the extraction process (listed above). Higher-order filters will be investigated at a future date.

With the scope of the problem restricted and the extraction approach specified, the remainder of the problem formulation is the determination of a good method for obtaining the continuous fitting function $\hat{H}(\omega)$. Both accuracy and computational efficiency will be considered when addressing this problem.

Figures of merit for evaluating each of the algorithms, are the worst-case percent deviation between the computed ω_o and BW , and their actual values. These deviations will be considered for the complete gambit of 2nd-order bandpass filters realizable by DCASP-2. The number and location of the sample data points required for good accuracy will also be considered as will the time required for the curve fitting.

A system model will now be developed which can be used to simulate the performance of different curve fitting algorithms. This model will approximate the actual model of the Biquads in DCASP-2.

High-Order Biquad model.:

The ideal transfer function for the DCASP-2 Biquad of Fig. 2.1-2 when configured to realize the bandpass transfer function (see equivalent circuit of Fig. 2.2-3') has been previously reported and is given by (2.2-6).

$$T_{IDEAL}(s) = \frac{\frac{g_{m4}}{c}s}{s^2 + \frac{g_{m5}}{c}s + \frac{g_{m4}g_{m3}}{c^2}}, \quad (2.2-6)$$

which can be expressed in normalized form by the equation

$$T_{IDEAL}(s) = \frac{\alpha_4 s}{s^2 + \alpha_5 s + \alpha_2 \alpha_3} \quad (2.2-7)$$

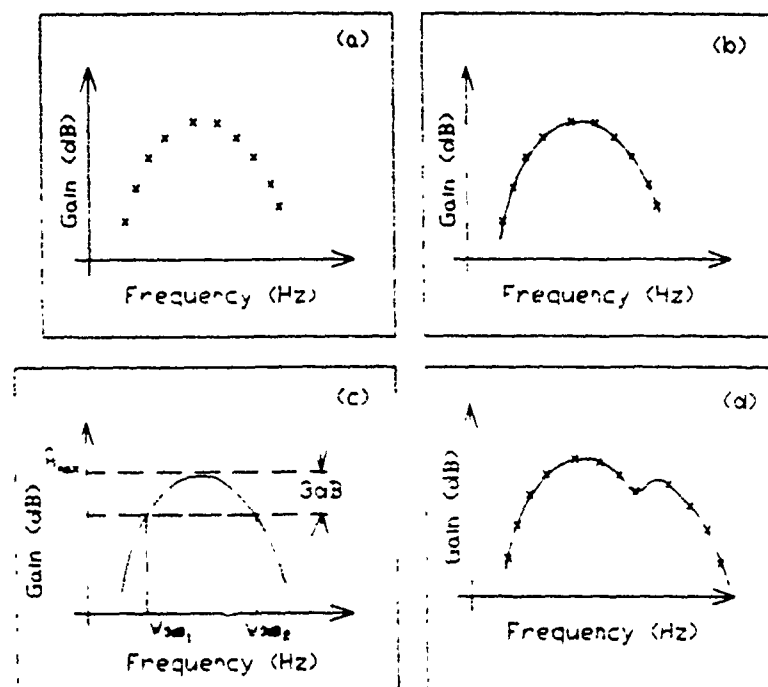


Fig. 2.2-3 a) b), c), d). Extraction of filter design parameters for previous example.

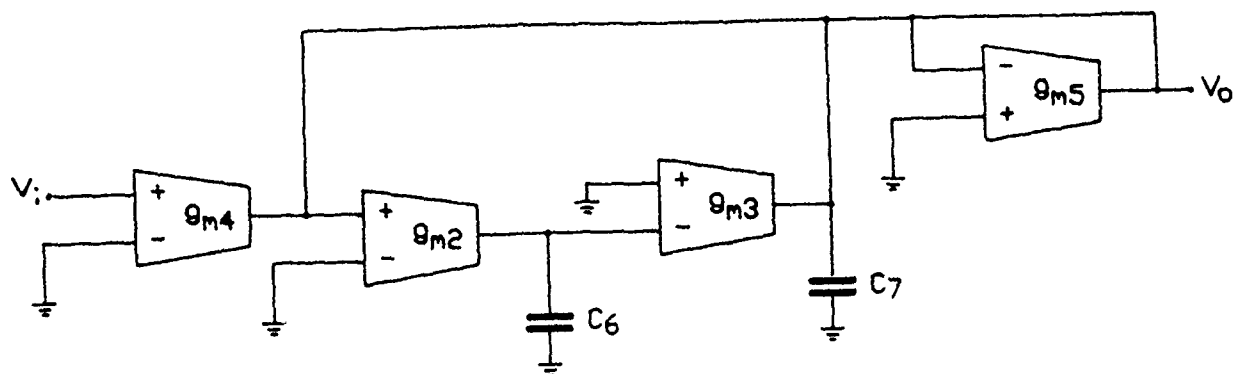


Fig. 2.2-3': TAC Bandpass Filter

$$\frac{V_o}{V_i} = \frac{g_{m4}C_6s}{s^2C_6C_7 + sC_6g_{m5} + g_{m2}g_{m3}}$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_6C_7}}$$

$$BW = \frac{g_{m5}}{C_7}$$

where it is assumed that the capacitors C_6 and C_7 are equal, $C_6 = C_7 = C$ and where the Laplace Transform variable s is actually the normalized Laplace Transform Variable s_n obtained from the normalization

$$s_n = \frac{sC}{g_m} \quad (2.2-8)$$

The parameter g_m is a normalization parameter with units conductance and the α parameters in (2.2-6) are defined by

$$\alpha_i = \frac{g_{mi}}{g_m} \quad i = 2, 3, 4 \text{ and } 5 \quad (2.2-9)$$

The subscript on s has now been used in (2.2-7) to reduce notational complexity in what is to follow.

From these equations several ideal characteristic filter parameters which are often of interest can be computed as follows.

$$\omega_o = \frac{\sqrt{g_{m2}g_{m3}}}{c} \stackrel{\text{norm}}{=} \sqrt{\alpha_2\alpha_3} \quad (2.2-10a)$$

$$BW = \frac{g_{m3}}{c} \stackrel{\text{norm}}{=} \alpha_5 \quad (2.2-10b)$$

$$Q = \frac{\omega_o}{BW} \quad (2.2-10c)$$

$$\omega_{3dB_1} = \frac{-BW + \sqrt{4\omega_o^2 - BW^2}}{2} \quad (2.2-10d)$$

$$\omega_{3dB_2} = \frac{+BW + \sqrt{4\omega_o^2 - BW^2}}{2} \quad (2.2-10e)$$

where ω_o is the frequency where the gain peaks, BW is the 3dB bandwidth, Q is the pole Q and ω_{3dB_1} and ω_{3dB_2} are the two frequencies where the gain is down 3dB from its peak value. The equations for ω_{3dB_1} and ω_{3dB_2} satisfy the expressions,

$$\omega_{3dB_1}\omega_{3dB_2} = \omega_o^2 \quad (2.2-11a)$$

$$\omega_{3dB_2} - \omega_{3dB_1} = BW \quad (2.2-11b)$$

Now that we have developed the ideal transfer function, we can extend our model by including the dominant parasitic effects. These are the finite output impedance of the OTA and the high frequency roll off of the gain of the OTA. The finite output impedance of the i^{th} OTA can be modeled by an output conductance, g_{oi} as shown in Fig. 2.2-4. Typically, $100 < \frac{g_{mi}}{g_{oi}} < 300$. Ideally $g_{oi} = 0$

A single pole model for the OTA is useful for modeling the high frequency roll-off of the device and is characterized by the equation

$$g_m(s) = \frac{g_{m_{oi}}}{1 + \frac{s}{\omega_{pi}}}, \quad (2.2 - 12)$$

where $g_{m_{oi}}$ is the low frequency transconductance gain and the ω_{pi} term is the pole frequency. Typically, $10 < \frac{\omega_{pi}}{\omega_o} < 20$, and ideally $\omega_{pi} = \infty$.

Applying these models to the biquadratic circuit, a model of the transfer function of the circuit which includes the major parasitics is, in normalized form, given by the expression

$$T_M(s) = \frac{\alpha_{04}s + (a_2s^2 + a_1s + a_0)}{s^2 + \alpha_{05}s + \alpha_{02}\alpha_{03} + (b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0)} \quad (2.2 - 13)$$

where it is assumed that $\omega_{p1} = \omega_{p2} = \omega_{p3} = \omega_{p4} = \omega_p$ and where s is the same normalization parameter as used in (2.2-8). The parameters α_{02} , α_{03} , α_{04} and α_{05} are as in (2.2-9) with g_m replaced with $g_{m_{oi}}$. In this model, parasitics are included in the polynomials involving the "a" and "b" coefficients. If we define the normalized output conductances and parasitic pole frequencies by the expressions

$$\beta_{oi} = \frac{g_{oi}}{g_m} \quad (2.2 - 14)$$

and

$$\omega_{pn} = \omega_p \frac{C}{g_m} \quad (2.2 - 15)$$

then the a and b coefficients in (2.2-13) are given by

$$\begin{aligned} a_0 &= \beta_{02}\alpha_{04} \\ a_1 &= \frac{\alpha_{04}\beta_{02}}{\omega_{pn}} \\ a_2 &= \frac{\alpha_{04}}{\omega_{pn}} \\ b_0 &= \beta_{02}\alpha_{05} + \beta_{02}(\beta_{03} + \beta_{04} + \beta_{05}) \\ b_1 &= \beta_{02} + \beta_{03} + \beta_{04} + \beta_{05} + \frac{\beta_{02}}{\omega_{pn}}(\alpha_{05} + 2[\beta_{03} + \beta_{04} + \beta_{05}]) \\ b_2 &= \frac{\alpha_{05}}{\omega_{pn}} + \frac{2}{\omega_{pn}}(\beta_{02} + \beta_{03} + \beta_{04} + \beta_{05}) + \frac{\beta_{02}(\beta_{03} + \beta_{04} + \beta_{05})}{\omega_{pn}^2} \\ b_3 &= \frac{2}{\omega_{pn}} + \frac{(\beta_{02} + \beta_{03} + \beta_{04} + \beta_{05})}{\omega_{pn}^2} \\ b_4 &= \frac{1}{\omega_{pn}^2} \end{aligned} \quad (2.2 - 16)$$

$$(2.2 - 17)$$

Ideally all "a" and "b" coefficients are zero.

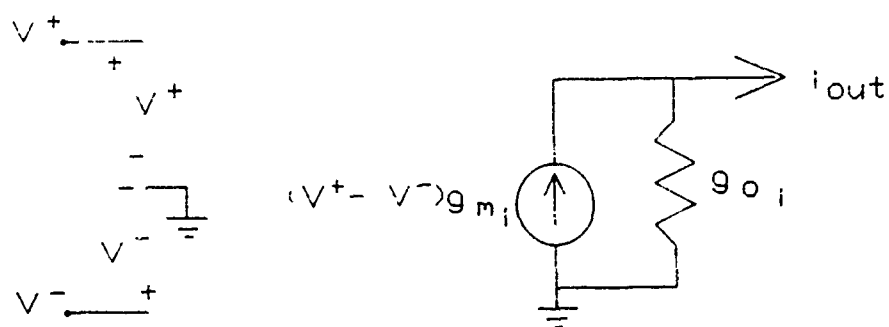


Fig. 2.2-4. OTA model including finite output impedance effects.

2.2.1.2b Functional filter parameter interpolation algorithms.

There are many interpolation or curve fitting algorithms for fitting a continuous function to a discrete set of data points available in the literature utilizing many different approximating functions. Some of these functions are as follows:

- polynomial: $p(x) = \sum a_i x^i$;
- spline or piece-wise polynomial — distinct polynomials approximating the function on adjacent intervals;
- rational fraction, a ratio of two polynomials $p_n(x)/p_m(x)$;
- Chebyshev series,
- and many others (fourier series, exponentials, etc.).[17,18]

There are also many different interpolation algorithms, such as

- least squares approximation,
- Lagrange interpolating polynomial,
- Newton interpolating polynomial,
- Aitken linear interpolation method
- Gregory-Newton interpolation,
- cubic spline interpolation, etc.[17]

Basically, the interpolation algorithm uses a specific approximation function (e.g., n_{th} -order polynomial function), with a specialized criterion for determining the so called "best fit". These two aspects differentiate one algorithm from another. Our goal here is to find the algorithm and approximation function that "best fits" our specific application (i.e., 2nd-order Biquads with both high and low Q).

If an approximation of the magnitude of $T_{ACT}(s)$ is of interest, a polynomial fit of the measured data in terms of the parameter ω is one of the most obvious approaches. Unfortunately, simulations have shown that polynomial fits of reasonably low order with a reasonably small number of sample points do a poor job of approximating a rational fraction over a very large range of ω values. These simulations also show that low-order polynomial fits with a small number of sample points do, however, fit rational fractions very well over a small (local) range of ω values. A discussion of several curve fitting functions and algorithms follows.

All are collocation algorithms in which the parameters which characterize a particular function type are selected so that the sample points and approximating functions agree at the sample points. In all cases the number of sample points is the same as the number of parameters in the characterizing function. Algorithms in which the number of data points exceed the number of parameters are under investigation but are not reported at this time. These latter algorithms are less sensitive to measurement errors in the data

and may also be useful in eliminating some of the local variations that are inherent in collocation approaches when the functional form of the model which is used for fitting differs from the actual system from which the data was gathered.

Rational-Fraction curve fitting algorithm based upon Newton-Raphson:

Two types of rational fraction fitting to measured data deserve consideration. Since it is assumed that the actual system is linear, it has a transfer function of the form

$$T_{ACT}(s) = \frac{\sum_{i=0}^m a_i s^i}{\sum_{i=0}^n b_i s^i} \quad (2.2 - 18)$$

A rational fraction fit in the s -variable is motivated by the fact that if the approximating function were to have an m_{th} -order numerator polynomial and an n_{th} -order polynomial, and if there were no measurement or fitting errors, then for the appropriate coefficients, the approximating function would be *identical* to $T_{ACT}(s)$ for all frequencies.

This approach is complicated by three primary factors. First, m and n are often unknown or are sufficiently large to make determination of the $m + n$ coefficients impractical. Second, measurements are generally real rather than complex numbers. Consequently, we may have measurements about $|T_{ACT}(j\omega)|$ at the sample points but not of $T_{ACT}(j\omega)$. Although we could take the magnitude of $T_{ACT}(j\omega)$ to obtain a fit to the resulting magnitude function, the inverse mapping needed to obtain $T_{ACT}(s)$ is non-unique and possibly nonexistent. Third, the set of equations which must be solved to obtain the a and b coefficients in the approximating function is nonlinear and the solution is computationally intense.

A second type of rational fraction fit involves fitting a rational fraction in the parameter ω to the sampled data points. Generally, there is no inverse mapping to a rational fraction in the s -domain which will agree in the magnitude sense with the approximating function itself. Thus, this approach generally guarantees that the fit to the actual function will not be perfect. This approach is motivated, however, by the fact that these approximations may be easier to make and by our conjecture that due to the fact that the inherent shape of most system transfer function looks more like that of a rational fraction in the ω domain rather than a polynomial in the ω domain, considerably fewer coefficients will be needed to obtain a good rational fraction fit than will be needed to obtain a good polynomial fit.

Mathematically, consider a system which can be modelled by a rational fraction of

the form

$$H(\omega) = \frac{N(\omega)}{D(\omega)} = \frac{\sum_{i=0}^s a_i \omega^i}{\sum_{j=0}^t b_j \omega^j}, \quad (2.2 - 19)$$

where some subset of a_i and b_j may a priori be defined to be zero and any one of the non-zero coefficients may be arbitrarily assigned any non-zero value. Thus for a system approximated by $n + 1$ non-zero and n unknown coefficients and characterized by n independent gain measurements ($\hat{H}(\omega_k)$, for $k = 1, 2, \dots, n$), there exist n independent non-linear equations

$$H(\omega_k) - \hat{H}(\omega_k) = 0 \text{ for } k = 1, 2, \dots, n \quad (2.2 - 19a)$$

A closed form solution of this n_{th} -order non-linear system is not readily obtainable. A more standard approach is to use the modified Newton-Raphson numerical technique to find the roots of this set of equations.

Our system of non-linear equations can be expressed as

$$f_k(\mathbf{x}) = 0 \text{ for } k = 1, 2, \dots, n, \quad (2.2 - 20)$$

or yet simpler

$$\mathbf{f}(\mathbf{x}) = 0, \quad (2.2 - 21)$$

where $f_k(\mathbf{x}) \stackrel{\text{def}}{=} H(\omega_k) - \hat{H}(\omega_k)$ for $k = 1, 2, \dots, n$, and \mathbf{x} denotes the vector containing $n + 1$ transfer function coefficients, a_1, a_2, \dots, a_s , and b_1, b_2, \dots, b_t that are non-zero. We wish to solve this system of equations for \mathbf{x} , the vector of unknown transfer function coefficients.

The modified Newton-Raphson technique involves approximating this non-linear system with a 1st-order truncated Taylor series expansion. A standard LU decomposition of the resultant linear system is then used. A discussion of this technique follows:

- (1) Make an estimate of \mathbf{x} , termed $\mathbf{x}^{(1)}$. A good choice of the first iteration value of \mathbf{x} would be the design or expected value of \mathbf{x} .
- (2) Compute $\mathbf{f}(\mathbf{x}^{(1)})$ and the $n \times n$ Jacobean matrix ($\delta \mathbf{f}(\mathbf{x}^{(1)})$), defined as

$$\delta f_{i,j}(\mathbf{x}^{(1)}) \stackrel{\text{def}}{=} \left. \frac{\delta f_i(\mathbf{x})}{\delta x_j} \right|_{\mathbf{x}=\mathbf{x}^{(1)}}.$$

- (3) Solve the linear system, $\delta \mathbf{f}(\mathbf{x}^{(1)}) \delta \mathbf{x} = -\mathbf{f}(\mathbf{x}^{(1)})$, for $\delta \mathbf{x}$, which represents an estimate in the error in $\mathbf{x}^{(1)}$.
- (4) Make a new estimate of \mathbf{x} , $\mathbf{x}^{(2)}$, from the expression

$$\mathbf{x}^{(2)} = \mathbf{x}^{(1)} + \delta \mathbf{x}.$$

- (5) Repeat, steps (2) through (4) as often as necessary with the latest estimates of the transfer function coefficients, until incremental changes in the coefficients is below a certain value which has been a priori agreed upon to determine convergence and thus deemed converged.

This technique has not been fully evaluated at this time, but it is suspected that this algorithm would be highly sensitive to both measurement errors in ω_k and $H(\omega_k)$, and the specific values of ω_k . If the system is not well characterized by the proposed rational fraction model, then differences between the actual and approximating function may differ significantly away from the sample points or the algorithm may actually diverge.

Polynomial Approximation via Collocation:

The polynomial approximation technique based upon collocation at the sample points is a common and obvious approach to try. The technique requires forcing an n_{th} -order polynomial ($H(\omega)$) to pass through each discrete data point, $(\omega_i, \hat{H}(\omega_i))$, for $i = 1, 2, \dots, n$. This constraint implies that there exists one and only one polynomial, $H(\omega)$, that meets these requirements. There are three common methods for computing this polynomial: Lagrange, Newton divided-differences, and the Aitken linear interpolation method. Each of these methods gives the same results though presented in a different form. The primary difference between these techniques is the computational time required and the associated round-off error. This aspect of the algorithm will not be discussed.

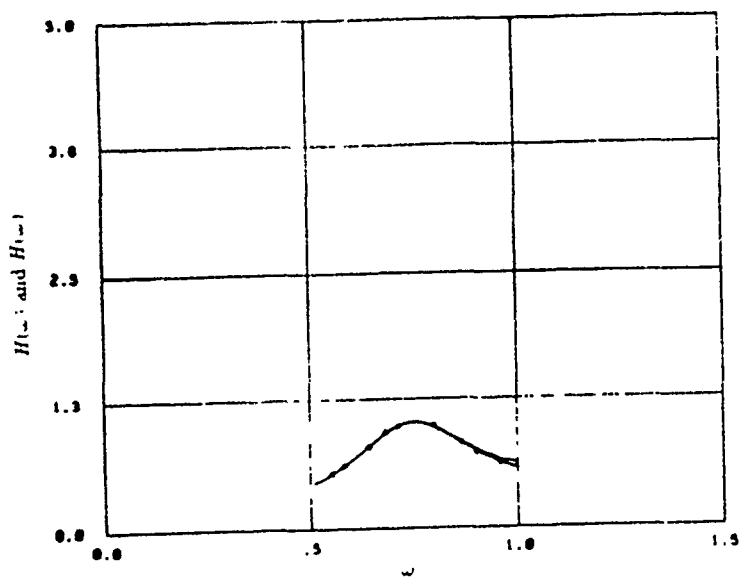
The resulting interpolating polynomial independent of the computational algorithm is shown below in eq. (2.2-22).

$$H(\omega) = \sum_{i=0}^n \hat{H}(\omega_i) \prod_{\substack{j=0 \\ j \neq i}}^n \frac{\omega - \omega_j}{\omega_i - \omega_j} \quad (2.2 - 22)$$

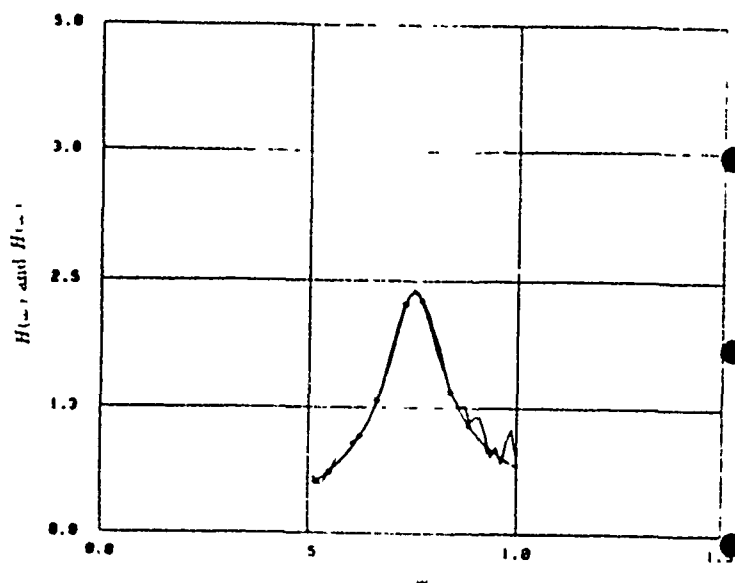
This polynomial interpolation algorithm was applied to the bandpass filter interpretation problem, in an attempt to estimate the location of the passband edges (ω_{3dB_1} and ω_{3dB_2}).

Simulation was performed on four different ideal 2nd-order bandpass filters with Q s of 1.875, 2.5, 3.75 and 7.5. In all cases, a 9th-order polynomial ($n = 10$) was passed through 10 sample points distributed rather uniformly about the resonant frequency. The results are depicted in Fig. 2.2-5.

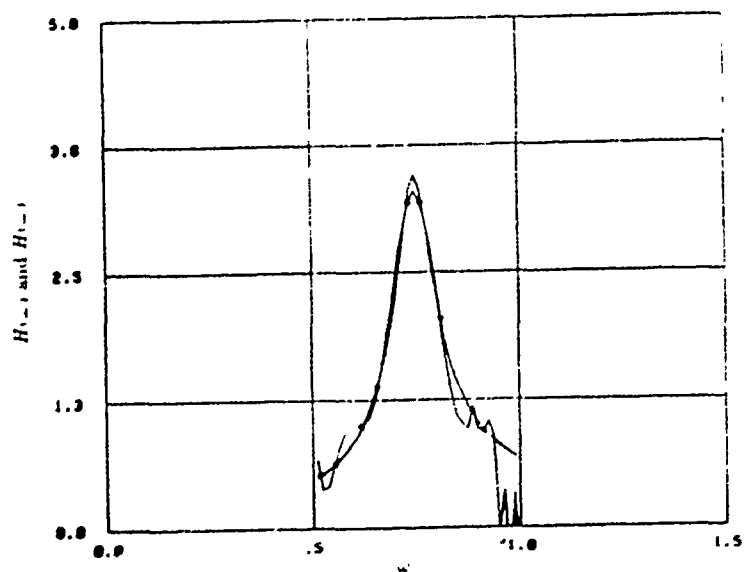
The results show that this approach requires little computation and yields fairly good results for filters with low Q 's. Definite difficulties were present outside the passband, where the polynomial could not handle the change in concavity without swinging dramatically below and above the theoretical curve, in sort of a ringing effect. This is a limitation of this approximating function. Also, at higher Q 's the polynomial function had difficulties tracking the sharp transition region near the peak (well within the passband). The



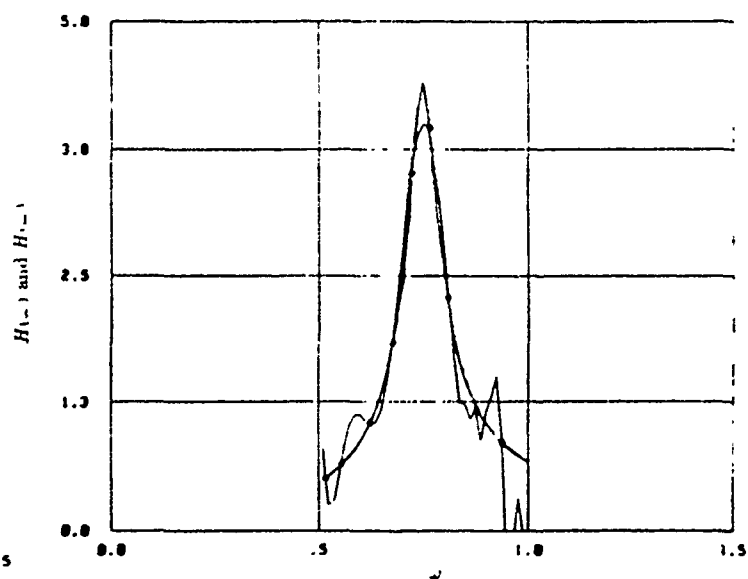
(a) $Q = 1.875$



(b) $Q = 2.5$



(c) $Q = 3.75$



(d) $Q = 7.5$

Fig. 2.2-5. Polynomial interpolation of 2nd-order bandpass transfer functions with a variety of Q 's.

problem stems from high Q filters (poles are near the $j\omega$ -axis), exhibiting a sharp peak. This is non-characteristic of polynomials and hence non-characteristic of the polynomial approximating function.

The problem could be addressed by collecting more points in the passband, but it is suspected that other approximating functions and possibly other algorithms would be better suited for this type of curve fitting problem which is characterized by fast transitions in the passband and slow changing concavity in the stop-band.

The polynomial fit does, however, appear to fit the data very well locally even though the fit over a wide domain is not too good. This motivates investigating the use of Spline functions in which the approximations are piecewise polynomial.

Spline interpolation approximation:

A spline fit of the second-order bandpass function based upon using 5 segments (4 knots) and 3rd-order polynomials is shown in Fig. 2.2-6. Only 6 sample points were used in this simulation. The spline functions avoid the need for high-order interpolating polynomials and minimize the ringing or oscillating effects associated with high-order polynomial approximations. In this section, we will mathematically describe the spline function, and present four spline based solutions to the interpolation problem.

Mathematical concept of spline function.

The spline function is an extension of the piece-wise linear function in that it pieces together low-order polynomial functions over a series of contiguous sub-intervals. The basic nature of the spline function is to guarantee both continuity and smoothness at each of the sub-interval intersections, termed "knots".

Mathematically: given n data points, $(\omega_i, \hat{H}(\omega_i))$ for $i = 1, 2, \dots, n$, there exists $(n-1)$ intervals that we desire $(n-1)$ m_{th} -order interpolating polynomial functions $(p_j^{(m)}(\omega))$ for $\omega \in [\omega_j, \omega_{j+1}]$ and $j = 1, 2, \dots, n-1$ to provide the "best fit" possible. Thus the resulting interpolation function $(H(\omega))$ would be defined as follows:

$$H(\omega) \stackrel{\text{def}}{=} \begin{cases} p_1^{(m)}(\omega) & \text{for } \omega \in [\omega_1, \omega_2]; \\ p_2^{(m)}(\omega) & \text{for } \omega \in [\omega_2, \omega_3]; \\ \vdots & \vdots \\ p_{n-1}^{(m)}(\omega) & \text{for } \omega \in [\omega_{n-1}, \omega_n]. \end{cases} \quad (2.2 - 23)$$

where $p_i^{(m)}(\omega)$ has the functional form

$$p_i^{(m)}(\omega) = \sum_{j=0}^m a_{ji} \omega^j. \quad (2.2 - 24)$$

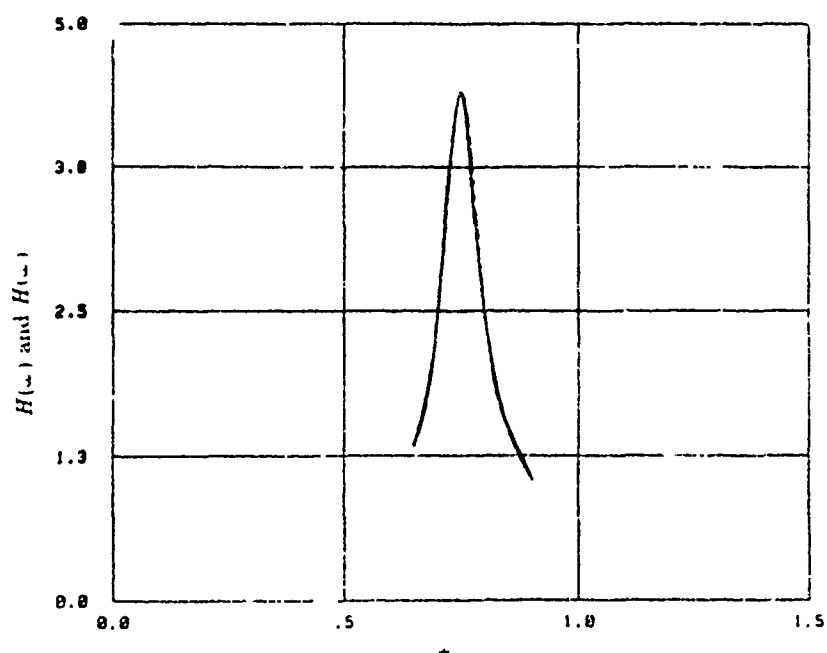


Fig. 2.2-6. Spline approximation for 2nd-order bandpass filter, (same as Fig. 2.2-5d)), with 6 measurements between 0.6 and 0.9.

The term "best fit" mentioned above, refers to a "smooth" continuous curve. Various levels of smoothness at the knots can be required. For example, the definition of a cubic spline [19] which requires agreement in function, first derivative and second derivative is given below.

- (1) The function, $H(\omega)$ must be continuous at each of the knots:

$$p_i^{(m)}(\omega_{i+1}) = p_{i+1}^{(m)}(\omega_{i+1}) \text{ for } i = 1, 2, \dots, n-1.$$
- (2) The slope of the function, $H'(\omega)$ must be continuous at each knot:

$$p_i'^{(m)}(\omega_{i+1}) = p_{i+1}'^{(m)}(\omega_{i+1}) \text{ for } i = 1, 2, \dots, n-1.$$
- (3) The curvature of the function, $H''(\omega)$ must be continuous at each knot:

$$p_i''^{(m)}(\omega_{i+1}) = p_{i+1}''^{(m)}(\omega_{i+1}) \text{ for } i = 1, 2, \dots, n-1.$$
- (4) The curvature of $H(\omega)$ must also be minimized by minimizing the order m of the interpolating polynomial segments. This should prevent ringing or oscillating, as the regular polynomial fit exhibited.

Thus, the order of the interpolating polynomials must be of degree 3 (i.e., $m = 3$). The functions are commonly referred to as a cubic spline. This results in $H''(\omega)$ functions. Now $H''(\omega)$ can be approximated via the Lagrange interpolation formula [19], along with the associated integrals of $H''(\omega)$, (i.e., $H'(\omega)$ and $H(\omega)$). Now if we impose the constraint that the first derivative must be continuous at each of the knots, we get a system of $(n-1)$ linear equations as a function of the second derivative, $H''(\omega)$ at each of the $(n-1)$ knots and the 2 end-points. This results in a system of $(n-1)$ equations and $(n+1)$ unknowns. The system becomes deterministic, if we assume that $H''(\omega_1) = 0$ and $H''(\omega_n) = 0$ — commonly referred to as a natural spline. Now, the system can be expressed as a $(n+1)$ order tridiagonal linear system and can be solved via a forward/backward substitution algorithm.

Now each of the second derivatives at each of the data points are known and the problem can be localized to solving 4 equations as shown below for 4 unknowns (a_j , for $j = 0, \dots, 3$) on each of the $(n-1)$ intervals, i , such that

$$\begin{aligned}\hat{H}(\omega_i) &= p_i^{(3)}(\omega_i) = a_0 + a_1\omega_i + a_2\omega_i^2 + a_3\omega_i^3 \\ \hat{H}(\omega_{i+1}) &= p_i^{(3)}(\omega_{i+1}) = a_0 + a_1\omega_{i+1} + a_2\omega_{i+1}^2 + a_3\omega_{i+1}^3 \\ H(\omega_i) &= p_i''^{(3)}(\omega_i) = 2a_2 + 6a_3\omega_i \\ H(\omega_{i+1}) &= p_i''^{(3)}(\omega_{i+1}) = 2a_2 + 6a_3\omega_{i+1}\end{aligned}\tag{2.2-25}$$

This briefly describes the basic steps involved in interpolating a cubic spline through n data points. For more information, see pp. 130-4 of [17].

Four knot distribution methods.

The following is a discussion of four different spline approximation methods, each using

a different selection criterion for selecting the frequencies (ω 's) that the experimental data points are taken. All use the cubic spline.

- (1) Equally spaced knot method — this method has equally spaced knots on the linear normalized frequency axis and is the obvious approach when no a priori information is known about the actual transfer function. The corresponding steps required to obtain the estimates of the filter's observable parameters (ω_o , ω_{3dB_1} and ω_{3dB_2}) can be stated as follows:

- i. collect equally spaced measurements of $H(\omega)$ as a function of ω ;
- ii. interpolate a spline function through this data; and
- iii. estimate the filter parameters.

- (2) One additional knot method — As the example of Section 2.2.1.2a, obtaining a good estimate of ω_{3dB_1} , ω_{3dB_2} is dependent upon accurately estimating H_{max} . This suggests the collection of one additional data point at the estimated location of the peak as estimated in item (1), above. Thus the resulting algorithm is as follows:

- i. execute the equally spaced procedure of item (1) above and obtain an estimate of ω_o ;
- ii. collect one additional data point near ω_o ;
- iii. interpolate a new spline function through this data; and
- iv. re-estimate the filter parameters.

- (3) Three additional knot method — Similar to the one additional knot method, this technique adds three knots at the estimated location of ω_o , ω_{3dB_1} and ω_{3dB_2} . This technique is described as follows:

- i. execute the equally spaced procedure described above;
- ii. collect three additional data point near ω_o , ω_{3dB_1} and ω_{3dB_2} ;
- iii. interpolate a new spline function through this data; and
- iv. re-estimate the filter parameters.

- (4) seven additional knot method — Similar to the two previous techniques, after obtaining estimates of where the passband is located, we add three knots at ω_o , ω_{3dB_1} and ω_{3dB_2} , two equally spaced knots between ω_{3dB_1} and ω_o , and two equally spaced knots between ω_o , and ω_{3dB_2} . Now, re-compute the spline function and estimate the filter parameters, that is

- i. execute the equally spaced procedure described above;
- ii. collect seven additional data point as mentioned above;
- iii. interpolate a new spline function through this data; and
- iv. re-estimate the filter parameters.

Simulation results.

An initial set of simulations were performed on the four algorithms described above using the model of (2.2-13) for the actual system. In this simulation, 3dB cutoff frequency and Q' estimates were made from the spline functions which were fitted to the data points and compared with the actual 3dB cutoff frequencies and Q' values. Here Q' is defined to be

$$Q' = \frac{\sqrt{\omega_{3dB_1} \omega_{3dB_2}}}{\omega_{3dB_2} - \omega_{3dB_1}}$$

where ω_{3dB_1} and ω_{3dB_2} are the $-3dB$ cutoff frequencies. Note that if the system were bandpass and exactly of second order, then Q' is actually equal to the pole Q . For small parasitics, Q' is close to the pole Q of the dominant pole pair. Actually, bandwidth is of more interest in most applications than the pole Q of the dominant pole pair. Q' is simply the reciprocal of the normalized bandwidth where the normalization factor is the center of the passband defined as the geometric mean of the two 3dB cutoff frequencies. Note again that in the ideal second-order bandpass case, the pole Q is also given by the expression

$$Q = \frac{\omega_o}{BW} = \frac{\sqrt{\omega_{3dB_1} \omega_{3dB_2}}}{\omega_{3dB_1} - \omega_{3dB_2}}$$

thus justifying our definition of Q' .

In these simulations, the parasitic affects were included by using typical values for the a and b coefficients in (2.2-13). Specifically, two cases were considered. The actual a and b coefficients used in these two cases are summarized in Table 2.2-3. These are of the same functional form as (2.2-16) and (2.2-17). Additional simulations using the exact forms given in (2.2-16) and (2.2-17) with accurate estimates for all parameters in these equations will be made in the future although it is anticipated that the results will differ little from those corresponding to the two cases listed in Table 2.2-3.

The results are summarized in Table 2.2-4 - Table 2.2-7. In these simulations, Q' and the center frequency were varied throughout the adjustment domain. The results were then sorted by Q' into four classes defined by

- Class 1: $0 < Q < 8$
- Class 2: $8 < Q < 15$
- Class 3: $15 < Q < 25$
- Class 4: $25 < Q < 50$

The number of samples in each class along with the percentage of the samples which accurately predicted ω_{3dB_1} and ω_{3dB_2} as well as Q' from the spline function to .1%, .2%, .5%, 1%, 2%, 5% 10% and 20% are listed in these tables. The number of sample points (knots) was varied from $n = 20$, to $n = 50$ to $n = 100$ and to $n = 300$ in these simulations.

Table 2.2-2 Comparison of 4 Spline-fit Algorithms

		CASE 1		CASE 2	
		ω_{3dB}	Q	ω_{3dB}	Q
0 Added Knots	$1 < Q < 8$	13	5	9	3
	$8 < Q < 15$	13	3	10	2
	$15 < Q < 25$	14	3	11	2
	$25 < Q < 50$	11	1	12	1
1 Added Knot	$1 < Q < 8$	15	6	11	4
	$8 < Q < 15$	15	4	11	3
	$15 < Q < 25$	15	4	12	2
	$25 < Q < 50$	15	2	13	2
3 Added Knots	$1 < Q < 8$	16	8	12	7
	$8 < Q < 15$	16	7	13	4
	$15 < Q < 25$	16	5	14	3
	$25 < Q < 50$	15	2	13	2
7 Added Knots	$1 < Q < 8$	22	11	20	10
	$8 < Q < 15$	21	9	21	8
	$15 < Q < 25$	23	8	20	5
	$25 < Q < 50$	23	5	20	4

A few comments about these results follows. First, for equally spaced knots, all ω_{3dB} values were predicted to 1% or better for all Q' -ranges with 300 points using the simple equally spaced knot algorithm summarized in Table 2.2-4a and 2.2-4b. As the number of sample points decreased, the accuracy of predicting the 3dB frequencies and the Q' values also deteriorated and became worse at higher Q values. It can be seen that by adding a few additional knots in the identified passband, significant improvements in accuracy of estimating both ω_{3dB} as well as Q' values are obtainable. Additional comments about the performance of the spline-based algorithms appear in the following section.

Comparison of Algorithms and Interpretation of Results:

The architectural similarities and differences of various approaches for obtaining ω_o , ω_{3dB_1} , and ω_{3dB_2} have been pointed out along with the basic description of these approaches. In this section, we are going to discuss their results as related to the number and location of the knots.

The polynomial approximation algorithm required the least amount of computation and provided good results for low Q filters. However, it was not reliable at higher Q 's (Q 's > 3) or when the frequency band of interest is large and exhibited ringing outside the passband.

The equally spaced spline approximation algorithm works well, but it general requires more knots to obtain the accuracy than is required for the other three spline approximation methods. For example, for $0 < Q' < 8$, and for the CASE 1 parasitic model, 100 knots provided 1% accuracy with the equally spaced knot algorithm and .5% accuracy with the other three algorithms. Correspondingly, with each addition of more knots in the four algorithms presented, a general trend to improved accuracy was observed. In an attempt to quantitatively compare these four algorithms, define as a "Figure of Merit" for each algorithm the total number of entries in each table which are at the ideal value of 100% for 3dB frequencies and for Q values. Table 2.2-2 compares these algorithms based upon this figure of merit. It can be seen from this table that the improvements with additional knots are significant and that these improvements are more pronounced in higher Q' applications.

At this point, it deserves mention that the whereas all additional knots require recalculation of the spline function, the number of total additional sample points is very small on a percentage basis. For example, with $n = 300$, the 7 additional knot algorithm requires a total of 307 samples with a net increase of just over 2%. Since the sampling time will likely dominate the calculation time for tuning algorithms based upon the spline function fits, the penalty for using the added knots is relatively insignificant. With this in mind, comments about the performance of the spline fit algorithm will be based upon the seven additional knot scheme. These results were presented in Table 2.2-7a and 2.2-7b.

First, it can be concluded that ω_{3dB} frequencies can be measured to 1% for all Q' values included provided a sufficient number of sample points are used. The numbers of sample points required to obtain approximately 1% accuracy with the seven additional

Table 2.2-3 Values of Parasitic Paramaters Used in Simulation

	CASE 1	CASE 2
a_0	0	0
a_1	0	0
a_2	$\alpha_{04}/20$	$\alpha_{04}/10$
b_0	$\alpha_{05}/1500$	$\alpha_{05}/500$
b_1	$.016 + \alpha_{05}/30,000$	$.05 + \alpha_{05}/5000$
b_2	$1/600 + \alpha_{05}/20$	$1/100 + \alpha_{05}/10$
b_3	$1/10$	$1/5$
b_4	$1/160,000$	$1/10,000$

Table 2.2-4a: Equally spaced knot algorithm, $\omega_p = 10$, $R_{ogm} = 100$.

n	0 < Q < 8							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	58	51	37	1	10	13	9	0
Percent(0.2%)	81	77	54	4	27	25	17	0
Percent(0.5%)	100	95	64	16	54	57	34	1
Percent(1%)	100	100	69	25	81	78	57	4
Percent(2%)	100	100	82	42	99	89	60	7
Percent(5%)	100	100	97	59	100	97	66	21
Percent(10%)	100	100	100	75	100	100	72	31
Percent(20%)	100	100	100	94	100	100	87	54

n	8 < Q < 15							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	68	53	13	0	4	5	1	0
Percent(0.2%)	94	72	20	0	9	13	4	0
Percent(0.5%)	100	87	37	0	31	30	8	0
Percent(1%)	100	97	80	3	60	49	12	0
Percent(2%)	100	100	74	11	92	68	15	0
Percent(5%)	100	100	99	50	100	78	25	0
Percent(10%)	100	100	100	72	100	90	39	1
Percent(20%)	100	100	100	100	100	99	68	8

n	15 < Q < 25							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	98	98	98	98	98	98	98	98
Percent(0.1%)	68	23	1	0	3	2	0	0
Percent(0.2%)	99	47	2	0	5	2	0	0
Percent(0.5%)	100	79	10	0	19	5	1	0
Percent(1%)	100	94	28	0	40	12	1	0
Percent(2%)	100	100	68	0	74	20	1	0
Percent(5%)	100	100	100	32	100	45	2	0
Percent(10%)	100	100	100	83	100	68	11	0
Percent(20%)	100	100	100	100	100	87	24	0

n	25 < Q < 50							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	66	66	66	66	66	66	66	66
Percent(0.1%)	59	2	0	0	3	0	0	0
Percent(0.2%)	97	8	0	0	5	0	0	0
Percent(0.5%)	100	30	0	0	8	0	0	0
Percent(1%)	100	71	3	0	12	0	0	0
Percent(2%)	100	98	35	0	36	0	0	0
Percent(5%)	100	100	98	0	77	3	0	0
Percent(10%)	100	100	100	0	95	12	0	0
Percent(20%)	100	100	100	0	100	32	0	0

Table 2.2-4b: Equally spaced knot algorithm, $\omega_p = 20$, $R_{ogm} = 300$.

n	0 < Q < 8							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	49	43	31	0	11	9	6	0
Percent(0.2%)	80	77	63	2	17	16	14	2
Percent(0.5%)	99	95	74	5	52	45	39	5
Percent(1%)	100	99	85	6	81	75	61	6
Percent(2%)	100	97	93	10	99	93	68	10
Percent(5%)	100	100	95	30	100	98	75	30
Percent(10%)	100	100	99	50	100	99	86	50
Percent(20%)	100	100	100	61	100	99	94	51

n	8 < Q < 15							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	82	82	82	82	82	82	82	82
Percent(0.1%)	34	21	7	0	4	4	0	0
Percent(0.2%)	91	46	18	0	4	5	1	0
Percent(0.5%)	100	67	28	0	17	12	1	0
Percent(1%)	100	69	41	0	28	24	5	0
Percent(2%)	100	91	50	0	83	44	12	0
Percent(5%)	100	100	82	35	99	54	21	0
Percent(10%)	100	100	98	61	100	74	29	0
Percent(20%)	100	100	100	88	100	85	46	0

n	15 < Q < 25							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	61	20	1	0	3	2	0	0
Percent(0.2%)	95	35	1	0	5	5	0	0
Percent(0.5%)	100	61	10	0	15	6	0	0
Percent(1%)	100	81	28	0	32	8	1	0
Percent(2%)	100	95	53	1	60	19	1	0
Percent(5%)	100	100	93	30	94	34	1	0
Percent(10%)	100	100	100	69	100	47	7	0
Percent(20%)	100	100	100	93	100	74	25	0

n	25 < Q < 50							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	97	97	97	97	97	97	97	97
Percent(0.1%)	66	4	0	0	2	0	0	0
Percent(0.2%)	94	13	0	0	3	0	0	0
Percent(0.5%)	100	34	0	0	7	0	0	0
Percent(1%)	100	68	4	0	10	1	0	0
Percent(2%)	100	99	37	0	38	2	0	0
Percent(5%)	100	100	94	22	77	6	0	0
Percent(10%)	100	100	100	76	97	14	0	0
Percent(20%)	100	100	100	100	100	33	1	0

Table 2.2-5a: One additional knot algorithm, $\omega_p = 10$, $R_{ogm} = 100$.

n	0 < Q < 8							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	57	53	44	2	11	13	12	1
Percent(0.2%)	81	81	60	10	25	25	23	1
Percent(0.5%)	100	100	71	24	53	54	47	3
Percent(1%)	100	100	78	37	81	83	61	9
Percent(2%)	100	100	88	49	99	98	67	18
Percent(5%)	100	100	100	61	100	100	77	38
Percent(10%)	100	100	100	78	100	100	86	56
Percent(20%)	100	100	100	96	100	100	99	57

n	8 < Q < 15							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	69	58	21	0	5	5	3	0
Percent(0.2%)	94	81	32	0	10	11	8	0
Percent(0.5%)	100	96	52	0	31	30	13	0
Percent(1%)	100	100	65	4	60	52	20	0
Percent(2%)	100	100	77	13	92	80	26	0
Percent(5%)	100	100	100	54	100	91	43	0
Percent(10%)	100	100	100	74	100	99	62	4
Percent(20%)	100	100	100	100	100	100	80	13

n	15 < Q < 25							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	98	98	98	98	98	98	98	98
Percent(0.1%)	68	41	1	0	1	4	0	0
Percent(0.2%)	100	67	2	0	7	6	0	0
Percent(0.5%)	100	84	13	0	19	11	0	0
Percent(1%)	100	97	38	0	40	28	1	0
Percent(2%)	100	100	71	0	72	41	1	0
Percent(5%)	100	100	100	35	100	65	4	0
Percent(10%)	100	100	100	87	100	87	17	0
Percent(20%)	100	100	100	100	100	100	41	0

n	25 < Q < 50							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	66	66	66	66	66	66	66	66
Percent(0.1%)	68	3	0	0	2	0	0	0
Percent(0.2%)	100	12	0	0	3	0	0	0
Percent(0.5%)	100	38	0	0	9	0	0	0
Percent(1%)	100	80	6	0	20	0	0	0
Percent(2%)	100	100	39	0	36	0	0	0
Percent(5%)	100	100	100	9	97	5	0	0
Percent(10%)	100	100	100	82	100	27	0	0
Percent(20%)	100	100	100	100	100	53	0	0

Table 2.2-5b: One additional knot algorithm, $\omega_p = 20$, $R_{ogm} = 300$.

n	0 < Q < 8							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	49	48	38	6	11	10	10	1
Percent(0.2%)	81	77	61	19	17	15	16	5
Percent(0.5%)	99	98	85	35	52	48	48	8
Percent(1%)	100	99	91	49	80	78	67	22
Percent(2%)	100	100	94	56	99	98	75	38
Percent(5%)	100	100	99	73	100	99	92	49
Percent(10%)	100	100	100	91	100	99	93	59
Percent(20%)	100	100	100	98	100	100	95	67

n	8 < Q < 15							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	82	82	82	82	82	82	82	82
Percent(0.1%)	33	26	16	0	5	1	1	0
Percent(0.2%)	90	54	26	0	7	4	1	0
Percent(0.5%)	100	74	37	0	20	16	9	0
Percent(1%)	100	88	43	0	28	24	16	0
Percent(2%)	100	98	57	4	84	52	23	0
Percent(5%)	100	100	82	37	100	66	34	0
Percent(10%)	100	100	100	62	100	83	37	0
Percent(20%)	100	100	100	91	100	99	56	1

n	15 < Q < 25							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	63	33	1	0	3	1	1	0
Percent(0.2%)	95	51	2	0	8	2	1	0
Percent(0.5%)	100	67	13	0	14	10	1	0
Percent(1%)	100	86	34	0	31	17	1	0
Percent(2%)	100	99	59	1	56	32	1	0
Percent(5%)	100	100	95	35	98	52	3	0
Percent(10%)	100	100	100	73	100	68	13	0
Percent(20%)	100	100	100	100	100	85	39	0

n	25 < Q < 50							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	97	97	97	97	97	97	97	97
Percent(0.1%)	76	9	0	0	1	1	0	0
Percent(0.2%)	95	20	0	0	3	1	0	0
Percent(0.5%)	100	44	0	0	8	4	0	0
Percent(1%)	100	71	5	0	13	5	0	0
Percent(2%)	100	100	46	0	38	7	0	0
Percent(5%)	100	100	95	22	88	10	0	0
Percent(10%)	100	100	100	76	100	25	0	0
Percent(20%)	100	100	100	100	100	47	1	0

Table 2.2-6a: Three additional knot algorithms, $\omega_p = 10$, $R_{ogm} = 100$.

n	0 < Q < 8							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	57	57	49	34	10	10	11	10
Percent(0.2%)	81	81	74	51	23	24	23	19
Percent(0.5%)	100	100	93	86	53	53	50	37
Percent(1%)	100	100	99	60	81	81	78	53
Percent(2%)	100	100	100	67	99	99	88	57
Percent(5%)	100	100	100	76	100	100	99	57
Percent(10%)	100	100	100	88	100	100	100	62
Percent(20%)	100	100	100	96	100	100	100	75

n	8 < Q < 15							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	92	66	50	1	5	4	6	0
Percent(0.2%)	93	94	67	5	10	9	10	0
Percent(0.5%)	100	100	79	12	31	29	24	0
Percent(1%)	100	100	88	28	61	61	43	0
Percent(2%)	100	100	100	52	92	93	63	5
Percent(5%)	100	100	100	66	100	100	76	10
Percent(10%)	100	100	100	78	100	100	87	22
Percent(20%)	100	100	100	95	100	100	100	48

n	15 < Q < 25							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	98	98	98	98	98	98	98	98
Percent(0.1%)	68	68	14	0	1	2	0	0
Percent(0.2%)	100	93	27	0	7	3	0	0
Percent(0.5%)	100	100	61	0	19	18	2	0
Percent(1%)	100	100	83	3	40	35	6	0
Percent(2%)	100	100	99	9	73	72	15	0
Percent(5%)	100	100	99	36	100	98	37	0
Percent(10%)	100	100	100	74	100	100	57	0
Percent(20%)	100	100	100	100	100	100	85	0

n	25 < Q < 50							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	66	66	66	66	66	66	66	66
Percent(0.1%)	67	24	0	0	2	0	0	0
Percent(0.2%)	100	48	2	0	3	0	0	0
Percent(0.5%)	100	92	20	0	8	3	0	0
Percent(1%)	100	100	47	0	15	9	0	0
Percent(2%)	100	100	74	0	39	21	0	0
Percent(5%)	100	100	91	23	98	45	0	0
Percent(10%)	100	100	100	61	100	68	3	0
Percent(20%)	100	100	100	100	100	94	26	0

Table 2.2-6b: Three additional knot algorithms, $\omega_p = 20$, $R_{ogm} = 300$.

n	0 < Q < 8							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	49	50	38	6	11	13	10	1
Percent(0.2%)	81	82	61	19	17	18	16	5
Percent(0.5%)	99	99	85	35	52	52	48	8
Percent(1%)	100	100	91	49	80	81	67	22
Percent(2%)	100	100	94	55	99	100	75	38
Percent(5%)	100	100	99	73	100	100	92	49
Percent(10%)	100	100	100	91	100	100	93	59
Percent(20%)	100	100	100	98	100	100	95	67

n	8 < Q < 15							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	82	82	82	82	82	82	82	82
Percent(0.1%)	33	32	16	0	5	2	1	0
Percent(0.2%)	90	84	26	0	7	2	1	0
Percent(0.5%)	100	94	37	0	20	17	9	0
Percent(1%)	100	100	43	0	28	26	16	0
Percent(2%)	100	100	57	4	84	72	23	0
Percent(5%)	100	100	82	37	100	94	34	0
Percent(10%)	100	100	100	62	100	99	37	0
Percent(20%)	100	100	100	91	100	100	56	1

n	15 < Q < 25							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	63	56	1	0	3	2	1	0
Percent(0.2%)	95	75	2	0	8	6	1	0
Percent(0.5%)	100	95	13	0	14	17	1	0
Percent(1%)	100	100	34	0	31	28	1	0
Percent(2%)	100	100	59	1	56	53	1	0
Percent(5%)	100	100	95	35	98	81	3	0
Percent(10%)	100	100	100	73	100	92	13	0
Percent(20%)	100	100	100	100	100	100	39	0

n	25 < Q < 50							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	97	97	97	97	97	97	97	97
Percent(0.1%)	76	9	0	0	1	1	0	0
Percent(0.2%)	95	20	0	0	3	1	0	0
Percent(0.5%)	100	44	0	0	8	4	0	0
Percent(1%)	100	71	5	0	13	5	0	0
Percent(2%)	100	100	46	0	38	7	0	0
Percent(5%)	100	100	95	22	88	10	0	0
Percent(10%)	100	100	100	76	100	25	0	0
Percent(20%)	100	100	100	100	100	46	1	0

Table 2.2-7a: Seven additional knot algorithms, $\omega_p = 10$, $R_{ogm} = 100$.

n	0 < Q < 8							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	57	57	57	48	10	12	10	10
Percent(0.2%)	81	81	80	73	24	23	25	24
Percent(0.5%)	100	100	100	93	53	53	53	54
Percent(1%)	100	100	100	98	81	81	81	72
Percent(2%)	100	100	100	100	99	99	100	86
Percent(5%)	100	100	100	100	100	100	100	94
Percent(10%)	100	100	100	100	100	100	100	97
Percent(20%)	100	100	100	100	100	100	100	100

n	8 < Q < 15							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	134	134	134	134	134	134	134	134
Percent(0.1%)	69	69	68	49	5	5	5	5
Percent(0.2%)	93	93	93	81	10	10	10	10
Percent(0.5%)	100	100	100	92	31	31	30	28
Percent(1%)	100	100	100	94	61	60	58	43
Percent(2%)	100	100	100	99	92	92	93	64
Percent(5%)	100	100	100	100	100	100	100	88
Percent(10%)	100	100	100	100	100	100	100	92
Percent(20%)	100	100	100	100	100	100	100	95

n	15 < Q < 25							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	98	98	98	98	98	98	98	98
Percent(0.1%)	68	67	67	28	2	1	8	1
Percent(0.2%)	100	100	97	57	7	7	14	1
Percent(0.5%)	100	100	100	86	19	20	24	5
Percent(1%)	100	100	100	96	39	40	41	15
Percent(2%)	100	100	100	99	73	76	65	29
Percent(5%)	100	100	100	100	100	100	99	57
Percent(10%)	100	100	100	100	100	100	100	77
Percent(20%)	100	100	100	100	100	100	100	92

n	25 < Q < 50							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	66	66	66	66	66	66	66	66
Percent(0.1%)	65	68	59	9	3	2	3	0
Percent(0.2%)	100	100	86	17	6	2	5	0
Percent(0.5%)	100	100	100	47	8	5	9	2
Percent(1%)	100	100	100	77	17	17	15	5
Percent(2%)	100	100	100	95	39	39	33	8
Percent(5%)	100	100	100	100	98	100	71	11
Percent(10%)	100	100	100	100	100	100	89	18
Percent(20%)	100	100	100	100	100	100	97	50

Table 2.2-7b: Seven additional knot algorithms, $\omega_p = 20$, $R_{ogm} = 300$.

n	$0 < Q < 8$							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	49	49	49	43	11	11	10	14
Percent(0.2%)	81	81	82	76	17	18	16	20
Percent(0.5%)	98	99	99	97	51	52	50	50
Percent(1%)	100	100	100	100	81	81	83	76
Percent(2%)	100	100	100	100	99	99	99	90
Percent(5%)	100	100	100	100	100	100	100	99
Percent(10%)	100	100	100	100	100	100	100	99
Percent(20%)	100	100	100	100	100	100	100	100

n	$8 < Q < 15$							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	82	82	82	82	82	82	82	82
Percent(0.1%)	35	34	32	29	5	4	5	4
Percent(0.2%)	90	91	89	41	6	7	7	5
Percent(0.5%)	100	100	100	73	20	20	20	22
Percent(1%)	100	100	100	87	28	29	28	29
Percent(2%)	100	100	100	95	84	83	70	43
Percent(5%)	100	100	100	100	100	100	99	63
Percent(10%)	100	100	100	100	100	100	100	76
Percent(20%)	100	100	100	100	100	100	100	90

n	$15 < Q < 25$							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	88	88	88	88	88	88	88	88
Percent(0.1%)	61	63	59	28	5	5	1	0
Percent(0.2%)	95	95	93	50	9	8	3	1
Percent(0.5%)	100	100	99	73	16	16	14	7
Percent(1%)	100	100	100	88	31	31	28	14
Percent(2%)	100	100	100	97	57	58	58	28
Percent(5%)	100	100	100	100	99	98	95	45
Percent(10%)	100	100	100	100	100	100	99	66
Percent(20%)	100	100	100	100	100	100	100	84

n	$25 < Q < 50$							
	$\omega_{3db_1}, \omega_{3db_2}$				Q			
	300	100	50	20	300	100	50	20
Total Number	97	97	97	97	97	97	97	97
Percent(0.1%)	74	76	58	13	1	2	1	0
Percent(0.2%)	94	96	81	21	4	2	1	0
Percent(0.5%)	100	100	98	52	8	9	2	1
Percent(1%)	100	100	100	86	15	13	13	4
Percent(2%)	100	100	100	99	41	38	31	8
Percent(5%)	100	100	100	100	88	88	67	12
Percent(10%)	100	100	100	100	100	100	86	23
Percent(20%)	100	100	100	100	100	100	96	43

Table 2.2-8. Summary of spline fitting algorithms for a 1% accuracy estimate of ω_{3dB_1} and ω_{3dB_2} .

Algorithm	number of data points
for equally spaced knot method	200 - 300
for one additional knot method	150 - 200
for three additional knot method	100 - 150
for seven additional knot method	30 - 50

knot algorithms are compared with those required for the other spline function algorithms in Table 2.2-8. It can also be concluded that this algorithm works even better for high Q' circuits. The reason the improvements are more significant at high Q' 's can be qualitatively explained. Since the ω_{3dB} frequencies and Q' values compared in Table 2.2-4 are essentially characteristics of the passband, those points which lie outside of the passband have only small effects on the predicted values of these parameters. For example, with a peak gain at $\omega = 1$ and with $Q = \frac{1}{2}$, most of the equally spaced points (approximately 275) lie in the passband. Thus, if $n = 300$, then there are 275 points in the passband with the equally spaced algorithm and 282 points in the passband for calculation of the second spline function with the 7 additional points algorithm. Correspondingly, if $Q = 20$, then there are approximately 7 of the uniformly spaced points in the passband with the equally spaced algorithm and 14 points in the passband with the 7 additional points algorithm. The significant improvement in the number of passband data points experienced in high Q applications should be apparent.

Based upon the premiss that the number of passband points plays a major role in determining the overall accuracy of estimating the 3dB frequencies and Q' values, there appears to be a paradox in the data of Table 2.2-4a, because, for example, with $Q = \frac{1}{2}$ and a peak gain at $\omega = 1$ we would expect to obtain an estimate of Q' and ω_{3dB1} and ω_{3dB2} much better than .5% with about 270 passband points since nearly .5% accuracy was demonstrated for about 14 points! This is actually not a paradox because the data for $0 < Q < 8$ in Table 2.2-4a was obtained by considering all structures with $Q < 8$. Were the first table limited to $Q < 1$, a dramatic improvement in accuracy for the equally spaced knot algorithms would have been observed due to the very high number of passband data points and minimal improvements would have been observed with the remaining three algorithms.

If 300 initial sample points are used, 0.5% accuracy appears attainable for the high Q circuits. It may well be the case that even further improvements in accuracy are attainable with other modest modifications of the spline fitting algorithm. Since our goal has been to obtain frequency control in the 1% range, and since it appears that the existing spline algorithms are capable of this, additional investigations at improving the spline fitting algorithm have not been made at this point in time.

Comments about the performance of these spline function algorithms as a function of the number of points in the algorithm deserves attention. The simulations summarized in Table 2.2-7 were based upon the assumption that the sample points were uniformly (linearly) spaced on the normalized interval from 0 to 2. In practice, we would expect deviation from our design center by at most $\pm 50\%$. This would effectively reduce the normalized interval over which sample points need be taken to $[+.5, 1.5]$ which effectively reduces the required number of sample points by a factor of 2 below what was used in the simulations of Table 2.2-7. The question of using linear or logarithmic spaced samples deserves mention. Since the logarithmic frequency axis is often of more interest than the linear frequency axis, it would make more sense to consider uniformly spaced samples on

a logarithmic axis. Defining the logarithmic frequency variable by h where

$$h = \log \omega$$

it follows that the normalized linear domain defined by $\omega \in [.5, 1.5]$ maps to the normalized logarithmic domain defined approximately by $h \in [-.3, .2]$. It is conjectured that a reduction in the number of sample points required for a given degree of accuracy can be obtained by using the uniform logarithmic point spacing. The question of whether the spline fit is made in terms of the ω variable or h variable also deserves attention. It is also conjectured that a polynomial spline fit in the h variable rather than the ω variable may offer improvements in accuracy. Neither of these conjectures have been substantiated at this point in time.

Another method of reducing the number of sample points while still maintaining a given degree of accuracy deserves mention. The equal spaced knot algorithm was based upon the assumption that all sample points were made a-priori and that the spline function was calculated based upon these a-priori measurements. The three extensions discussed above were based upon the assumption that a few additional sample points could be added through a second series of a small number of additional measurements near the passband predicted by the first set of measurements. Although all sample points from both sets of measurements were used in the second spline function calculation, the affects of all except for a few of the original points in the neighborhood of the passband on the estimates of ω_{3dB} and Q' were negligible. Since very few of the original sample points affect the estimates of ω_{3dB} and Q' for narrow bandwidth systems, a significant reduction of the number of required sample points can be obtained in high Q applications if a much coarser grid is used initially since the first spline function fit essentially only serves to locate the actual passband from which additional samples will be made. If sufficient resolution on the magnitude measurement circuit exists, a very small number of samples is needed to locate the passband. Unfortunately, for narrow-band systems, the magnitude of the transfer function may be so low in the stopband so as to cause practical limitations in accurately making gain measurements; in fact, it may well be the case that the magnitude at many sample points in the stopband is less than 1 l.s.b. of the A/D converter in the magnitude measurement system. This problem can be circumvented if we require at least one sample point lie in the nominal passband. If the normalized desired system bandwidth is BW_n , then the number of sample points needed to nominally obtain one sample point in the passband for the linearly spaced samples in the interval $[.5, 1.5]$ is given by

$$n_1 = \frac{1.5 - .5}{BW_n} = \frac{1}{BW_n} \quad (2.2 - 26)$$

With a bandpass system which is nominally second-order, the pole Q is the reciprocal of the bandwidth. Thus the number of sample points needed is

$$n_1 = Q \quad (2.2 - 27)$$

If the 7 additional knot algorithm is used, it is conjectured that approximately $Q + 7$ total data points are needed to obtain accuracies in ω_{3dB1} and ω_{3dB2} to about .5% using the two spline approach.

Significant reductions in spline function computation time can also be achieved. The computation time required for a spline function fit to a large number points can be approximated by

$$t = \alpha N \quad (2.2 - 28)$$

where N is the number of data points and α is a constant independent of N . The computation time reduction potential is based upon the premiss that a spline function fit to the data points in the passband plus one or two data points adjacent to the passband will differ very little, in the passband, from a spline function fit through all of the data points. With this premiss, it can be observed that the algorithm used to generate the data in Table 2.2-7a for $n = 300$ required fitting one spline through 300 points and a second spline through 307 points. Thus the time required for spline calculations can be approximated by $t \cong (607)\alpha$. Nearly the same accuracy would have been obtained if the second spline function were restricted to passband data points plus, say two, points adjacent to the passband on each side. For example, if $Q = 20$, it follows from the previous example that there are approximately 14 passband points with the four additional adjacent points the time required for calculating the second spline is reduced to $t_2 \cong 18\alpha$ and the total computational time for the 300 point algorithm becomes 318α which is nearly a 50% reduction over what was required for calculating the two spline functions with a large number of points. If the number of sample points for the first spline calculation is now reduced to $n_1 = Q$, it follows that the 7 additional point algorithm will require a total spline computation time of

$$t = \alpha Q + (7 + 21 + 2)\alpha \quad (2.2 - 29)$$

For $Q = 20$, $t = 31\alpha$ which is about 5% of what was required previously to obtain nearly the same accuracy in estimating ω_{3dB1} and ω_{3dB2} .

2.2.2 Data Collection Hardware

The measurement system can be subdivided into three separate hardware subsystems: excitation, frequency counter and gain/phase Performance Detector subsystems. The remainder of this section will discuss each of these hardware subsystems, their architectures and design details of specific implementations.

2.2.2.1 Excitation system.

This subsystem provides the analog signal processor with a sinusoidal input waveform of a specified frequency and amplitude needed during the calibration phase. The proposed architecture is based upon a voltage controlled oscillator (VCO) as shown in Fig. 2.2-7. Two digital words (D_{freq} and D_{amp}) are supplied by the performance measurement controller. D_{freq} is converted by a n -bit DAC (typically a logarithmic DAC) to a control voltage (V_f), which is used to control the frequency of oscillation of the VCO. Similarly, the digital word D_{amp} is converted to a control voltage V_a which is a reference signal for an automatic gain control (AGC) circuit. The output of the VCO, v_{exc} , should be of the

form,

$$v_{exc} = V_m \sin(\omega(t).) \quad (2.2 - 30)$$

where V_m and ω are a function of D_{amp} and D_{freq} , respectively.

The basic specifications for this subsystem are as follows:

- (1) The frequency range should cover the current CSP control range and extend well below and above the passband for all realizable filters within this range. For DCASP-2, the required range is approximately from 500Hz to 5MHz.
- (2) The resolution of the frequency control should be set at a fixed percent change of the current frequency, dictated by the maximum number of samples required in the passband at the highest Q , (i.e., $\frac{100\%}{Q_{max}N}$ where N is the number of samples in the passband). For DCASP-2, and the current SPLINE fitting algorithm needed for attaining absolute accuracy in the .5% to 1% range, this value is around .2%.
- (3) The range of V_m should satisfy the expression, $\frac{V_{max}}{H_{max}} \leq V_m \leq V_{max}$, where V_{max} is the maximum signal swing permissible at the filter input or output and H_{max} is the maximum gain over the operating frequency range of the filter (assuming that there is no peaking at any internal nodes to the CSP), thus preventing the output signal from being distorted because of too large an output signal swing, or too noisy because of too small an output signal swing.

In light of global processing variations, it may be necessary to calibrate the frequency control of the excitation subsystem in order to meet the above specifications, which is easily provided for by the current DCASP architecture.

Currently, no excitation system has been implemented in CMOS, since this circuit design was not expected to limit the overall capabilities and performance of the DCASP architecture under investigation. An HP 3325A programmable synthesizer/function generator is currently being used in its absence. This instrument easily meets the aforementioned specifications and is readily interfaced to the tuning host discussed in Section 2.4 of this document.

2.2.2.2 Frequency measurement system.

This subsystem measures the fundamental frequency of the excitation waveform, thus providing the ordinal values of the transfer function frequency response.

A basic description of the architecture of a frequency counter subsystem is shown in Fig. 2.2-8. This system has two analog inputs, f_{ref} and f_{unk} . f_{ref} is an externally provided reference frequency waveform, while f_{unk} is the "unknown" sinusoidal waveform of unknown frequency. The outputs are two n-bit digital words, D_{ref} and D_{unk} , which are supplied to the performance measurement controller for post-processing. The internal

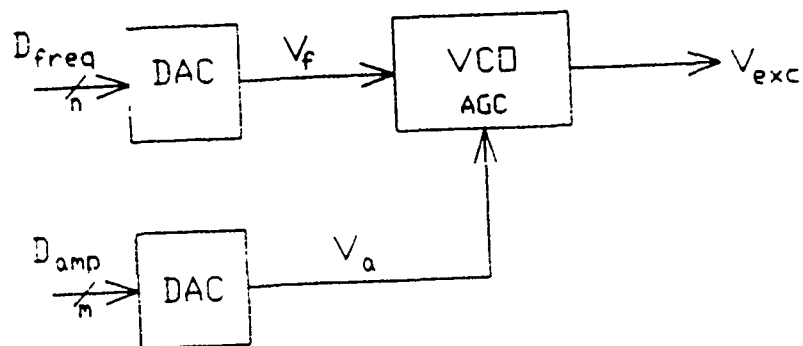


Fig. 2.2-7. Block diagram of typical excitation hardware system.

hardware consists of a zero crossing comparator with hysteresis that drives a digital counter's clock input. Thus counting the number of periods of the unknown input waveform that occurs in a fixed time interval; the period and frequency of the unknown input waveform can be estimated. The digital control signals *clear* and *latch* are used to start and stop the counting process, and thus control the conversion time interval. The hysteresis in the high-speed comparators compensate for harmonic distortion and noise that may be present on the input waveform.

The basic concept illustrated here is that the number of periods in a fixed time interval is proportional to the frequency of the waveform. This can be expressed mathematically as

$$N = \frac{\int_{t_1}^{t_2} |\sin(2\pi ft + \theta)| dt}{\int_0^T |\sin(2\pi ft + \theta)| dt}, \quad (2.2 - 31)$$

where N is the number of periods in the interval $t \in [t_1, t_2]$.

The quantization effects of the actual hardware system can be expressed as $N_x - 1 \leq D_x \leq N_x + 1$ for $x \in (ref, unk)$, where D_x (corresponding to the physical output word of the hardware system) is the quantized or measured value of N_x (the exact or theoretical number of periods). Now, based upon the proportionality between frequency and the number of periods in a fixed interval, the unknown frequency, f_{unk} can be expressed as

$$f_{unk} = f_{ref} \frac{D_{unk}}{D_{ref}}. \quad (2.2 - 32)$$

The overall error induced in f_{unk} , assuming a LSB error in both D_{ref} and D_{unk} and based upon a worst case sensitivity analysis on eq. (2.2-32), is:

$$\frac{\Delta f_{unk}}{f_{unk}} \approx \frac{1}{D_{unk}} \left(1 + \frac{f_{unk}}{f_{ref}} \right) \quad (2.2 - 33)$$

Thus for a specific value f_{unk} and f_{ref} , the length of the measurement time interval can be determined for a desired accuracy. Also, the overall accuracy of the frequency counter for a fixed time interval can be enhanced by increasing the reference frequency as limited by the speed of the physical hardware. For $f_{ref} \gg f_{unk}$, the width m of the digital word D_{unk} determines the overall percent accuracy of the frequency counter, as expressed in eq. (2.2-34).

$$m \approx -\log_2 \left(\frac{\Delta f_{unk}}{f_{unk}} \right) \quad (2.2 - 34)$$

This also implies that the digital counter associated with D_{unk} can be used to indicate when a certain desired accuracy has been obtained and thus automatically terminate the conversion process. The width n of the digital word D_{ref} is a function of the minimum unknown frequency and the corresponding digital word width m . Assuming that the end-of-conversion (EOC) is triggered by the saturation of the "unknown" counter, then

$$n \approx m + \log_2 \left(\frac{f_{ref}}{f_{unk}} \right). \quad (2.2 - 35)$$

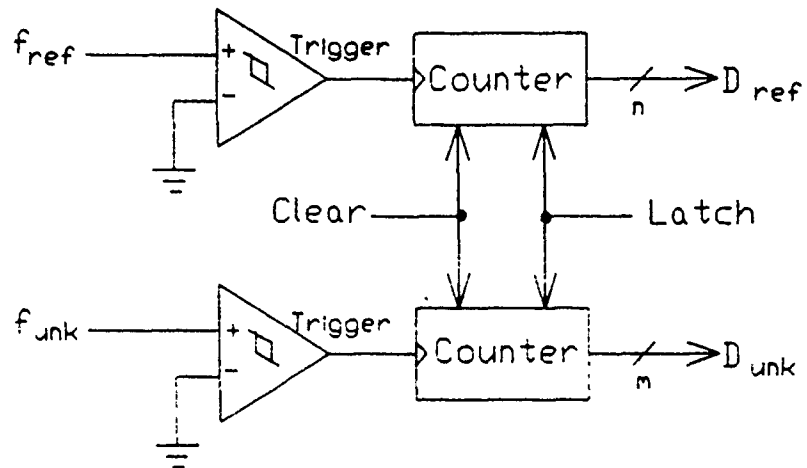


Fig. 2.2-8. Frequency counter hardware schematic.

The design presented here, is simple and straight forward and unlimited in obtainable accuracy. Since the DCASP architecture currently under investigation is not limited in performance nor capabilities by the specifics of the frequency counter implementation, the frequency counter subsystem has not been fabricated in CMOS technology. Rather a HP 5316A 100MHz Universal Counter has been substituted in the absence of an integrated version of this circuit.

2.2.2.3 Gain/Phase Measurement System.

The discrete time sampling algorithm discussed in Sec. 2.2.2.1 of this report was based upon the assumption that samples of the waveform at discrete points in time are available. Since tedious arithmetic based upon the values of these samples is required to extract gain and phase information, it is most expedient to implement these operations with the digital controller. The most straightforward way to approach this problem thus involves building a high speed clocked A/D converter. High speed A/D converter design with good accuracy and resolution is challenging. An acceptable alternative is to build a fast sample and hold and a slower speed A/D converter. This significantly relaxes the A/D converter design specifications and simplifies the A/D converter design problem thus reducing the cost associated with implementing the A/D converter. Furthermore, with the latter approach, a single A/D can service several sample and holds thus further reducing system design costs and guaranteeing inherent channel to channel matching of the A/D conversion process. This channel to channel matching possibility has farther reaching implications. Since gain measurements will be made based upon the excitation and response samples, any nonideal factors which linearly affect the input and output in identical ways will have minimal impact on system gain calculations. Thus, architectures which have inherent channel to channel matching in the data converters and/or sample and hold circuits should offer potential for improved performance. The difficulty of this approach is that stringent and challenging specifications must be placed on the design of these sample and holds (S/H's), for high frequency applications requiring high precision and high speed sampling.

The discrete time sampling algorithm of Sec. 2.2.2.1 requires simultaneous sampling of the excitation and response waveforms. This can be achieved with two phase-coherent sample and hold circuits, as shown in Fig. 2.2-9. These circuits share the sample control line. The resulting sample and held output voltages (V_o/Exc and $V_o/Resp$) are made available for conversion to digital words by a subsequent A/D(s) which is (are) not included in the figure.

Such sample and holds are often designed to operate in two modes, the track-mode and the hold-mode in which a holding capacitor is used to hold the sampled waveform. In track-mode the voltage drop across the holding capacitor tracks the input voltage. In the hold-mode, the charge on the hold capacitor is electrically isolated from the input signal and the voltage drop across the low-loss capacitor is buffered and supplied to the output, as the sampled signal. The transition from the track mode to the hold mode is referred to

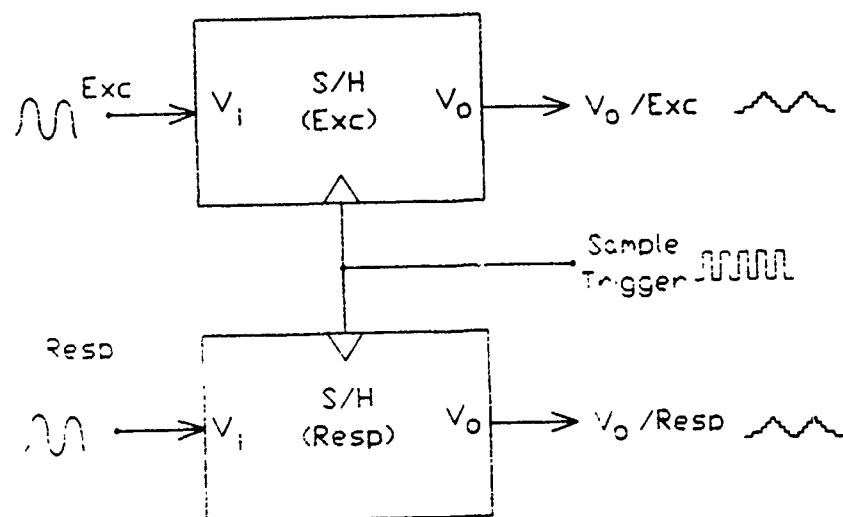


Fig. 2.2-9. Block diagram of a two phase-coherent S/H circuit.

as sampling.

Performance Limitations:

Three different Sample and Hold circuits have been investigated. Before the performance limitations of the Sample/Hold circuits can be properly addressed, the term *performance* should be defined in this specific context. Several parameters which are useful for characterizing the performance of Sample and Hold circuits follow:

Channel-to-Channel Aperture Jitter (Δt_{ap}) — Aperture Time is qualitatively defined as the time between the inception of the sample trigger and the instant the voltage drop across the hold capacitor ceases to track the input signal. This instant shall be referred to as the sampling time t_s . The channel to channel variation in the aperture times will be termed aperture jitter.

Channel-to-Channel Gain Variation ($\Delta H_{s/h}$) — The variation in the Gain between matched channels of the Performance Detector over a specific frequency range and voltage range. The Gain specified in dB is defined as the linear voltage gain between the input signal and the sample and held output signal. Ideally the gain should be $0dB$.

Differential Nonlinearity (DNL) — The maximum deviation from an ideal straight line drawn between the maximum and minimum sample and held output voltage over the intended range of input signals, as a function of the input frequency. This quantity is expressed as a percentage of the full scale (FS) analog voltage range. This error term is independent of gain error and offset error.

Droop Rate (dV_o/dt) — Droop rate is the rate of change in the sample and held output voltage while the circuit is in hold-mode. dV_o/dt is a direct function of the leakage current associated with the hold capacitor and the size of the holding capacitor.

Hold Mode Settling Time (t_{hm}) — This is the time for the sampled and held output signal to settle to within a specified error band, measured from the rising edge of the sample and hold line. This is a function of the external load capacitance placed on the output. This time factor is the minimum amount of time that should be allocated between requesting a sample and instigating the A/D conversion process.

Offset Voltage (V_{os}) — This is the DC sample and held output voltage associated with sampling the input signal with the input grounded. This component includes clock (*sample*) feedthrough and any offset associated with buffering the sample and held output signal.

Power Supply Rejection Ratio ($PSRR$) — The AC voltage gain between an AC voltage source in series with the DC power supply voltages (V_{DD} and V_{SS}) and the output voltage V_o for the S/H operating in both track- and hold-modes. $PSRR$ is measured in dB as a function of frequency.

Note that the Aperture Time and Gain are not specified here because the Sampling Algorithm eliminates these errors, assuming the two channels are matched. Furthermore since matching of the adjacent S/H is suspected to be fairly good, the channel-to-channel type variations should not be especially taxing. Also, the DC offset voltage is not particularly challenging because its effect can easily be cancelled in the discrete time Sampling Algorithm. The differential nonlinearity is expected to be the most challenging of the specifications listed above, especially when subjected to large-amplitude high-frequency signals.

The problem of analyzing the inherent performance limitations of each of the S/H architectures has been broken down into three separate categories:

- (1) Track-Mode performance limitations — those factors that limit the ability of the S/H circuitry to accurately track the response input signal relative to its ability to track the excitation input signal; and how these inaccuracies relate to the overall inaccuracy of the so called "sampling".
- (2) Sampling-Transition performance limitations — those inaccuracies in the overall "sampling" induced by the transition between tracking the input signal and holding the resultant analog voltage on a hold capacitor.
- (3) Hold-Mode performance limitations — those limitations that cause the resulting held analog voltage to deviate from its ideal value.

Errors in each of these categories must then be related to the overall error in so called "sampling" the excitation and response signals. These errors induce errors in the computed gain and phase measurements of the Performance Measurement System.

Before each of these architectures are discussed, common problems or non-idealities that plague each of these S/H designs will first be characterized and then modeled. Primarily this discussion will focus on the analog switch since it (1) is common to all S/H designs and (2) contributes heavily to the overall differential nonlinearity and other performance limitations of the S/H's.

After the analog switch has been discussed, three S/H architectures will be described. This section is concluded with a discussion of the design of an operational amplifier which is central to all of the S/H architectures.

2.2.2.3a Sample and Hold for Data Conversion

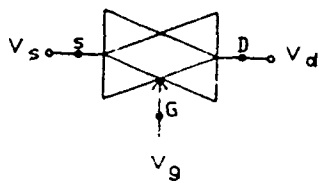
2.2.2.3a1 Analog Switch

In the S/H application the purpose of the analog switch, shown in Fig. 2.2-10, is to provide a short circuit between the source node V_s and the drain node V_d when the switch

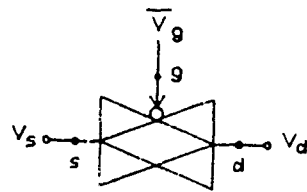
is on, provide an open circuit when the switch is "off", and rapidly switch between the "on" and "off" states when the control line V_g changes from a logical "1" (+5V) to a "0" state (-5V). In actuality the analog switch deviates greatly from this ideal performance with the following symptoms:

- (1) When the analog switch is turned on, it exhibits two undesirable characteristics:
 - (a) It has a finite on-resistance meaning that there is some finite voltage drop across the switch that increases as the current through the switch increases.
 - (b) This on-resistance is dependent upon the DC potential of the source/drain nodes, thus inducing signal dependent nonlinearities into the host circuit. The non-zero on impedance manifests itself in delays and a frequency dependent gain function when the switch is used in high speed sample and hold circuits. These effects are dominantly linear. The voltage-dependent nonlinearities in the switch on impedance cause distortion in the sample and hold. These latter effects cause major concern if the distortion becomes very large.
- (2) Each of the pass-transistors of the analog switches have a parasitic capacitor between the source/drain node and the gate. This capacitor weakly couples the control signal driving the gates into the signal path of the analog switch, resulting in the two following characteristics:
 - (a) It injects charge into the source and drain nodes of these devices when it is turned "off". This is commonly referred to as *clock feedthrough*.
 - (b) It injects power supply noise into the source and drain nodes even while these devices are "off".
- (3) The reverse biased junctions of the n^+ and p^+ diffusions associated with the source and drain nodes of the pass-transistors of the analog switches contribute to two parasitic effects:
 - (a) A parasitic diffusion capacitor is produced between the source/drain nodes and the bulk/well. Furthermore, these parasitic capacitances are a function of the DC voltage across the capacitor. These nonlinear parasitics induce undesirable nonlinearities into circuits containing these components.
 - (b) The source/drain diffusions exhibits a reverse bias leakage current, thus implying that the source/drain nodes of the analog switch are not electrically isolated when the switch is "off".

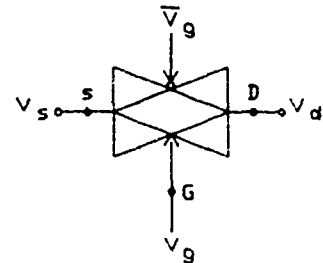
Each of these nonidealities are discussed below, after the different analog switch architectures are presented.



(a) positive-true
logic

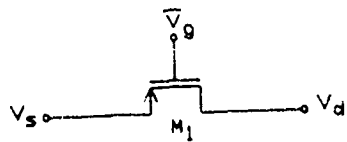


(b) negative-true
logic

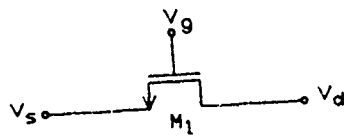


(c) complimentary
logic

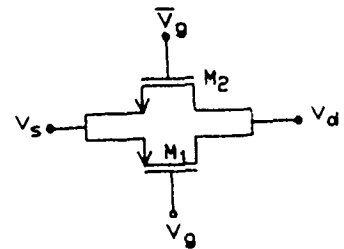
Fig. 2.2-10. Analog switch symbols.



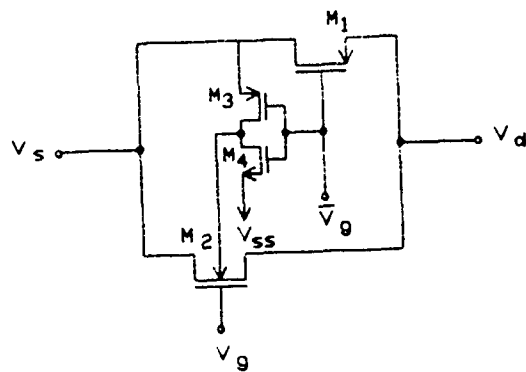
(a) p-channel



(b) n-channel



(c) complimentary



(d) floating well complimentary

Fig. 2.2-11. Analog switch circuit schematics.

Description:

There are four types of analog switches that are currently under investigation, as shown in Fig. 2.2-11. The first two switches are the simple n-channel and p-channel devices. These devices have a limited operating voltage range, since the devices have a tendency to turn "off" with large input signal. The turning off of the switches is due to threshold voltage limitations caused by decreasing the excess bias on the G-S terminals with increasing signal swings. The threshold voltage itself is also signal dependent due to bulk (γ) effects. γ effects become more problematic as the reverse bias between the bulk/source p/n junction is increased. This increase in reverse bias increases the size of the depletion region surrounding this junction and reduces the majority carriers in the channel. Quantitatively, in a typical CMOS process, this modulation of V_T varies between 0.8V and 2.5V as V_{BS} voltages range between 3V and 7V, as is typical for our input signal swing of $\pm 2V$. Here the term "on" refers to the device being biased in the active or triode region, so that the channel is characterized by the presence of a strong inversion layer. The device is referred to as "off", when the device is biased in cutoff, where the channel is void of majority carriers. The other bias regions such as weak-inversion and saturation are undesirable states, since the device has a much larger "on-resistance" in these states, yet not large enough to be considered "off". Quantitatively, consider a circuit biased with ± 5 volt supplies with an input signal of $+2V$ placed on the source node of an n-channel MOSFET with a zero bias threshold voltage of .9V gated on with $+5V$ applied to the gate. This results in a $V_{BS} = -7V$ and thus for $\gamma = .3V^{1/2}$, $V_T \approx 2.5V$. This results in a $V_{GS} - V_T \approx 0.5V$, which would be considered barely "on", especially if V_{DS} was non-zero. This will be illustrated later in the discussion of on-resistance nonlinearities. Similar problems are experienced with single p-channel switches when the input signals become negative.

This soft turn-on problem is typically addressed by using the complimentary analog switch shown in Fig. 2.2-11c. This switch has the characteristics that as V_i swings positive, the n-channel transistor M_1 starts to turn "off", but the p-channel device M_2 counteracts this effect by turning "on" even stronger. Similarly as the V_i swings negative the n-channel MOSFET compensates for the p-channel transistor. The price paid for the complimentary signal is both the area required for the second transistor and, more importantly, the necessity of generating and bussing the complimentary clock signals.

The last analog switch under consideration is referred to as the "floating-well complimentary analog switch", as shown in Fig. 2.2-11d. This switch attempts to take advantage of the p-well process by tying the p-well of M_2 to V_i when the switch is "on" and to V_{SS} when "off". Thus the bulk effect of M_2 is completely eliminated when the device is on. One criterion for a floating-well type architecture to operate properly, is that the n^+ diffusion and p-well junctions associated with M_2 must remain reversed biased at all times. Thus when the transistor is "off" the p-well is dropped to the lowest potential in the circuit. Furthermore when the transistor is "on", it is assumed that V_d is one diode drop above V_i . This assumption will restrict how much current can be pulled through the device, and thus limit its application. Lastly, when the switch is turned "off", there is a time delay

between the analog switch turning "off" and the p-well being discharged down to V_{SS} . This time delay should be of no consequence as long V_d does not change drastically in this time period, as is expected in most S/H applications. Note also the dynamic p-well biasing circuitry does not affect the time required to turn the analog switch "off", except for a slight increase in the load capacitance seen on the \bar{V}_q node.

Voltage Dependent "On-Resistance" Nonlinearities:

As mentioned above, when the analog switch is turned "on", and current is being conducted by the switch, a voltage drop across the switch V_{DS} is produced. This implies a finite on-resistance. The term "on-resistance" normally implies that there exists a linear relationship between the conduction current and the associated voltage drop across the analog switch. Unfortunately, this is not the case. First of all, the analog switch is not a two terminal device, but rather is a two port device (as shown in Fig. 2.2-12a), in which there exists some family of nonlinear I-V curves that can be characterized by small-signal linearized two port parameters as a function of the DC quiescent two port parameters V_D , V_S , I_D and I_S . Equivalently the two-port system can be represented as shown in Fig. 2.2-12b, where $V_{DS} \stackrel{\text{def}}{=} V_D - V_S$ and $I_S = I_{S1} + I_{S2}$. If we neglect leakage currents, ($I_{S2} = 0$) and assume that $I_D = I_S$ then the small-signal linearized on-resistance r_{on} can be defined as

$$r_{on} \stackrel{\text{def}}{=} \frac{\delta V_{DS}}{\delta I_D} \quad (2.2 - 36)$$

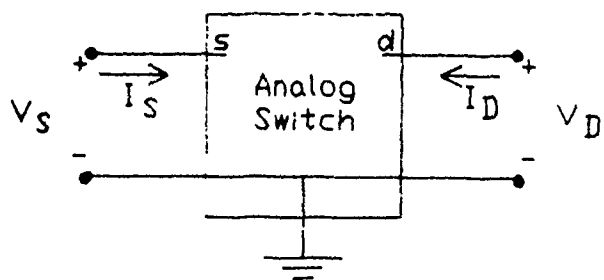
r_{on} is a function of the bias point V_{DS} and V_S . With this formulation, it is assumed that r_{on} is frequency independent. Since the intended use of this model as driven by the S/H application is ideally based upon the assumption that there is little to no voltage drop across the device when the switch is in the "on" state, we shall assume that the DC component of V_{DS} satisfies the relation $V_{DS} \approx 0$. This simplifies the model and reduces the on-resistance to being a function of a single DC potential, V_S .

N- and P-Channel Analog Switches

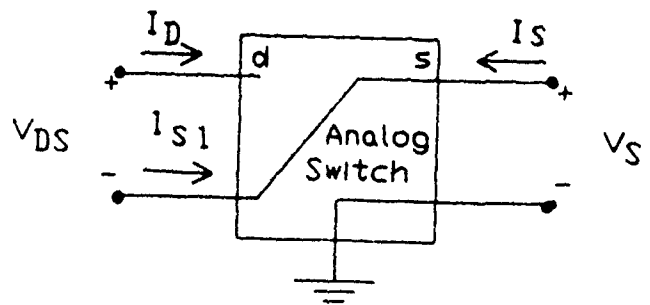
First the n-channel and p-channel pass-transistor analog switches will be study with the intent of accurately characterizing the nonlinear on-resistance characteristics. After this has been completed, then the complimentary and floating-well analog switches will be be studied, since these complex devices are composed of simple pass-transistors.

Hand Calculations

Mathematically the expression for r_{on} for the single n-channel and p-channel analog switches can be derived easily from Sah's equation.



(a) Normal



(b) Equivalent

Fig. 2.2-12. Two port representation of an analog switch.

Sah's Equation:

$$I_{D_n} = \beta_n \left(V_{GS} - V_{T_{on}} - \gamma_n \left(\sqrt{\psi + V_{BS}} - \sqrt{\psi} \right) - \frac{V_{DS}}{2} \right) V_{DS} (1 + \lambda V_{DS}) \quad (2.2-37a)$$

where

$$\beta_n = K_n \frac{W}{L} \quad (2.2-37b)$$

Thus if we assume the following definitions for on-resistance r_{on} and on-conductance g_n :

$$g_n = \frac{1}{r_{on_n}} \stackrel{\text{def}}{=} \left. \frac{\delta I_D}{\delta V_{DS}} \right|_{V_{DS}=0} \quad (2.2-38)$$

Thus from equations (2.2-37a,b), we find

$$g_n = \beta_n \left(V_{GS} - V_{T_{on}} - \gamma_n \left(\sqrt{\psi + V_{BS}} - \sqrt{\psi} \right) \right). \quad (2.2-39)$$

For a system with $\pm 5V$ power supplies this equation becomes

$$g_n = \beta_n \left(5 - V_S - V_{T_{on}} - \gamma_n \left(\sqrt{\psi + V_S + 5} - \sqrt{\psi} \right) \right) \quad \text{for } V_{T_{on}}, \gamma_n > 0. \quad (2.2-40a)$$

Similarly for a p-channel pass-transistor

$$g_p = \beta_p \left(5 + V_S - V_{T_{op}} - \gamma_p \left(\sqrt{\psi - V_S + 5} - \sqrt{\psi} \right) \right) \quad \text{for } V_{T_{op}}, \gamma_p > 0. \quad (2.2-40b)$$

If γ_n and γ_p are assumed constant, the expressions for g_n and g_p are quite simple. γ is actually dependent upon the value of V_{BS} since the depletion region around the source will modulate the channel length. A more exact value of " γ " is given by γ' defined by (for $V_{DS} \approx 0$).

$$\gamma'_n = \gamma_n (1 - \alpha_{S_n} - \alpha_{D_n}) = \gamma_n (1 - 2\alpha_{S_n}) \quad (2.2-41a)$$

where

$$\alpha_{S_n} = \frac{1}{2} \frac{X_J}{L} \left[\sqrt{1 - 2 \frac{w_{S_n}}{X_J}} - 1 \right] \quad (2.2-41b)$$

$$w_{S_n} = X_{D_n} \sqrt{2\phi_F - V_{BS}} = X_{D_n} \sqrt{2\phi_F + 5 - V_S} \quad (2.2-41c)$$

$$X_{D_n} = \sqrt{\frac{2\epsilon_{si}}{qN_{sub_n}}} \quad (2.2-41d)$$

Similarly,

$$\gamma'_p = \gamma_p (1 - 2\alpha_{S_p}) \quad (2.2-42a)$$

$$\alpha_{S_p} = \frac{1}{2} \frac{X_J}{L} \left[\sqrt{1 - 2 \frac{w_{S_p}}{X_J}} - 1 \right] \quad (2.2-42b)$$

$$w_{S_p} = X_{D_p} \sqrt{2\phi_F + 5 + V_S} \quad (2.2-42c)$$

$$X_{D_p} = \sqrt{\frac{2\epsilon_{si}}{qN_{sub_p}}} \quad (2.2-42d)$$

More details about this formulation can be found in [19]. The physical constants referred to in equations (2.2-37a,b) through (2.2-42a-d) are contained in Table 2.2-9a. Also the MOSIS recommended analog processing parameters for these same equations are contained in Table 2.2-9b.

Table 2.2-9a. Physical constants.

Constant	Value	Units
ϵ_o	$8.85418E - 12$	F/m
ϵ_{si}	$11.7 \times \epsilon_o$	F/m
q	$1.60218E - 19$	C

Table 2.2-9b. Process parameters.

Parameter	Value		Units
	n - channel	p - channel	
K	$3.286649E - 05$	$1.526452E - 05$	A/V^2
N_{sub}	$1.00E + 16$	$1.121088E + 14$	$1/cm^3$
V_{t_o}	0.827125	-0.894654	V
γ	1.35960	0.879003	$V^{1/2}$
ϕ_F	0.6	0.6	V
X_J	0.40μ	0.40μ	m
λ	$1.604983E - 02$	$4.708659E - 02$	$1/V$

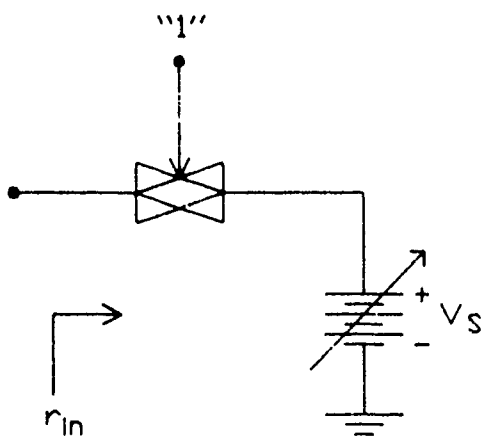
Unfortunately, the model parameters contained in Table 2.2-9b are not consistent with the accepted device physics of the MOSFET, thus the results from this analysis are somewhat subjective. This anomaly stems from the basic extraction algorithm MOSIS uses to come up with these so called "nominal analog process parameters". This extraction algorithm uses the standard parameter extraction technique of taking physical I-V measurements of various fabricated test vehicles and then by fitting the experimental data to a device model via a standard curve fitting algorithm, the parameters of the device model can be extracted. Unfortunately, the developers of this parameter extraction system, knowingly used a subset of the level 2 SPICE model parameters. Secondly, they did not constrain these parameters to be self-consistent or consistent with fundamental solid-state physics. Thirdly, the power supplies they used in their extraction system were most likely 0 to 5V, not $\pm 5V$. Lastly, their test vehicle and the associated measurements were not focused on modelling the nonlinear characteristics of the MOSFET nor extracting reasonable γ or N_{sub} SPICE parameters.

Conceptually, the S/H designer can minimize the effect of these nonidealities of the "on resistance" by minimizing the on-resistance. This can be achieved by making the channel lengths of the pass-transistors minimum length. Making the devices minimum length introduces troublesome short-channel effects. The hand-analysis shown above does not attempt to incorporate all of the short channel affects that typically plagues IC designers. A more detailed analysis of these switches using the circuit simulator SPICE follows.

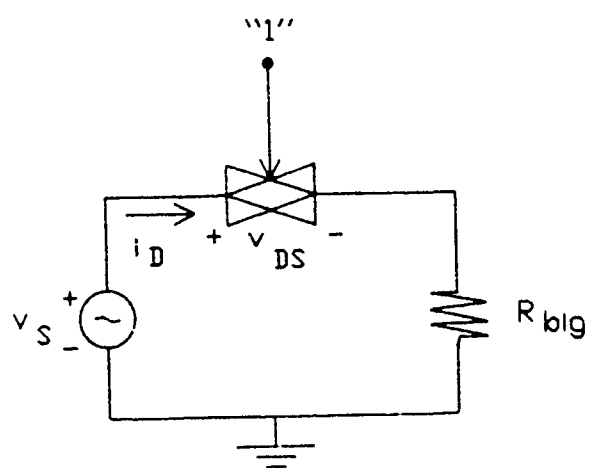
SPICE Analysis of n- and p-Channel Switches

With SPICE, the small-signal equivalent resistance can be computed by cascading the analog switch with a ideal independent voltage source V_S , and then performing a transfer function analysis on this network for various values of V_S , as shown in Fig. 2.2-13a. In this analysis SPICE first determines the DC operating point for the circuit and then computes the small-signal model parameters for each of the MOSFET's. From this small-signal model then the input resistance (on-resistance) and other two port characteristics can be computed.

An alternative analysis technique is to cascade the analog switch with a linear resistor R_{big} of value approximately $10\times$ the expected on-resistance of the analog switch, as shown in Fig. 2.2-13b. This will allow the switch S_s to both float up and down as a function of the instantaneous voltage v_S , thus modulating the bulk effect of each of the pass-transistors. Furthermore, the resistor R_{big} limits the voltage drop across the switch and closely models the typical RC type relationship present in the S/H architectures, without the phase shifting or frequency dependent components. Thus, if we excite this system with a large-amplitude ($\pm 2V$) low-frequency (1kHz) sinusoid, the instantaneous voltage drop across the switch v_{DS} and the instantaneous current through the switch i_D can be simulated from SPICE. The effective instantaneous on-resistance can be computed from the ratio $r_{on} = v_{DS}/i_D$. Though this is not exactly equivalent to the small-signal analysis technique, the results are expected to be comparable. Note: this second technique has numerical



(a) transfer function



(b) transient

Fig. 2.2-13. SPICE analysis test setup to measure effective on-resistance of an analog switch.

resolution problems near $v_S = 0V$, since at this value both the current i_D and voltage drop v_{DS} approach zero. This problem can be solved by applying a DC offset voltage to the base of R_{biq} and thus moving the discontinuity to a location out of the range of interest.

The graph shown in Fig. 2.2-14 compares the three equivalent on-resistances:

- (1) **Theoretical** — The small-signal on-resistance computed from theoretical hand-calculations, shown in Eqs. (2.2-40) through (2.2-42).
- (2) **Linearized** — The small-signal linearized on-resistance simulated by a small-signal SPICE analysis or transfer function characterization technique.
- (3) **Instantaneous** — The instantaneous on-resistance simulated by a large-signal SPICE transient-analysis.

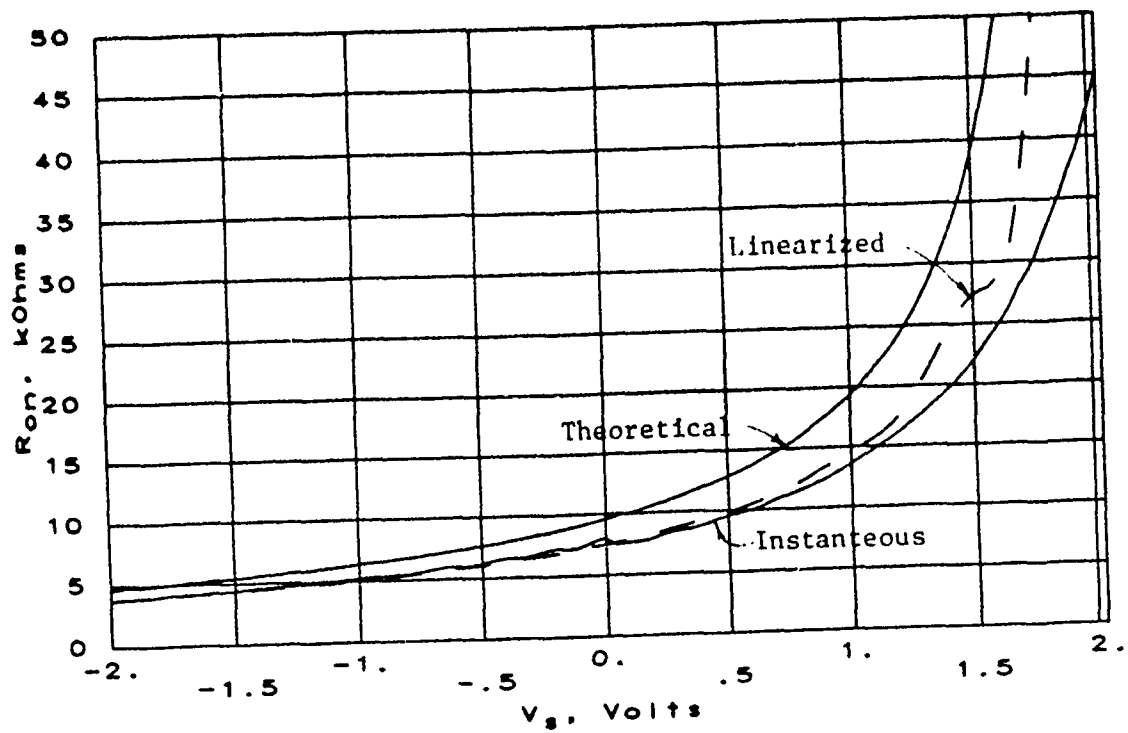
More specifically the plots shown in Figs. 2.2-14a and 2.2-14b are plots of the effective on-resistance of a single n-channel and p-channel pass-transistors with $L = 3\mu m$ and $W = 4\mu m$, as a function of the bias voltage V_S , with a $\pm 5V$ power supply and the gate voltage at the appropriate rail. The SPICE parameters used in these simulations are shown in Appendix-A.

The two SPICE simulation techniques agreed quite well with each other for the pass-transistors biased in the active region, but once the devices started turning "off" or entering weak-inversion, the two curves started separating some, since the large signal simulation allowed the v_{DS} to be non-zero and the small-signal simulation did not. Furthermore the modeling of the weak-inversion region of MOS devices is poorly implemented in earlier versions of SPICE. This variation was expected. Lastly, the simulation near the edges where the bulk-effect dominates the circuit performance is not expected to be accurately depicted in Fig. 2.2-14, since the SPICE parameters $NSUB$ and $GAMMA$ are suspected to be grossly mis-estimated by MOSIS, as previously discussed.

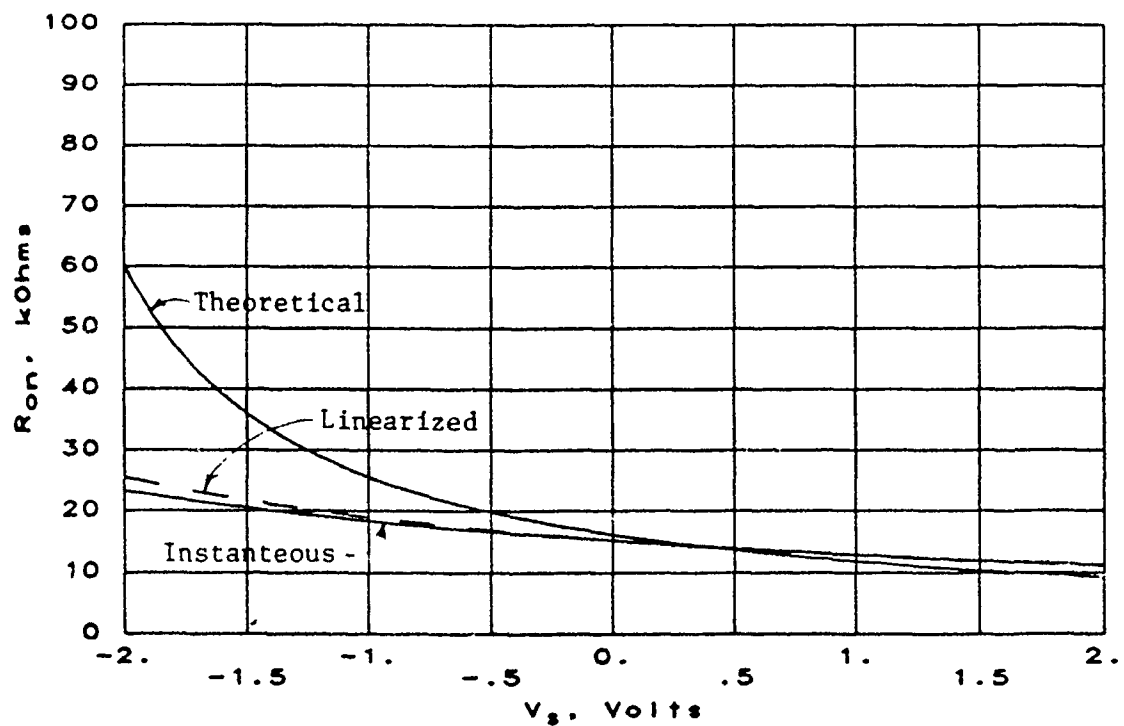
The hand-calculated results discussed earlier agreed in basic trends as can be seen from Fig. 2.2-14, but quantitatively differ as described below.

- (a) The bulk-effect started affecting the devices on-resistances at a much lower bias voltage than is predicted by the SPICE simulation. This is particularly noticable in the p-channel device.
- (b) When the bulk-effect is non-dominant, the simulated on resistance differs from that of the hand analysis by about 20%.

The differences between hand-calculations and the simulated results can primarily be attributed to the specific SPICE parameters MOSIS supplies. Ideally, the SPICE simulation should more accurately represent the physical system, although this accuracy remains in question for these specific SPICE parameters.



(a) n-channel ($L = 3\mu m$, $W = 4\mu m$)



(b) p-channel ($L = 3\mu m$, $W = 4\mu m$)

Fig. 2.2-14. Effective on-resistance of a single pass-transistor MOSFET as a function of the biasing V_s .

On-Resistance Model

Motivated by the modeling problems in and near the weak inversion region of the MOSFET I-V characteristics, only the region near $V_S = 0V$ will be considered. This region coincides with the middle of the normal operating region for this device. In this region, both the n- and p-channel transistor's on-resistance varies linearly with V_S , as is shown in Figs. 2.2-14a and 2.2-14b. Thus consider the following macro-model for the small-signal voltage dependent on-resistance, \tilde{r}_{on} .

$$\tilde{r}_{on} \approx r_{on_o} (1 + m_{V_S} V_S) \quad (2.2 - 43a)$$

where

$$r_{on_o} \stackrel{\text{def}}{=} r_{on} |_{V_S=0V} \quad (2.2 - 43b)$$

$$m_{V_S} \stackrel{\text{def}}{=} \left. \frac{\delta \frac{r_{on}}{r_{on_o}}}{\delta V_S} \right|_{V_S=0V} \quad (2.2 - 43c)$$

Here r_{on_o} represents the nominal value of r_{on} , while the model parameter m_{V_S} represents the slope of the normalized r_{on} as a function of V_S . This macro-model will be used to model the 1st-order nonlinearities associated with the on-resistance of the simple analog switches. The parameter m_{V_S} can be thought of as a figure of merit for characterizing nonlinearity of analog switches with good linearity corresponding to small values of m_{V_S} .

These macro-model parameters were extracted from the previous results based upon both theoretical hand-calculations and repeated small-signal linearized SPICE simulations for different quiescent values of V_S . These parameters are shown in Table 2-10.

Comments:

- (a) As discussed before, the theoretical hand-calculation agreed quite well with the small-signal SPICE simulation for the n-channel MOSFET, showing almost identical slope with a 20% increase in nominal on-resistance. The p-channel characteristics differed significantly between the two approximation techniques with a 50% decrease in slope observed for the simulation relative to the theoretical.
- (b) Observe the change in slope m_{V_S} and the nominal on-resistance r_{on_o} between the two n-channel transistors and also between to the two p-channel devices. This shows that the n-channel transistor is less influenced by short-channel effects with a 20% change in m_{V_S} and a 25% change in r_{on_o} , than the p-channel transistor with a 45% change in m_{V_S} and a 40% change in r_{on_o} .
- (c) The floating-well n-channel transistor showed a 40% decrease in the nominal on-resistance in comparison to the regular n-channel transistor with the same device sizes. This can be attributed to the bulk-effect sweeping majority carriers (e^-) out of the channel. Also the nonlinearity or slope of r_{on} was decreased 50%.

Table 2.2-10. 1st-Order nonlinear model for the p- and n-channel simple analog switches.

Device			Theoretical		Linearized	
Type	W	L	r_{on_0}	mV_s	r_{on_0}	mV_s
n-channel	$4\mu m$	$3\mu m$	$9.58k\Omega$	+0.51	$10.70k\Omega$	+0.59
n-channel	$12\mu m$	$9\mu m$	$10.70k\Omega$	+0.59	$16.20k\Omega$	+0.37
p-channel	$4\mu m$	$3\mu m$	$16.20k\Omega$	-0.37	$8.01k\Omega$	-0.35
p-channel	$40\mu m$	$30\mu m$	$17.94k\Omega$	-0.43	$24.78k\Omega$	-0.35
floating n-chan.	$4\mu m$	$3\mu m$	$8.01k\Omega$	+0.35	$4.41k\Omega$	+0.23

This is noteworthy since this shows that for a complex model that includes bulk-effects, short-channel effects and other complexities; the nonlinearity due to the V_{GS} dependencies of Eq. 2.2-39 contributes 50% of the overall error.

Complimentary Analog Switches

In the previous section, we analyzed the single device pass-transistor architectures and attempted to determine the overall variation in on-resistance as a function of the DC biasing of the source node. In this section the complimentary analog switches of Fig. 2.2-11c and d will be studied. In each of the single device architectures, the designer has only the width and length parameters available for optimizing performance with the W/L ratio fixed by specified on resistance. If the length is assumed minimum, to minimize on impedance, the designer has no free parameters for optimizing performance. In the case of the complimentary switches of Fig. 2.2-11c, the designer has control of the four geometrical device sizing parameters, L_p , L_n , W_p and W_n . With L_p and L_n fixed at $3\mu m$ to minimize on resistance, the ratio W_p/W_n and the width W_n are convenient free variables. We shall refer to this ratio, W_p/W_n , as " α ",

$$\alpha \stackrel{\text{def}}{=} \frac{W_p}{W_n}. \quad (2.2 - 44)$$

The overall on-conductance g_{np} of the parallel combination of the two on-conductance per unit width of the n-channel transistor is, ideally, expressed as follows in terms of α :

$$g_{np} = g_n + \alpha g_p \quad (2.2 - 45)$$

where g_n and g_p represents the unit voltage dependent on-conductance for the n- and p-channel MOSFETs with unit channel-widths and channel-lengths of $4\mu m$ and $3\mu m$ respectively.

To better illustrate how the complimentary analog switch has an improved linearity over the single pass-transistor class of switches, a family of plots of the effective unit on-resistance of the standard analog switch as a function of both the source voltage V_S and the design parameter α is shown in Fig. 2.2-15. This plot was based upon the results discussed previously in which the on-resistances of the discrete pass-transistors was computed from multiple small-signal transfer function SPICE analysis. From these plots it becomes evident that the design parameter α is a useful design tool for minimizing on-resistance nonlinearities.

Minimization of On-Resistance Nonlinearities

There are three techniques presented here for minimizing the nonlinearities of the on-resistance of the complimentary devices. which are as follows:

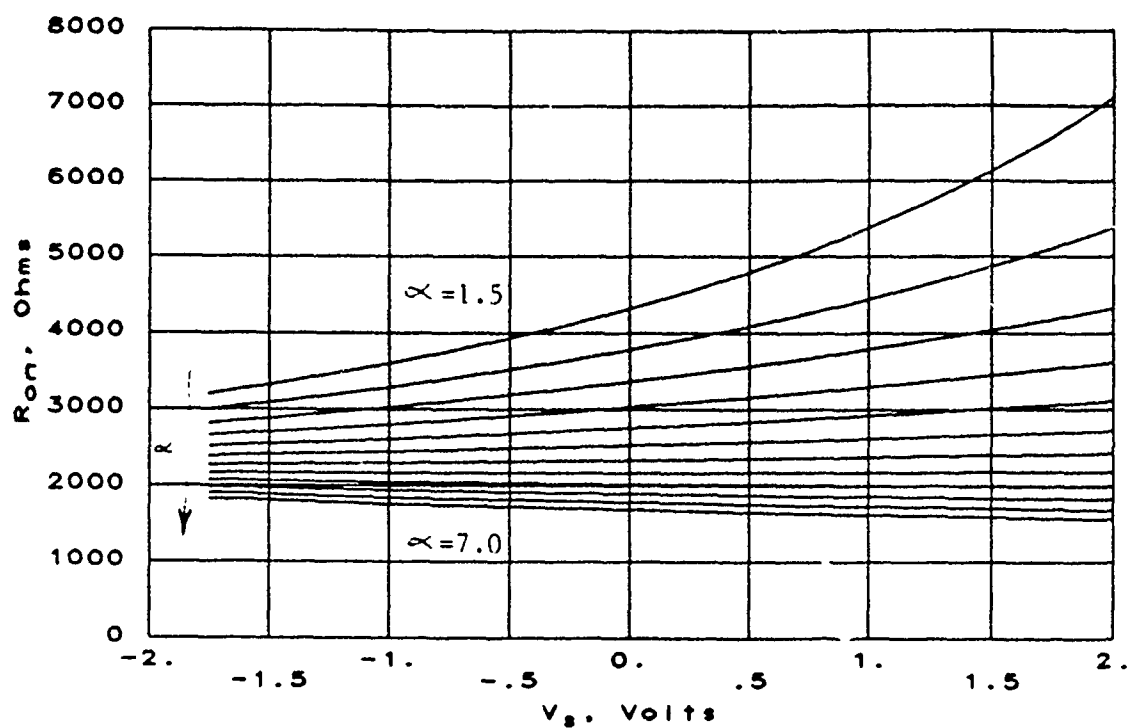


Fig. 2.2-15. The effective small-signal simulated on-resistance of the standard complimentary switch shown in Fig. 2.2-11c vs. the DC potential V_S of the test circuit shown in Fig. 2.2-13a as a function of α the design parameter.

Theoretical Approach — From equations (2.2-40a) and (2.2-40b) g_{np} can be computed as follows:

$$g_{np} = \beta_n \left(5 - V_S - V_{T_{on}} - \gamma_n \left(\sqrt{\psi + V_S + 5} - \sqrt{\psi} \right) \right) + \alpha\beta_p \left(5 + V_S - V_{T_{op}} - \gamma_p \left(\sqrt{\psi - V_S + 5} - \sqrt{\psi} \right) \right) \quad (2.2 - 46)$$

This equation can be broken into two parts: a portion independent of V_S and a portion dependent upon V_S , i.e.,

$$g_{np}^{(lin)} = \beta_n \left(5 - V_{T_{on}} + \gamma_n \sqrt{\psi} \right) + \alpha\beta_p \left(5 - V_{T_{op}} + \gamma_p \sqrt{\psi} \right) - (\gamma_n \beta_n + \alpha\gamma_p \beta_p) \sqrt{\psi + 5} \quad (2.2 - 47)$$

$$g_{np}^{(non)}(V_S) = V_S(\beta_n - \alpha\beta_p) - \gamma_n \beta_n (\sqrt{\psi + V_S + 5} - \sqrt{\psi + 5}) - \alpha\gamma_p \beta_p (\sqrt{\psi - V_S + 5} - \sqrt{\psi + 5}) \quad (2.2 - 48)$$

where $g_{np}^{(lin)}$ is the linear on-conductance component and $g_{np}^{(non)}$ is the nonlinear component expressed as a function of V_S .

Before we attempt to minimize $g_{np}^{(non)}$ effects, this function was first normalized with respect to the average conductance g_{np_0} defined as

$$g_{np_0} \stackrel{\text{def}}{=} g_{np}|_{V_S=0} = \beta_n \left(5 - V_{T_{on}} - \gamma_n \left(\sqrt{\psi + 5} - \sqrt{\psi} \right) \right) + \alpha\beta_p \left(5 - V_{T_{op}} - \gamma_p \left(\sqrt{\psi + 5} - \sqrt{\psi} \right) \right)$$

Assuming $\psi \approx .6V$, this equation reduces to

$$g_{np_0} \approx \beta_n (5 - V_{T_{on}} - 1.592\gamma_n) + \alpha\beta_p (5 - V_{T_{op}} - 1.592\gamma_p) \quad (2.2 - 49)$$

The normalized nonlinear conductance shall be referred to as $\hat{g}_{np}^{(non)}$, and is defined by the equation

$$\hat{g}_{np}^{(non)} = \frac{g_{np}^{(non)}}{g_{np_0}} \quad (2.2 - 50)$$

Comments:

- (a) For large reverse bias voltages across the source-diffusion/bulk junction the effective V_{th} of the MOS device increases due to the bulk effect, thus reducing the $V_{GS} - V_{th}$ across the gate and forcing the device into the poorly modelled weak-inversion region. In order to avoid this region and the inaccuracies associated with a simplified hand-analysis, only those values of V_S near zero will be considered.

- (b) In Eq. (2.2-48) the nonlinear component is composed of two parts, (a) the V_{GS} component, $V_S(\beta_n - \alpha\beta_p)$ and (b) the V_{BS} term or γ -effect component.
- (c) Of these two parts, the V_{GS} component is well modeled, while the γ component is not. The MOSIS process parameters used in the V_{GS} component are easily extracted from experimental data and thus expected to depict the process and this aspect of the analysis accurately. The process parameters associated with the γ component are not easily extracted.

Because of the above comments, it was decided to minimize or cancel only the 1st-order effects (i.e., V_{GS} component) with the design parameter α . More precisely this is accomplished by taking the following limite and solving for α .

$$\lim_{V_S \rightarrow 0} \frac{\delta \hat{g}_{np}^{(non)}}{\delta V_S} = 0, \quad (2.2 - 51a)$$

where $\hat{g}_{np}^{(non)}$ is defined in eqs. (2.2-48) and (2.2-50). Thus using the process parameters found in Appendix-A, we find

$$\alpha = \frac{\beta_n}{\beta_p} \approx 2.2 \quad (2.2 - 51b)$$

SPICE Simulation Min/Max Technique — Another approach to minimizing the nonlinearities contributed by the voltage dependent on-resistances of the analog switch, is to compute the effective on-resistance from either of the three methods of approximating this impedance, (i.e., theoretical hand analysis, small-signal linearized SPICE simulation, large-signal instantaneous SPICE simulation), as illustrated by the family of curves shown in Fig. 2.2-15.

The following heuristic figure of merit σ for characterizing the presence of voltage dependencies on a resistor will be used to characterize the complimentary switches.

$$\sigma = 100\% \times \left| \frac{r_{on}(V_S = -2V) - r_{on}(V_S = +2V)}{r_{on}(V_S = 0V)} \right| \quad (2.2 - 52)$$

This figure of merit characterizes the worstcase variation in the on-resistance normalized relative to the nominal value of r_{on} at $V_S = 0V$. This is useful when the on-resistance r_{on} as a function of the V_S is a monotonic function, as illustrated by the smooth nearly flat curves shown in Fig. 2.2-15. When r_{on} is almost linear, the monotonicity can not be ascertained from the curves shown in Fig. 2.2-15 but in this case, the nonlinearity would be very small anyway.

A plot of σ versus α for each of the three approximation techniques is shown in Fig. 2.2-16a, The following comments can be made.

Comments:

- (a) The small-signal "linearized" and large-signal "instantaneous" SPICE simulations agreed fairly well, recommending channel-width ratios around 5 with a corresponding figure of merit of less than 10% deviation from the nominal value.
- (b) σ for the two SPICE approximations was fairly insensitive to variation in α , as signified by the broad shallow dip around $\alpha = 5$, and thus the optimal α is fairly insensitive to large process variation associated with the process parameters which contribute to this nonlinearity.
- (c) Hypothetically the relative variation in r_{on} could be minimized to approximately 1%, given an exact characterization and modeling of the process was known a priori to fabrication. Obviously this is not practical, but it does bring out the point that the more exact our model is and the finer the control of the process is, the better the circuit performance can be predicted and designed, thus yielding a highly linearized analog switch.
- (d) The "theoretical" hand-calculations differed significantly from the SPICE simulated approximations in the sense the optimal α was approximately 2.4 and was much more sensitive to process variation. This can be attributed to the increased sensitivity to the bulk-effect as was illustrated in the Fig. 2.2-14a and 2.2-14b.
- (e) The optimal α for the theoretical curve was very close to that predicted by the earlier hand-calculation presented in Eq. (2.2-51) (i.e., $\alpha = 2.2$).

The floating-well complimentary switch was compared to the regular complimentary switch via the small-signal SPICE simulation approximation. The results of this comparison are shown in Fig. 2.2-16b.

Comments:

- (a) Both curves look almost identical in shape.
- (b) The floating-well complimentary switch showed an optimal value for α around 4 instead of 5 as before.
- (c) Since there was no noticeable increase in the overall linearity of the analog switch, utilization of this more complex structure (floating-well) is not particularly justifiable. This was not as expected and implies that the bulk-effect was non-dominant. The hand-analysis should include a more elaborate model for short-channel effects to more closely predict these simulated results.

SPICE Simulation Slope Technique — Motivated by the modeling problems in and near the weak inversion region of the MOSFET I-V characteristics; the 1st-order non-linear model developed previously and shown in Eq. (2.2-43) and tabulated in Table 2.2-10

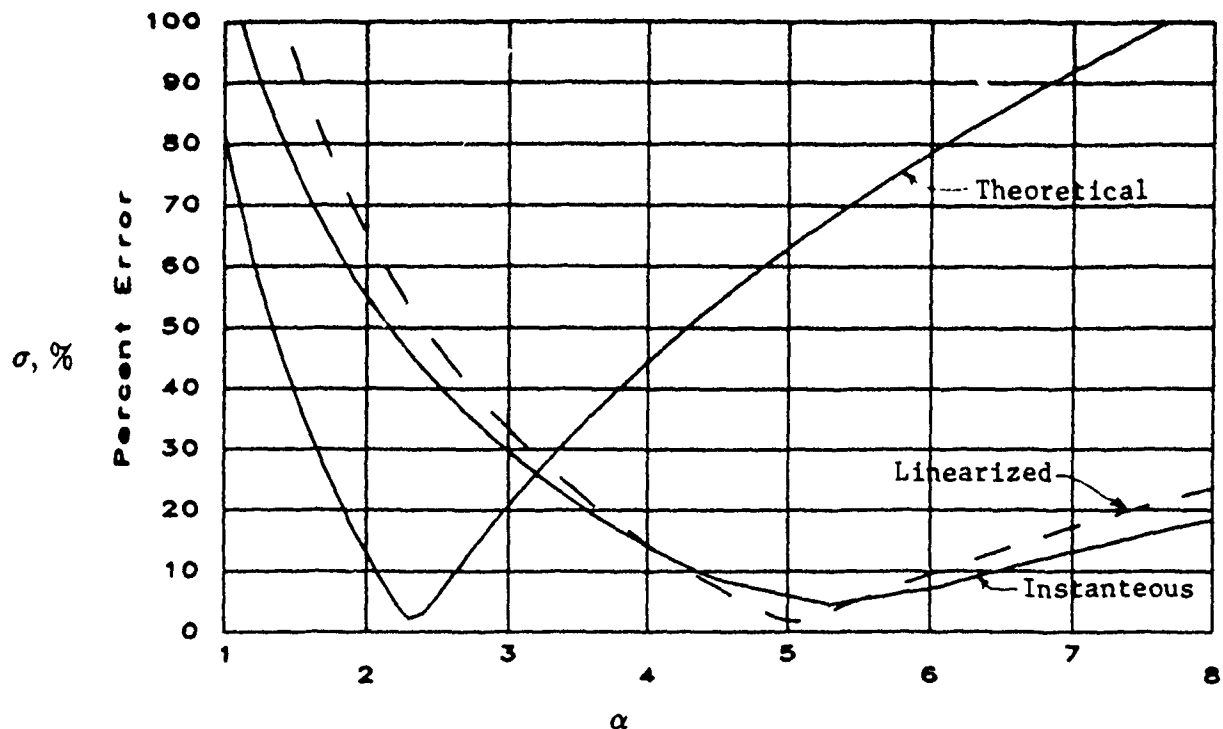


Fig. 2.2-16a. On-Resistance nonlinearity figure of merit σ for the complimentary switch of Fig. 2.2-11c vs. the design parameter α for all three r_{on} approximations.

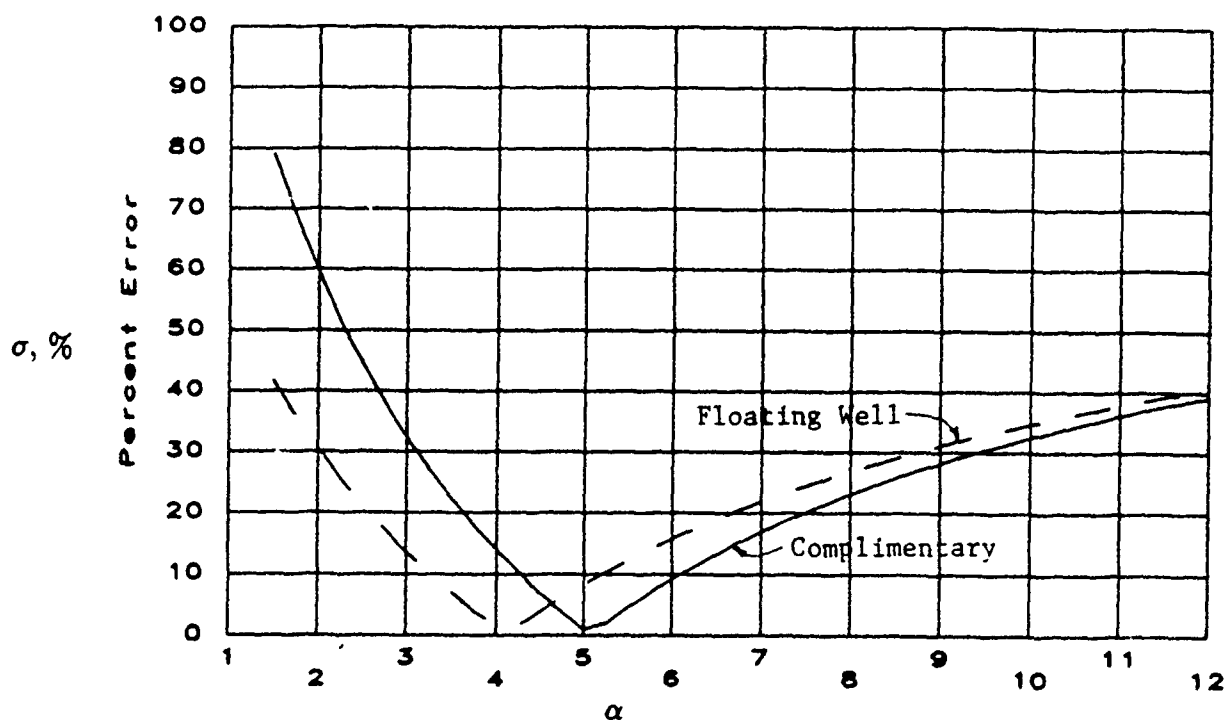


Fig. 2.2-16b. On-Resistance nonlinearity figure of merit σ for the small-signal SPICE simulation approximation vs. the design parameter α for both type of complimentary switches as shown in Figs. 2.2-11c and 2.2-11d.

will be used to develop this equivalent model for the complimentary analog switches.

Let the n- and p-channel devices be modeled by the following equations:

$$\tilde{r}_n \approx r_{n_o} (1 + m_n V_S) \quad (2.2 - 53a)$$

$$\tilde{r}_p \approx \frac{1}{\alpha} r_{p_o} (1 + m_p V_S) \quad (2.2 - 53b)$$

where r_{n_o} and r_{p_o} represent the nominal value of r_{on} formerly referred to as r_{on_o} . Also the terms m_n and m_p represent the slope of the normalized on-resistance, formerly m_{V_S} .

Now the effective on-resistance r_{np} of the complimentary analog switch can be expressed as the parallel combination of these two models, or rather

$$r_{np} = \frac{\tilde{r}_n \tilde{r}_p}{\tilde{r}_n + \tilde{r}_p} \quad (2.2 - 54a)$$

$$= \frac{r_{n_o} r_{p_o} (1 + m_n V_S) (1 + m_p V_S)}{(\alpha r_{n_o} + r_{p_o}) + (\alpha r_{n_o} m_n + r_{p_o} m_p) V_S} \quad (2.2 - 54b)$$

Therefore the slope of the normalized on-resistance of the complimentary switch at $V_S = 0V$ is as follows:

$$m_{np} \stackrel{\text{def}}{=} \left. \frac{\delta \frac{r_{np}}{r_{np_o}}}{\delta V_S} \right|_{V_S=0V} = \frac{\alpha r_{n_o} m_p + r_{p_o} m_n}{\alpha r_{n_o} + r_{p_o}} \quad (2.2 - 55a)$$

where

$$r_{np_o} = \frac{r_{n_o} r_{p_o}}{\alpha r_{n_o} + r_{p_o}} \quad (2.2 - 55b)$$

This slope represents the 1st-order nonlinearity of the on-resistance of the complimentary switch as a function of the 1st-order nonlinearities of the n- and p-channel pass-transistors. To minimize this nonideality via the design parameter α

let $m_{np} = 0$ and solve for the corresponding α , i.e.,

$$\boxed{\alpha = - \frac{m_n r_{p_o}}{m_p r_{n_o}}} \quad (2.2 - 56)$$

Note this technique eliminates nonlinearities near the middle of the input voltage swing and not for the full range signals. α was computed from Eq. (2.2-56) and the model data contained in Table 2.2-10. These results are presented in Table 2.2-11.

The n-channel device sizes and the p-channel length shown in Table 2.2-11, indicate the intended sizes, while the width of the p-channel is intended to be multiplied by α for optimal performance. Note also the channel-widths of both the n- and p-channel device can be scaled up together to decrease the on-resistance of the complimentary switch, as long as the ratio remains constant.

This analysis agrees quite well with that predicted by the "SPICE Simulation Min/Max Technique".

Table 2.2-11. Optimal design values for α based upon Eq. (2.2-56) and the parametric data contained in Table 2.2-10 as a function of the switch type and the unit device size prior to scaling by α .

Switch Type	n-chan		p-chan		α	
	W	L	W	L	Theoretical	Linearized
Standard	$4\mu m$	$3\mu m$	$4\mu m$	$3\mu m$	2.3	5.1
Floating	$4\mu m$	$3\mu m$	$4\mu m$	$3\mu m$	1.9	4.0
Standard	$12\mu m$	$9\mu m$	$40\mu m$	$30\mu m$	2.3	4.3

Conclusions

The results presented here show a large shallow minimum associated with determining the "optimal" α 's. From the evidence presented in this section the following observations can be made:

- (1) The optimum α lies somewhere in the range of 2.2 to 5, with an associated error (σ) somewhere in the range of 30-50%. The recommended value for α is 3.2 with a corresponding expected value for σ of 30%, as approximated by the intersection of the "theoretical" and "instantaneous" curves, as shown in Fig. 2.2-16a.
- (2) The validity of the MOSIS SPICE model parameters for this type of analysis are questioned.
- (3) The optimum α can be extracted from experimental measurements as those anticipated from the test vehicle discussed in section 5.16.
- (4) If a circuit design relies on matching or exact device sizes to cancel out these complex nonlinearities, the design is doomed from the start. This should only emphasize how important it is that this nonideality be designed out instead of designed with.

Voltage Dependent Diffusion Capacitor Nonlinearities:

The basic MOS technology depends upon the source and drain diffusions being reversed biased with respect to the bulk or well, thus providing isolation from the bulk/well and also preventing unwanted large forward biased currents. Accompanying these diffusions is a parasitic capacitance formed by the depletion region surrounding each of these reversed biased p/n-junctions. This parasitic capacitance has two dominant effects on switch performance:

- (1) It adds extraneous load capacitance to internal nodes of the analog network, thus resulting in additional parasitic poles.
- (2) The value of this parasitic capacitance is highly dependent upon the magnitude of the reverse bias across the p/n-junction and thus injects voltage dependent nonlinearities in the host network.

This section focuses on the magnitude of these nonidealities and on layout strategies to minimize their effects.

Since this parasitic capacitor is voltage dependent, it can be treated as any other nonlinear device by

- (a) determining the DC bias point (i.e., the amount of reverse bias across the p/n-junction, which shall be referred to as V_{BS} or bulk-source voltage)

- (b) computing its effective small-signal linearized AC equivalent parasitic capacitance C_{par} about this operating point, such that

$$C_{par} \stackrel{\text{def}}{=} \frac{\delta Q_j}{\delta V_{BS}}, \quad (2.2 - 57)$$

where Q_j represents the charge stored in the diffusion region and V_{BS} is the voltage drop across the capacitor.

Theory

This parasitic capacitance is well characterized by existing models, and the corresponding process characterization parameters are easily extracted from experimental data. This capacitance is typically broken into two parts, (1) a sidewall capacitance which is a function of the perimeter of the diffusion and (2) a bottom plate capacitor which is a function of the lateral junction area A_j . These parasitic capacitances have different characteristics because of a field implant surrounding the perimeter P_j of the diffusion. Also because of this implant the perimeter does not include the perimeter adjacent to the channel [20].

The capacitance model [19] is as follows:

$$C_{par} = \frac{A_j C_j}{\left(1 + \frac{V_{BS}}{\phi_B}\right)^{M_j}} + \frac{P_j C_{jsw}}{\left(1 + \frac{V_{BS}}{\phi_B}\right)^{M_{jsw}}} \quad (2.2 - 58)$$

where the process is specified by five constants: C_j the zero-bias bottom junction capacitance density (per unit junction area), C_{jsw} the zero-bias junction sidewall capacitance density (per unit perimeter length), M_j the bottom grading coefficient, M_{jsw} the grading coefficient of the sidewall, and ϕ_B is the bulk junction potential (typically 0.8V).

For the MOSIS 3 μ CMOS process the area and perimeter of the source and drain can be related to the channel-width of the MOS device for a minimum size layout. It will be assumed that the drain and source perimeters and areas are characterized by the equations

Small Devices: $W < 7\mu m$

$$A_D = A_S = 49\mu m^2 + (2\mu m)W \quad (2.2 - 59a)$$

$$P_D = P_S = 32\mu m - W \quad (2.2 - 59b)$$

Medium Devices: $7\mu m \leq W \leq \sim 50\mu m$

$$A_D = A_S = (8\mu m)W \quad (2.2 - 59c)$$

$$P_D = P_S = W + 16\mu m \quad (2.2 - 59d)$$

Large Devices: $W > \sim 50\mu m$

$$A_D = (8\mu m)W \quad (2.2 - 59e)$$

$$A_S = \left(\frac{9}{2}\mu m\right)W \quad (2.2 - 59f)$$

$$P_D = W + 32\mu m \quad (2.2 - 59g)$$

$$P_S = 18\mu m \quad (2.2 - 59h)$$

Simulation

From this theory, n^+ and p^+ diffusion capacitors were simulated with channel-widths of $8\mu m$ over the full scale range of $\pm 2V$ with the bulks at $\pm 5V$. The results of these two simulation are shown in Fig. 2.2-17 and are labeled C_n and C_p .

Comments:

- (1) For the n-type diffusion, as V_S was increased, the junction formed by the n^+ diffusion and the p^- bulk/well at $-5V$ became increasingly reversed biased. This increases the width of the depletion region surrounding the junction and thus decreases the small-signal capacitance C_n .
- (2) Similarly, the p-type diffusion exhibited an increase in capacitance C_p as V_S was increased, since this was decreasing the reverse-bias.
- (3) By placing the two nonlinear capacitors in parallel the parasitic effects tended to cancel each other, in a similar manner as did the on-resistance nonlinearities cancel in complimentary switch. Note: It is very common in analog IC design for internal nodes to have both a parasitic n^+ and p^+ diffusions attached. This is illustrated by the plot of C_{np} in Fig. 2.2-17 which is $\frac{1}{2}$ of the parallel combination of C_p and C_n , each sized at $8 \times 8\mu m^2$.
- (4) The optimal ratio between the area of the n^+ diffusion and the area of the p^+ diffusion is approximately 1:1.

Conclusions

The overall percent change in C_n with respect to the nominal capacitance C_{n_0} defined as C_n at $V_S = 0V$ over a $\pm 2V$ range, was as follows along with corresponding results for C_p and C_{pn} .

$$\Delta C_n = 32\% \quad \Delta C_p = 31\% \quad \Delta C_{np} = 5\% \quad (2.2 - 60a)$$

A $6\times$ improvement can be gained by sizing the p^+ and n^+ diffusions the same size, with an approximate parasitic capacitance of

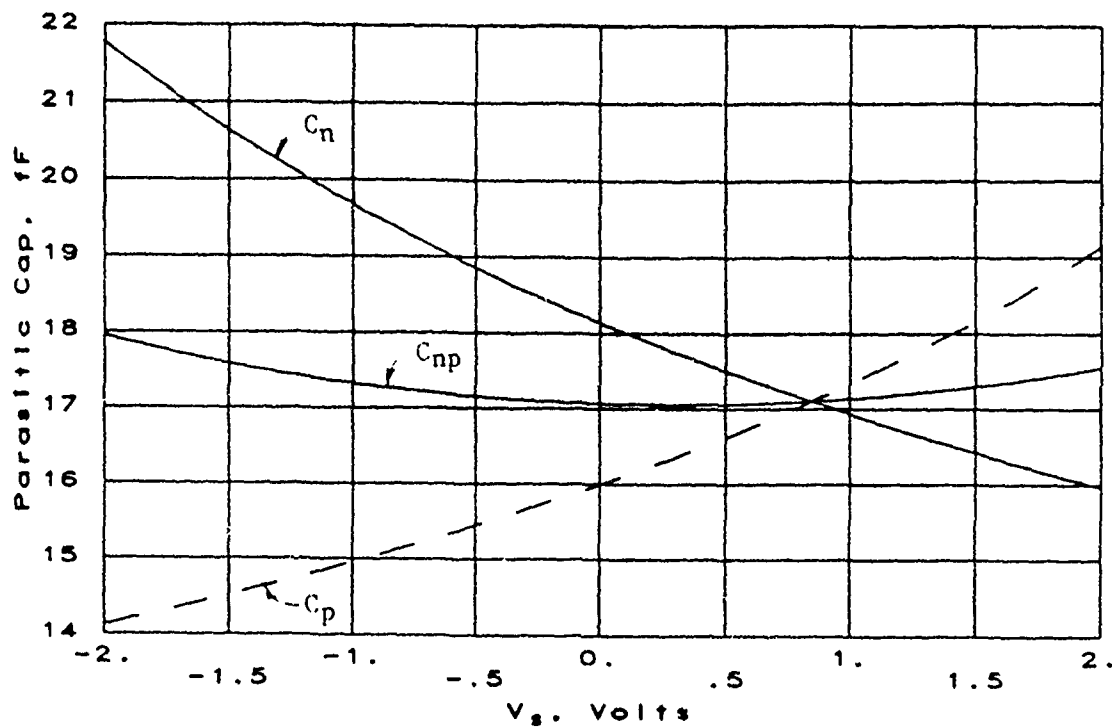


Fig. 2.2-17. Simulated small-signal capacitance for diffusion junction capacitors as a function of the DC potential V_s of the diffusion region relative to ground with the bulks at $\pm 5V$. ($C_n \Rightarrow n^+$ diffusion, $C_p \Rightarrow p^+$ diffusion and $C_{np} \Rightarrow \frac{C_n C_p}{C_n + C_p}$)

$$C_{par} \approx \frac{1}{4} \frac{fF}{\mu m^2} \quad (2.2 - 60b)$$

Clock Feed Through Effects:

The clock feed through problem originates from a capacitive coupling between the gate and the channel of a MOSFET. This coupling allows the control signal which turns the device "off" and "on" to feed through into source and drain nodes. In applications where the switch is used to store charge on a capacitor, which is regularly required in switched-capacitor and sample and hold circuits, this feed through distorts the charge content and associated potential of the drain and/or source nodes. The term *clock* or *clock feed through* originated from the two phase clock controls lines found in switched capacitor circuits, which has been a driving force in studying this phenomena and understanding it.

Before this problem can be addressed, the coupling capacitor must be identified and discussed. This coupling capacitor is composed of two components,

- (1) the overlap capacitor C_{ov} formed between the edge of the polysilicon gate and the portion of the source and drain diffusions that have laterally diffused under the gate (typically $\frac{1}{4}\mu m - \frac{1}{2}\mu m$); and
- (2) the gate capacitor C_G formed between the gate and the conductive charge in the channel.

The first capacitor is a voltage independent parallel plate capacitor tied between both the gate and source nodes and the gate and drain nodes of value

$$C_{ov} = C_{ox} W L_D = \frac{\epsilon_{ox}}{T_{ox}} W L_D, \quad (2.2 - 61)$$

where W is the channel-width, L_D is the lateral diffusion length, ϵ_{ox} is the permittivity of SiO_2 , and T_{ox} is the thickness of the oxide.

The second type of capacitor is operation region dependent and is complicated by the concept of a channel and how it relates to the four terminals of a MOS device. For instance, if an NMOS transistor is "off", meaning that the gate is at a low potential, then the gate depletes the concentration of majority carriers in the region underneath the gate or channel to the point the channel is non-conductive. Since the available free minority carrier (holes) concentration is minuscule, there is no attributable charge in the channel. But now if we slowly turn "on" the device by increasing the gate potential, electrons will collect in the channel. Thus if we assume this charge is evenly distributed underneath the channel, or rather that the source and drain nodes are at the same potential, then the effective gate capacitance is a function of the width and length of the gate and the oxide thickness, given by the expression

$$C_G = C_{ox} W L. \quad (2.2 - 62)$$

where W and L are the width and length of the channel, and C_{ox} is the gate capacitance density. This distributed capacitance is typically lumped for analysis purposes by dividing it equally between the source and drain nodes such that,

$$C_{GS} = C_{GD} = \frac{1}{2}C_{ox}WL + C_{ov}. \quad (2.2 - 63)$$

Now if the source and drain nodes are no longer constrained to be at the same potential, then the node with the higher potential (commonly referred to as the drain) will attract more of the e^- towards it thus cause a skewing effect in charge distribution. If the voltage drop between the source and drain V_{DS} is increased even more, then portions of the channel near the drain terminal will be depleted of almost all charge. In this situation the channel is "pinched off" and the device is now operating in saturation. In this mode it is a standard practice to attribute $\frac{2}{3}$ of the gate capacitance C_G with the source node and none with the drain node, as expressed in Eq. (2.2-64) [21].

$$C_{GS} = \frac{2}{3}C_{ox}WL + C_{ov} \quad (2.2 - 64a)$$

$$C_{GD} = C_{ov} \quad (2.2 - 64b)$$

Fortunately, the analog switches currently under investigation are assumed to have very little voltage drop across the pass-transistors, and thus they are operating in the active or cutoff regions, and particularly, not in saturation.

From the above discussion it should be obvious that as a device goes from the "on" state (active) to the "off" state (cutoff) the distributed charge in the channel must be dissipated to the source and drain nodes. If we think of the channel while in the active-mode as a conductor shorting the source and drain nodes, then when the gate is turned "off" the charge in the channel can exit by either path (source or drain). Thus the external impedance loading of the source and drain nodes plays a vital role in determining how this charge is redistributed. The concept being illustrated here is that if the gate voltage is instantaneously turned "off", the charge in the channel becomes highly motivated to evacuate the channel, thus taking the path of least impedance. For example, if the external load impedance differed between the two nodes by a factor of two, then it would be expected to see twice as much charge leave by the way of least impedance over the other pathway. The worstcase loading would result in the entire charge $C_{ox}WL(V_{GS} - V_{TE})$ being redistributed onto the source (drain) node, given the loading impedance on the drain (source) node is so great that it restricted the flow of charge in this direction.

In typical S/H applications the loading impedance on the source and drain nodes of the analog switch are predominately capacitive, thus in order to isolate or protect a node from this feed through effect, additional load capacitance can be added to the other node. This phenomenon is discussed well in references [22], [23], and [24], and illustrated

in Fig. 2.2-19, where the ratio of the amount of charge Q_L dumped on a load capacitor C_L to the amount of charge initially present in the channel Q_{ch} is plotted as a function of (1) the ratio the source capacitor C_S as shown in Fig. 2.2-18 to the load capacitor C_L , and (2) the fall rate of the clock signal expressed as a dimension-less quantity

$$(V_H - V_{TE}) \sqrt{\frac{\beta}{UC_L}} \quad (2.2 - 65a)$$

where V_{TE} is the effective threshold voltage, $\beta = \mu C_{ox} \frac{W}{L}$, and U is the fall rate.

Comments:

- (1) For slow clock transitions the charge in the channel had ample time to redistribute itself before much charge had time to exit the channel region, as evident by the left-hand side of Fig. 2.2-19.
- (2) For a fast clock transition or fall time, the charge in the channel had no time to redistribute, and thus fled this region by the path of least impedance, as evident by the right-hand side of Fig. 2.2-19.

Complimentary Analog Switches

Both the n- and p-channel pass-transistors are subject to the above clock feed through phenomenon, with a somewhat cancelling effect, since the clock signal driving the n-channel device is trying to inject e^- onto the source and drain nodes, while the clock of the p-channel transistor is trying to inject *holes* onto these nodes. Unfortunately, the p-channel device is typically 2-5 times bigger than the n-channel device, thus this cancelling effect could realistically contribute only to a 20-50% reduction in clock feed through.

The above description of the complimentary switch is over simplified. In actuality, the p- and n-channel devices do not switch simultaneous, thus affecting the load impedance seen on the source and drain nodes as the first device turns "off". This effect is complex to analyze, involving time dependent differential equations modeling the distributed charge in the channel. The results of this analysis as shown in Fig. 2.2-20, show the amount of switch charge injected onto a $5pF$ load capacitor when a complimentary switch was turned "off", as a function of the time delay t_d or skew between the n-channel and p-channel clock waveforms, as a function of the n-channel clock rise times t_G for a fixed p-channel clock fall times $t_{GP} = 10\eta sec$ [24].

Comments:

- (1) In the results shown in Fig. 2.2-20, the p-channel and n-channel pass-transistors had the same size, thus for equal rise times and fall times, and for a clock time delay t_d of zero, the charge injection was zero.

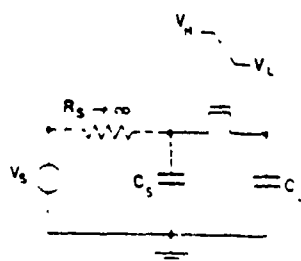


Fig. 2.2-18. Test circuit for modeling the clock feed through effects or switch charge injection of a single MOS device as used to generate the results shown in Fig. 2.2-19. Courtesy of the Department of Electrical Engineering and Information Sciences Institute, University of Southern California [23].

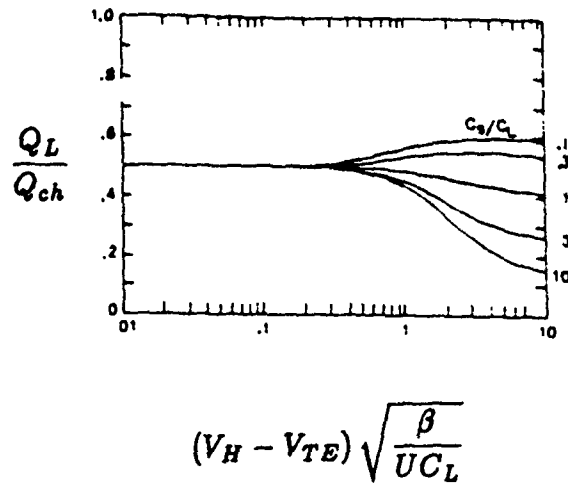


Fig. 2.2-19. Percentage of channel charge Q_{ch} injected in the data-holding node and C_L , for the test circuit shown in Fig. 2.2-18. A family of curves corresponding to various C_S/C_L ratios (listed to right of curves) has been plotted. Courtesy of the Department of Electrical Engineering and Information Sciences Institute, University of Southern California [23].

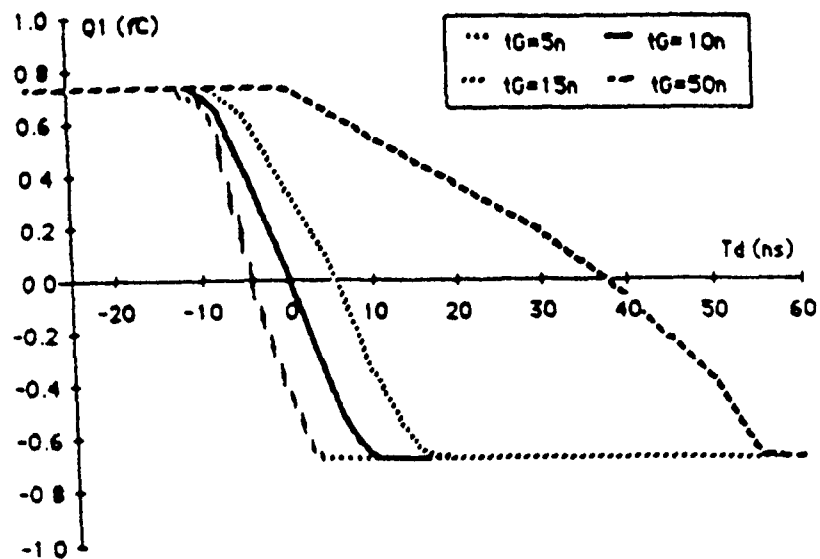


Fig. 2.2-20. Theoretical clock feed through or switch charge injection onto a $5pF$ load capacitor when a complimentary switch was turned "off", as a function of the time delay t_d or between the instants the n-channel clock starts to rise and the instants the p-channel clock signals starting to fall, both with the intention of turning off their respective device. The family of curves shown here represents different n-channel clock rise times t_G for a fixed p-channel clock fall times $t_{GP} = 10$ ns. Courtesy of Kath. Universiteit Leuven, Dept. Elektrotechniek [13].

- (2) The steep transition region in the middle of each of these curves was of length slightly smaller than the sum of the two gate rise and fall times, (i.e., $t_G + t_{GP}$). Thus the flat regions to the left and right of steep transition region depicts the worstcase situation, in which one device is turned "off" completely prior to the other transistor starting to turn "off".
- (3) These plateaus have nearly equal heights, supporting the hypothesis that the worstcase charge injection is for the case of a single n-channel or p-channel transistor turning "off" by itself. The equal height was expected since the device sizes were equal and the C_{ox} parameter is constant for the n- and p-type devices.

Conclusions

The clock feed through effects examined here, can be reduced by the following design strategies:

- (1) Increase the load capacitance C_S to 3-5 times larger than the data-holding load capacitance C_L . This should approximately reduce the feed through effect by a factor of 3-5 compared to the case in which C_S is excluded completely, (assuming fast clock transitions).
- (2) For complimentary switches, time the pass-transistors to switch at exactly the same time, with as fast a clock transition as possible. Furthermore if timing jitter is a problem, then it would be advantageous to switch the larger device off first, since this device has more charge in the channel to feed through. Typically the n-channel pass-transistor is 3 times smaller than the p-channel device, thus by switching the p-channel transistor off first, would reduce the clock feed through by a factor of 3.
- (3) Lastly, make the devices as small as possible, thus restricting the amount of available charge in the channel to feed through.

A pessimistic practical estimate of this coupling capacitor for a complimentary switch would correspond to the entire gate to channel capacitance of the n-channel pass transistor, (i.e., $C_{GS} = C_{ox}W_nL_n$ where W_n and L_n correspond to the channel-length and -width of the n-channel pass-transistor). Typically with good design techniques as listed above, this number can be reduced at least by a factor of 2 and possibly as much as a factor of 5 or 10.

In light of the intended S/H application for these switches, the impact of the charge injection problem appears in two areas: (1) it induces a DC offset voltage V_{os} on the hold capacitor C_L ; and (2) this offset voltage is dependent upon the instantaneous value of the source voltage v_S , which causes nonlinear distortion of the samples. The DC offset voltage can be canceled out by the Sampling Algorithm, but the voltage dependence or nonlinear

distortion can not. This is quantified as follows.

Consider the charge injected by the gate-source coupling capacitor, C_{GS} . This charge is $Q_{ch} = C_{GS}v_{GS}$, where $v_{GS} \stackrel{\text{def}}{=} V_G - v_S$ (typically 3V-7V). V_G corresponds to the DC "on" gate potential (typically either $\pm 5V$), and v_S is the instantaneous source potential. Thus the effective offset voltage generated by Q_{ch} being dumped on to the load or holding capacitor C_L would be

$$V_{os} = v_{GS} \frac{C_{GS}}{C_L} \Rightarrow 3V \frac{C_{GS}}{C_L} \leq V_{os} \leq 7V \frac{C_{GS}}{C_L} \quad (2.2 - 66a)$$

$$V_{os} = 5V \frac{C_{GS}}{C_L} \pm 40\%. \quad (2.2 - 66b)$$

The percent variation in V_{os} relative to the input-signal range of $4V_{p-p}$ as induced by v_S varying between $\pm 2V$ is quantized as follows based upon Eq. (2.2-66b):

$$\Delta V_{os} = \pm 200 \frac{C_{ox} W_p L_p}{C_L} \% \quad (2.2 - 67)$$

The impact of V_{os} variations is discussed late in the context of the specific S/H architectures.

Leakage Current:

The source and drain diffusions associated with the n- and p-channel MOSFETs are reverse-biased p/n junctions, each with an associate reverse-bias leakage current. This leakage current is primarily a function of the area of the diffusions, and is determined by a complex relationship involving surface effects, the generation and recombination of carriers in the depletion layer, and the tunneling of carriers between states in the bandgap [25]. Because of this complexity, a simplified analysis is presented below, based upon Einstein's relation and the Shockley equation. In this model, J_{rev} represents the current density of the reversed biased pn junction and must be multiplied by the junction area to determine the total diode current. The numerical results presented here were derived from the MOSIS process parameters as contained in Appendix A and experimental measurements on the test devices.

$$J_{rev} = J_{diff} + J_{gen} \approx 0.28 \left(\frac{pA}{\mu m^2} \right) \quad (2.2 - 68a)$$

$$J_{diff} = q \left(D_p \frac{n_i^2}{N_D L_p} + D_n \frac{n_i^2}{N_A L_n} \right) = 0.281 \left(\frac{pA}{\mu m^2} \right) \quad (2.2 - 68b)$$

$$J_{gen} = \frac{1}{2} q \frac{n_i}{\tau_o} W_j = 0.464 W_j \left(\frac{A}{m^2} \right) \quad (2.2 - 68c)$$

$$D_p = \mu_p \frac{kT}{q} = 1.25 \times 10^{-3} \left(\frac{m^2}{sec} \right) \quad (2.2 - 68d)$$

$$D_n = \mu_n \frac{kT}{q} = 3.51 \times 10^{-3} \left(\frac{m^2}{sec} \right) \quad (2.2 - 68e)$$

$$L_p = \sqrt{D_p \tau_p} = 77 \times 10^{-3} (m) \quad (2.2 - 68f)$$

$$L_n = \sqrt{D_n \tau_n} = 2.96 \times 10^{-3} (m) \quad (2.2 - 68g)$$

$$N_D = 3.01 \times 10^{15} \quad (2.2 - 68h)$$

$$N_A = 1.458 \times 10^{15} \quad (2.2 - 68i)$$

Here the overall reverse-bias current density J_{rev} is computed as a function of two components: (1) the reverse-biased current density component caused by minority carriers diffusing across the depletion region J_{diff} , and (2) the component due to the generation and recombination of carriers in the depletion region J_{gen} . Of these two components it is anticipated that the diffusion current density J_{diff} will dominate over the recombination/generation component. The parameter W_j corresponding to the junction width is unknown. For p^+ diffusions the leakage current would be caused by e^- or minority carriers diffusing across the depletion region towards the positive rail into the n -well/bulk. Similarly the leakage current in n^+ diffusions are characterized as holes being swept into the p -well/bulk towards the negative voltage rail.

Conclusions

Because of the basic logistics of this phenomenon, as discussed above, the n^+ and p^+ diffusions have opposite characteristics — one is trying to charge up a node, and the other is trying to discharge this node. Thus in the case of complimentary switches the presences of both n^+ and p^+ diffusions on the source/drain nodes of the analog switch implies that there is some inherent cancellation of this effect associated with this basic architecture.

In light of the specific S/H application, the analog switch is the primary cause of charge leaking off of the hold capacitor, but there is one physical aspect that is overlooked in this discussion; and that is for charge to leak off of a capacitor, both the top plate and bottom plate of the capacitor must have current paths available. Thus if one side of the capacitor is much better isolated than the other, it will predominate the leakage effect and reduce the overall leakage current.

The leakage current for both p^+ and n^+ diffusions has been estimated around $0.28 \frac{pA}{\mu m^2}$.

2.2.2.3b Sample/Hold-1

The simplest of the three S/H architectures, referred to as S/H-1, is described here. This is followed by a discussion of inherent performance limitations of this structure. These limitations cause minor reductions in the input voltage swing and major reductions in performance at high frequencies. Experimental results for this architecture are provided

in Section 5.2 of this report.

Description:

The circuit schematic for the S/H-1 cell is shown in Fig. 2.2-21a, with its associated timing diagram contained in Fig. 2.2-21b. When the *Sample* signal is high, the S/H is in the track-mode. In this mode of operation the "sampling" analog switch S_s is turned "on" and the input signal V_i is connected across the hold capacitor C_h . In this mode if the analog switch S_s is modeled as a voltage dependent on-resistance r_s , as discussed in Section 2.2.2.3a, then the circuit can be reduced to an equivalent RC network as shown in Fig. 2.2-21c.

When the *Sample* signal is thrown low, the analog switch S_s is opened and the hold capacitor C_h is electrically isolated from the input signal V_i . This transition is referred to as "sampling", and the resultant mode of operation termed the "hold-mode". The equivalent circuit in this mode is shown in Fig. 2.2-21d. The voltage V_h across the hold capacitor is ideally the instantaneous value of the input signal grabbed at the instance the analog switch was opened. This sample and held voltage V_h is buffered by an Operational Amplifier whose output V_o is supplied to an A/D converter for conversion into a digital word.

The capacitor C_1 was added to the network to help reduce the clock feed through generated by turning "off" S_s .

The analog sampling switch S_s is the floating-well complimentary analog switch shown in Fig. 2.2-11d, and discussed in detail in Section 2.2.2.3a. This switch was designed to maximize its ability to linearly track a high-frequency input signal and to minimize clock feed through during the sampling transition. The sampling switch is an analog transmission gate compensated for signal voltage dependencies in the on-resistance of the switch over $\pm 2V$ operation. This nonlinearity distorts the input signal being sampled. The device sizes for this analog switch and the associated sample/hold component values are contained in Table 2.2-21.

Performance Limitations:

This S/H architecture was designed in accordance with DCASP-1, thus the intended input signal swing and input frequency was $\pm 2V$ and $2kHz$ to $5MHz$. The basic motivation in this design is to maximize the channel-to-channel accuracy of "sampling" large-amplitude high-frequency input signals. The performance limitations shall be broken down into three classifications, track-mode, sampling transition, and hold-mode limitations. A discussion of these limitations for this S/H structure follows.

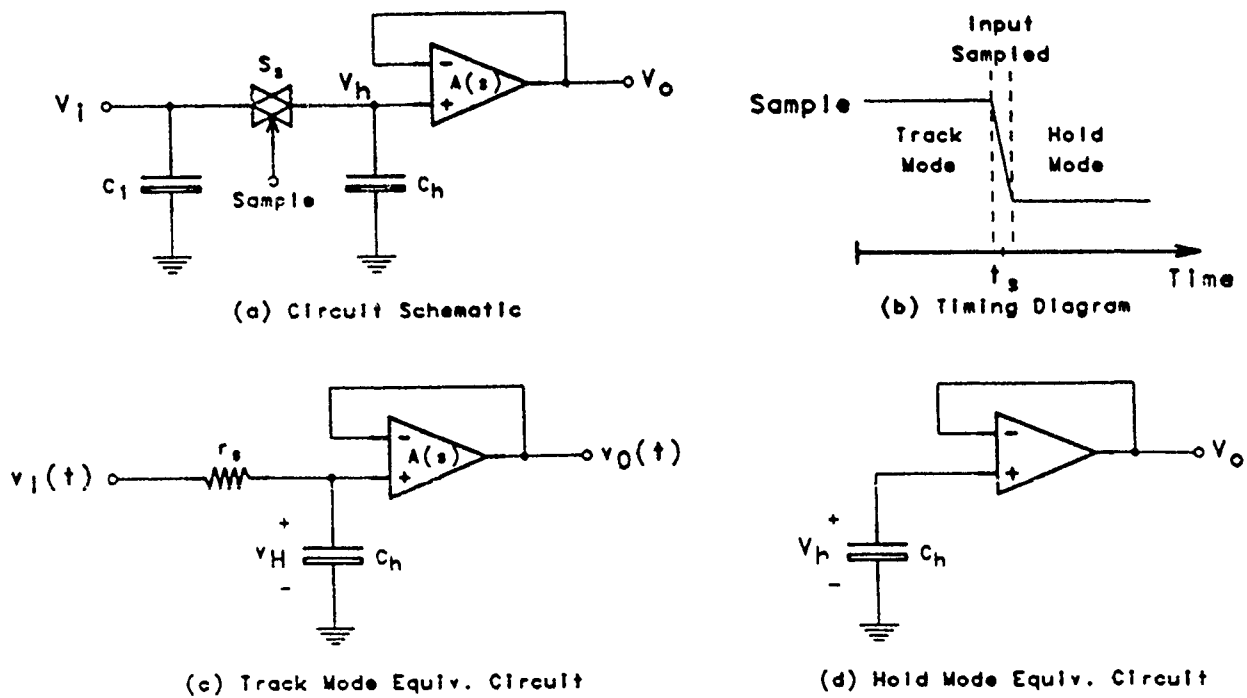


Fig. 2.2-21. S/H-1

Table 2.2-12. Device sizes and component values for S/H-1 circuit schematic of Figures 2.2-21a and 2.2-11d.

Component	Size		Value
	<i>W</i>	<i>L</i>	
M_1	$8\mu m$	$3\mu m$	
M_2	$4\mu m$	$3\mu m$	
M_3	$52\mu m$	$3\mu m$	
M_4	$26\mu m$	$3\mu m$	
C_1			$2pF$
C_h			$7pF$

Track-Mode

In the track-mode the performance issue at hand is how well does the voltage across the hold capacitor, V_h track the input signal V_i . The primary limitations discussed below are the channel-to-channel gain and phase mismatch caused by (1) voltage dependencies in the on-resistance of the analog switch S_s , and (2) the voltage dependencies in the parasitic diffusion capacitors (associated with the drain/source diffusions of S_s) in parallel with C_h . Before these nonidealities can be addressed, the gain and phase must be defined.

The on-resistance of S_s is in series with the hold capacitor C_h . If the circuit is assumed linear, this switch impedance produces a single pole at $\frac{1}{r_s C_h}$. At high operating frequencies, this pole can cause a significant reduction in measured signal amplitude. The frequency response of this single pole network from V_i to V_h in Fig. 2.2-21c is as follows:

$$|A_v| \stackrel{\text{def}}{=} \left| \frac{v_h}{v_i} \right| = \sqrt{\frac{1}{1 + \frac{f^2}{f_p^2}}} \quad (2.2 - 69a)$$

$$\angle A_v = -\tan^{-1}\left(\frac{f}{f_p}\right) \quad (2.2 - 69b)$$

where

$$f_p \stackrel{\text{def}}{=} \frac{1}{2\pi r_s C_h} \quad (2.2 - 69c)$$

For the design specified in Table 2.2-12, this S/H structure has an approximate pole location of 8MHz. This response shows significant reduction in gain and shift in phase for input frequencies in the MHz range as shown in Fig. 2.2-22. If we assume that f_p for the two channels are ideally matched, then the Sampling Algorithm will cancel out this effect. Unfortunately, the frequency responses are not well matched, since the on-resistance and parasitic diffusion capacitors are both voltage dependent. This distorts the apparent pole locations as the instantaneous input voltage swings vary between its extreme values.

This effect shall be examined by a sensitivity analysis on the gain and phase expressions of Eq. (2.2-69), as follows:

$$S_{f_p}^{|A_v|} \stackrel{\text{def}}{=} \frac{\frac{\delta |A_v|}{|A_v|}}{\frac{\delta f_p}{f_p}} = \frac{\frac{f_p^2}{f^2}}{1 + \frac{f^2}{f_p^2}} \quad (2.2 - 70a)$$

$$S_{f_p}^{\angle A_v} \stackrel{\text{def}}{=} \frac{\frac{\delta \angle A_v}{\angle A_v}}{\frac{\delta f_p}{f_p}} = -\frac{\frac{f}{f_p}}{\tan^{-1}\left(\frac{f}{f_p}\right) \left(1 + \frac{f^2}{f_p^2}\right)} \quad (2.2 - 70b)$$

$$\Rightarrow \bar{S}_{f_p}^{\angle A_v} \stackrel{\text{def}}{=} \frac{\frac{\delta \angle A_v}{\pi/2}}{\frac{\delta f_p}{f_p}} = -\frac{\frac{f}{f_p}}{\frac{\pi}{2} \left(1 + \frac{f^2}{f_p^2}\right)} \quad (2.2 - 70c)$$

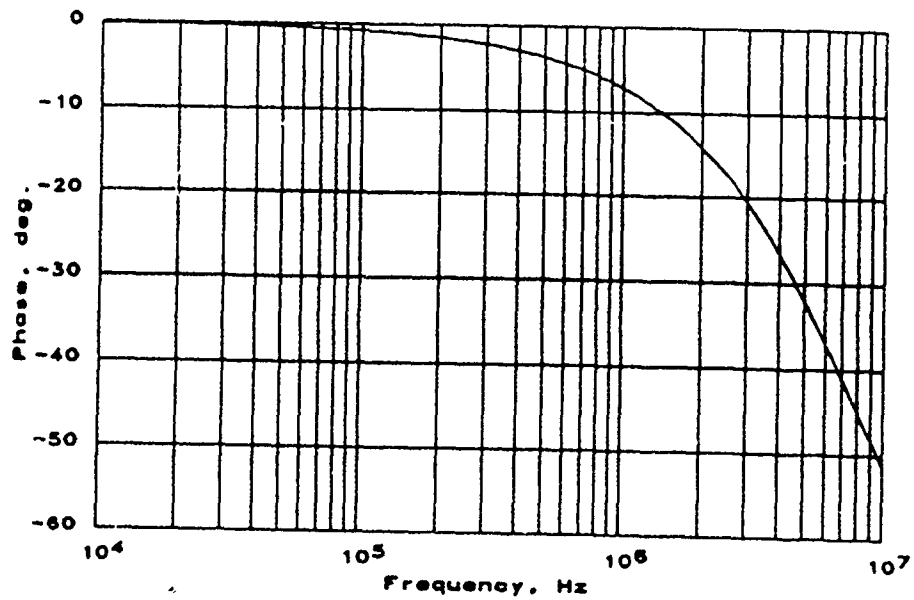
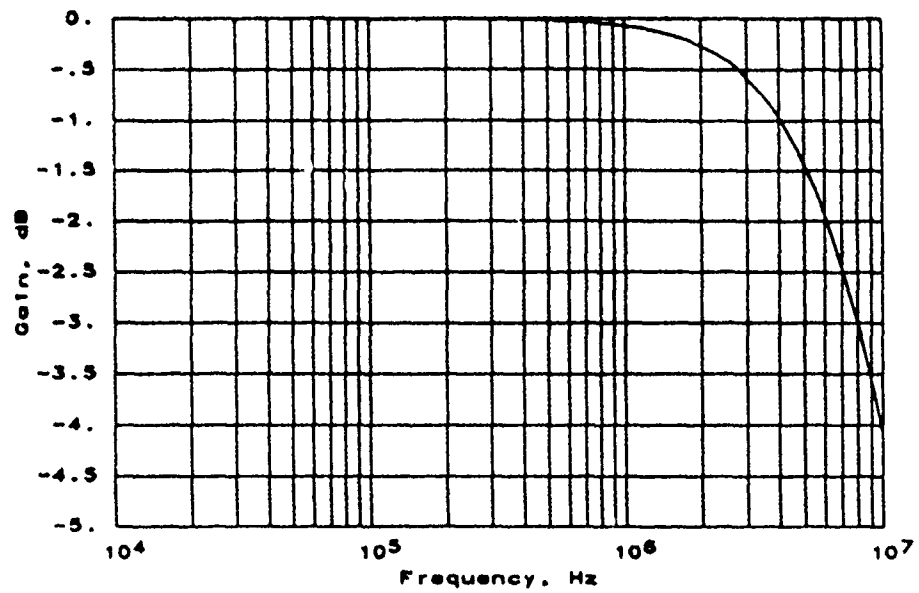


Fig. 2.2-22. BODE plot of the equivalent circuit shown in Fig. 2.2-21 for the S/H-1 operating in Track-Mode. (r_s is nominally $2.85k\Omega$ based upon device sizes contained in Table 2.2-12.)

$$S_{r_s}' = S_{C_h}' = -1 \quad (2.2 - 70d)$$

The results of this sensitivity analysis are shown in Fig. 2.2-23. Eq.(2.2-70a) represents the sensitivity of the gain $|A_v|$ with respect to movement of the pole location f_p , thus from equation Eq. (2.2-71a) below, the overall percent change in $|A_v|$ ($\Delta|A_v|$) due to changes in r_s can be estimated from the percent change in r_s (Δr_s).

$$\Delta|A_v| \approx S_{f_p}^{|A_v|} \times S_{r_s}^{f_p} \times \Delta r_s \quad (2.2 - 71a)$$

Similarly, in Eq. (2.2-70b), the sensitivity of the phase angle was computed as a function of f_p . This result is of limited use, since the ideal value of $\angle A_v$ is 0. A better indication of the effect of f_p on the phase is provided in Eq. (2.2-70c), which is normalized with respect to $\frac{\pi}{2}$ instead of the actual angle. Thus from this equation the overall variation in the phase angle in radians is

$$\Delta \angle A_v \approx \bar{S}_{f_p}^{\angle A_v} \times S_{r_s}^{f_p} \times \Delta r_s \quad (2.2 - 71b)$$

Similar expressions can be derived in terms of C_h .

Based upon the on-resistance nonlinearity analysis discussed in Section 2.2.2.3a, the on-resistance of the analog switch varies by $\pm 15\%$ from its nominal value.

$$r_s \approx 2.85k\Omega \pm 15\% \quad (2.2 - 72a)$$

The $\pm 15\%$ change shown in here is an estimation of the overall percent change in resistance because of voltage dependent effects over a $\pm 2V$ range.

The effective value of the hold capacitor including parasitic capacitances attributed to the n^+ and p^+ diffusions of the physical layout is shown in Eq. 2.2-72b.

$$C_h \approx 7pF + (50fF \pm 10\%) = 7.05pF \pm .07\% \quad (2.2 - 72b)$$

The nonlinearity contribution due to the parasitic capacitance is small compared to that due to the on-resistance.

By applying these estimates of nonlinearity to the results of the sensitivity analysis, (i.e., Eq. (2.2-71b)), we find that at 5MHz the corresponding gain jitter is in the range of 13-14%, as shown in Fig. 2.2-24. Shown here is the approximate gain error due to nonlinearities as a function of input-frequency. Note the near linear relationship between the input-frequency and the percent error in gain, approximated by the expression shown in Eq. (2.2-73).

$$\frac{\Delta||A_v||}{|A_v|} \approx 3.75f \left(\frac{\%}{MHz} \right) \quad (2.2 - 73)$$

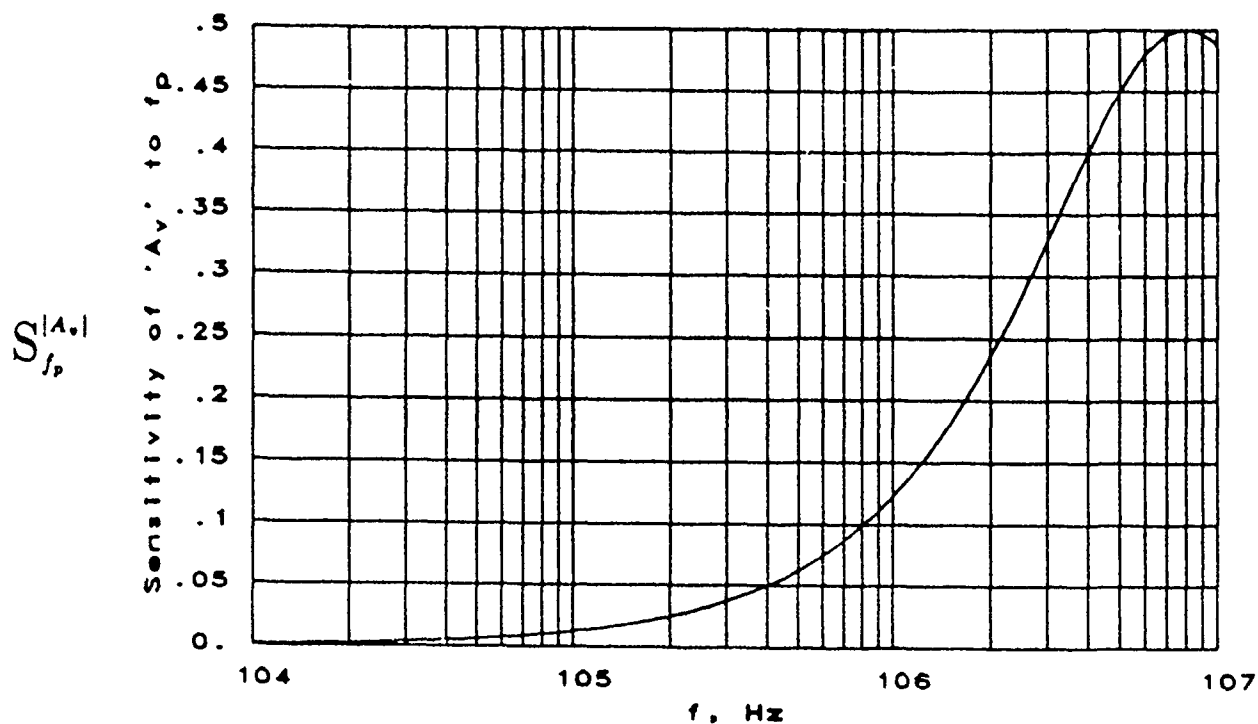


Fig. 2.2-23a. Plot of gain sensitivity as function of pole location f_p , as mathematically represented in Eq. 2.2-70a for $f_p = 8MHz$.

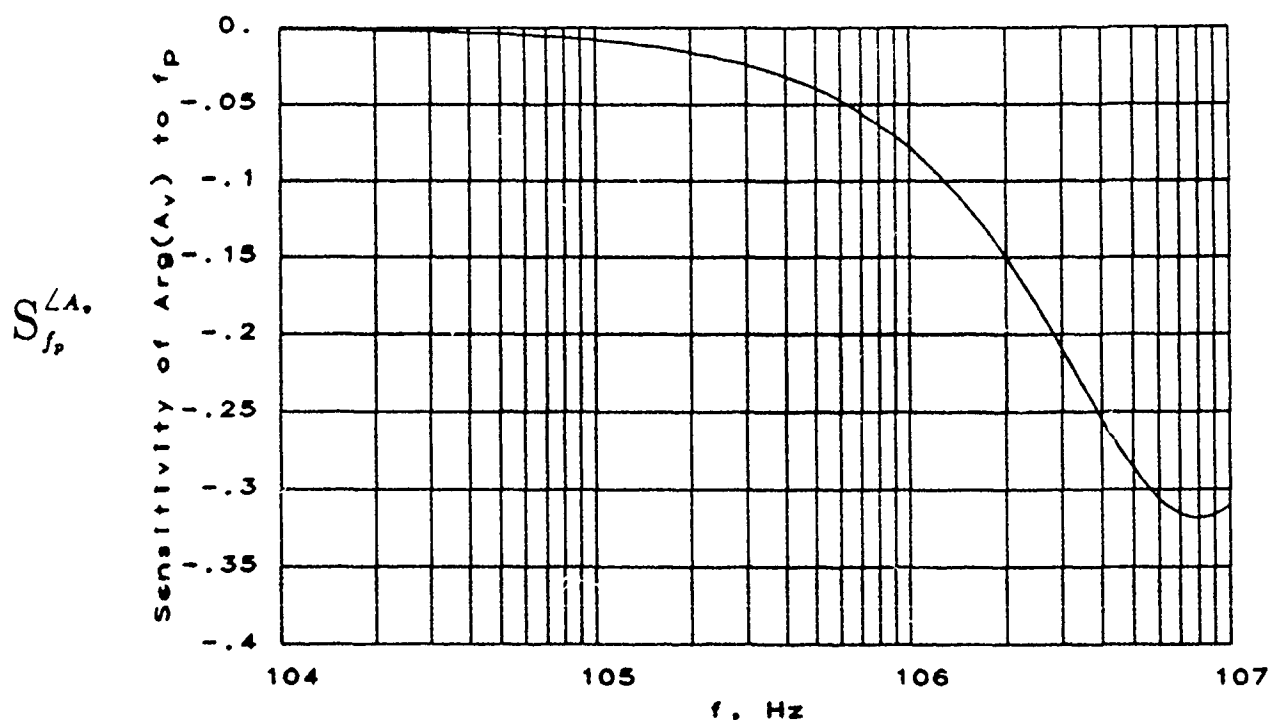


Fig. 2.2-23b. Plot of normalized phase sensitivity as function of pole location f_p , as mathematically represented in Eq. 2.2-70c for $f_p = 8MHz$.

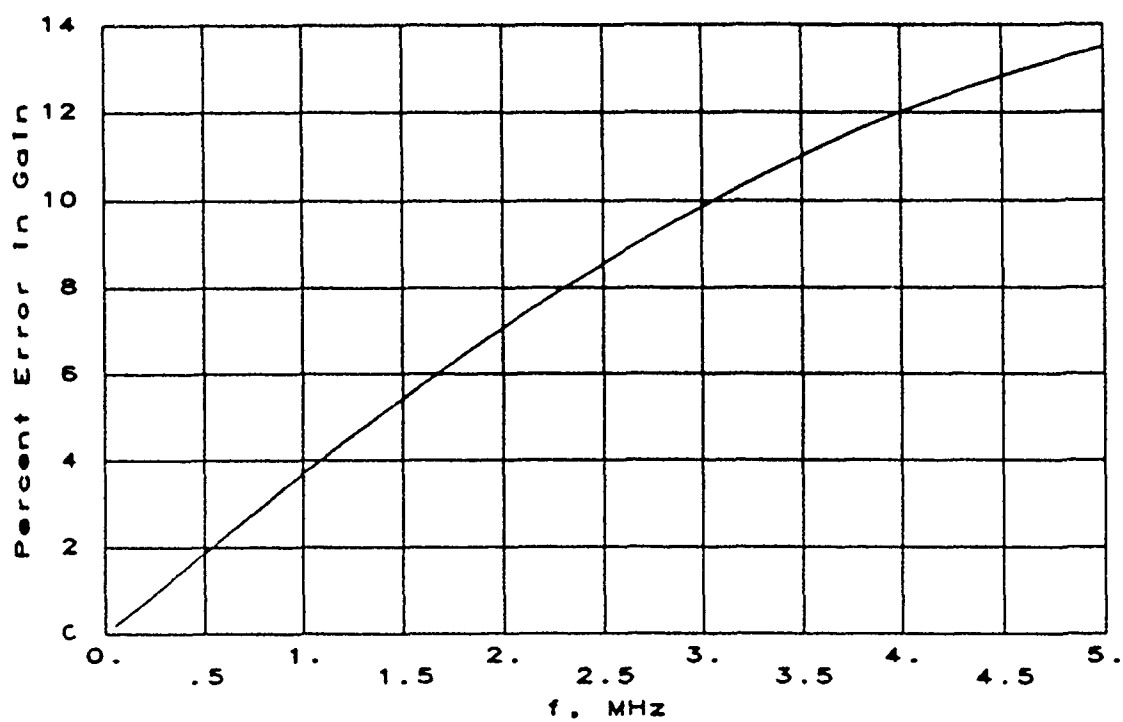


Fig. 2.2-24 Plot of switch nonlinearity inducing errors in the track-mode gain $|A_v|$ for S/H-1 as a function of input-frequency. (Assuming $f_p = 8\text{MHz}$)

One way to reduce this error term is by increasing the channel-widths of both the n- and p-channel pass-transistors in the analog switch S_a . This unfortunately will also increase the clock feed through and the parasitic capacitance nonlinearity.

Sampling-Transition

The primary contributor to sampling transition related errors and the only one considered here, is the clock feedthrough generated by switching S_a "off". This feedthrough component is proportional to the size of the pass-transistor devices, as discussed in Section 2.2.2.3a. From this discussion it was concluded that the worstcase variation in this offset voltage was estimated as that shown in Eq. (2.2-67). Thus for the specific device sizes as listed in Table 2.2-12, the overall *worstcase* clock feedthrough error would be $\pm 0.5\%$ relative to the full scale input voltage range. Optimistically, this error is expected to be in the range of $\pm 0.1\%$ to $\pm 0.25\%$, since there is some cancellation effects of the complimentary switch, and from the capacitor C_1 .

Hold-Mode

There are two error sources that contribute to the overall sampling error, once the S/H is in hold mode: (1) the leakage current associated with the source/drain diffusions attached to the top plate of the hold capacitor, and (2) the input offset voltage of the buffer adding an offset to the overall output voltage V_o .

For this particular process the leakage current is directly proportional to the area of the diffusions connected to the top plate of the hold capacitor, as discussed in Section 2.2.2.3a. For the device sizes used in this particular design, the leakage current has been estimated at 14pA based upon Eq. (2.2-68a). This causes the hold voltage to drift at a rate of $2.1 \frac{\mu\text{V}}{\mu\text{sec}}$. That can be related to a 0.05% error relative to a full scale $4V_{p-p}$ input signal in a 1msec. time frame. This is much longer than the amount of time required for the A/D to convert this sample and held signal to a digital output word.

The offset voltage is signal independent and can be easily canceled by the Sampling Algorithm and will not be considered here.

Conclusions:

Based upon the above performance analysis, the S/H-1 cell was determined to have three dominate performance limitations, (1) the nonlinearity originating from the voltage dependent on-resistance of S_a which increased linearly with frequency; and (2) the nonlinearity induced by the voltage dependent clock feedthrough of S_a which contributed approximately 0.5% error relative to a full scale input voltage (3) the frequency dependence of the gain. During the design process of the S/H-1 cell the clock feedthrough error was fixed at 0.5% , thus determining the device sizes shown in Table 2.2-12, and also determin-

ing the frequency dependent on-resistance error component such that at approximately 125kHz this error term will contribute the same amount of error as the clock feedthrough component (0.5%). This yields an effective 8-bit accuracy at low frequencies, a 7-bit accuracy at 125kHz , and a 6-bit accuracy at 400kHz , in terms of the final digital word length generated by an external A/D.

The major inherent design limitation of this architecture is that the two aforementioned nonlinearities have conflicting design criterion. Nonlinearities in the on-resistance of S_s decrease with the size of the hold capacitor whereas clock feedthrough effects increase with C_h .

2.2.2.3c Sample/Hold-2

Driven by the frequency limitations of the S/H-1 architecture, the following architecture was developed based upon feedback, null-port, and offset voltage cancellation techniques. The S/H structure discussed here (1) cancels out the input offset voltage of the OpAmp, (2) improves the frequency response of the S/H in the track-mode by reducing the on-resistance of the sampling switch, and (3) minimizes the voltage dependency in the clock feedthrough thus reducing this nonideality to a small DC offset voltage, which can be cancelled out by the Sampling Algorithm. This S/H is referred to as S/H-2.

The basic architecture and its inherent performance limitations are described below. Corresponding experimental results are presented in Section 5.13.

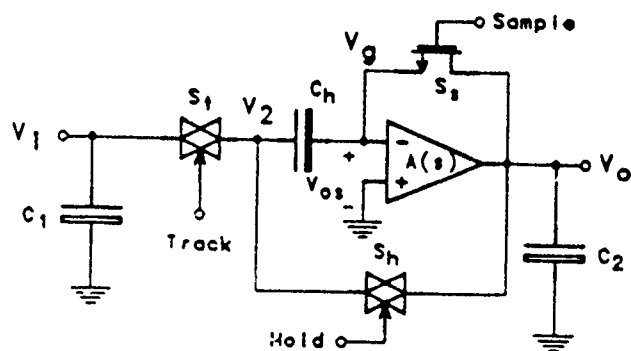
Description:

A block diagram for the S/H-2 cell is shown in Fig. 2.2-25a with its associated timing diagram contained in Fig. 2.2-25b. The operation of this circuit is as follows.

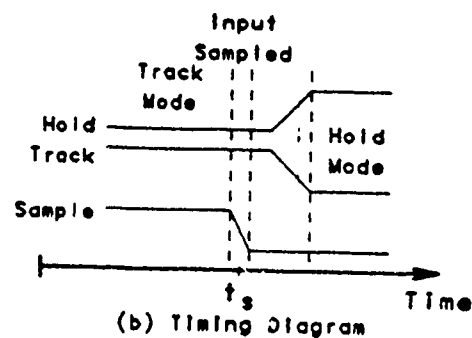
Consider initially the circuit in the track-mode in which the "track" switch S_t and "sampling" switch S_s are both closed and the "hold" switch S_h is open. If we model the S_t and S_s switches which are "on", as voltage dependent on-resistances, denoted as r_t and r_s respectively, then the operation of this circuit is depicted by the equivalent circuit shown in Fig. 2.2-25c. In the track mode, the negative input terminal of the OpAmp is biased at the offset voltage of the OpAmp V_{OS} , thus in steady state and at low frequencies (where r_t and r_s are negligible), v_H is equal to the input voltage minus the offset voltage of the OpAmp, i.e.,

$$v_H(t) = v_I(t) - V_{OS} \quad (2.2 - 74)$$

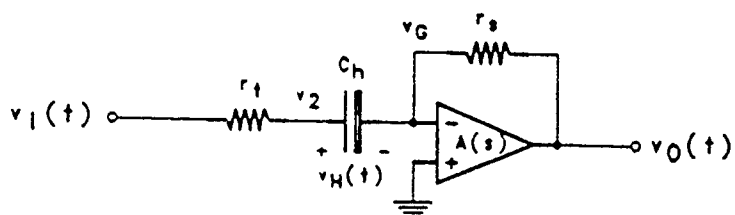
Now if the switch S_s is opened at time t_s , the bottom plate of the hold capacitor C_h is electrically isolated and the input voltage v_I is essentially "sampled". Note that when S_s was opened charge is injected on to the bottom plate of the hold capacitor, but fortunately this clock feedthrough component is independent of the input voltage, since the potential on either side of the switch is ideally zero.



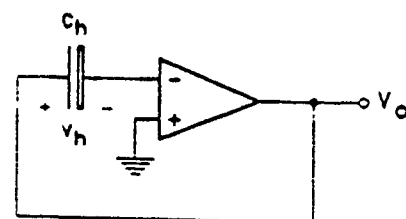
(a) Circuit Schematic



(b) Timing Diagram



(c) Track Mode Equiv. Circuit



(d) Hold Mode Equiv. Circuit

Fig. 2.2-25. S/H-2

Now with S_i open and C_h isolated (in particular from any clock feedthrough components) the top plate of the capacitor is disconnected from the input signal by opening the "tracking" switch S_t , and then connected to the output by closing the "holding" switch S_h . This places the S/H in the hold-mode, with the so called "sampled" input signal buffered and available on the V_O node, as shown in the equivalent circuit in Fig. 2.2-25d. Thus the expression for the output voltage is

$$V_O(t) = v_H(t_s) + V_{OS} = v_I(t_s) - V_{OS} + V_{OS} = v_I(t_s) \quad \text{for } t > t_s \quad (2.2 - 75)$$

Notice that this architecture is intrinsically independent of the OpAmp input offset voltage, and that the finite on-resistance of the S_h switch is not considered here, since the output signal at this point is essentially DC.

The analog switch S_i is a single n-channel MOSFET, while the other two switches, S_t and S_h are the regular complimentary switches who's circuit schematic is provided in Fig. 2.2-11c. The device sizes for these analog switches and the other S/H components are shown in Table 2.2-13. The two capacitors C_1 and C_2 were added to the circuit to reduce clock feedthrough.

Obviously this structure was not designed strictly to cancel offset problems associated with the OpAmp. Its primary benefit is that it reduces the high-frequency track-mode nonlinearities associated with the analog switches and thus allows the S/H to more accurately track the input signal. More specifically analysis of the track-mode equivalent circuit shown in Fig. 2.2-25c, assuming the open-loop gain of the OpAmp is frequency independent of value A , yields a single pole at

$$\omega_p = \frac{1}{(r_t + \frac{r_t}{1+A}) C_h} \quad (2.2 - 76)$$

Note, the on-resistance of the r_t switch can be greatly decreased since it is no longer constrained in size by the clock feedthrough phenomenon affecting the hold capacitor. Furthermore the *effective* on-resistance of r_s is reduced drastically by the open-loop gain of the OpAmp, as is inherent in this architecture.

These aspects of the design will be discussed in more detail in the following performance limitations section.

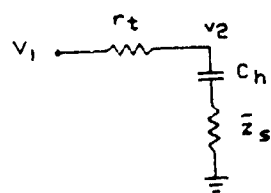
Performance Limitations:

This S/H architecture was designed in accordance with DCASP-2, thus the intended input signal swing and maximum input frequency was $\pm 2V$ and $5MHz$. The performance limitations of this architecture shall be broken down into three classifications, track-mode, sampling transition, and hold-mode limitations.

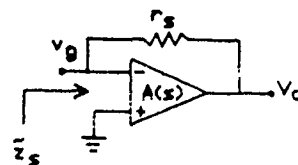
Track-Mode

Table 2.2-13. Device sizes and component values for S/H-2 circuit schematic of Figures 2.2-25a.

Component	n-channel		p-channel		Value
	<i>W</i>	<i>L</i>	<i>W</i>	<i>L</i>	
S_s	$12\mu m$	$3\mu m$			
S_t	$9\mu m$	$3\mu m$	$23\mu m$	$3\mu m$	
S_h	$9\mu m$	$3\mu m$	$23\mu m$	$3\mu m$	
C_1					$5pF$
C_2					$5pF$
C_h					$1.5pF$



(a) reduced track-mode
equivalent circuit.



(b) \bar{z}_s OpAmp circuit

Fig. 2.2-26. Circuit schematics for frequency-domain analysis of S/H-2 in track-mode.

To better understand how the high-frequency track-mode nonidealities associated with the finite switch on-resistances and the finite frequency response of the OpAmp limits the ability of this circuit to track the input signal v_I , consider the following high frequency analysis of the track-mode equivalent circuit, as shown in Fig. 2.2-25c.

In this circuit the role of the OpAmp is to provide a low impedance point to ground for the bottom plate of the hold capacitor via the null port across the input nodes of the OpAmp when feedback is present. Electrical isolation of the bottom plate of the hold capacitor is achieved when feedback is removed. Thus, in the track-mode the circuit shown in Fig. 2.2-25c can be reduced to that shown in Fig. 2.2-26a, where \tilde{z}_s corresponds to the frequency dependent input-impedance of the OpAmp circuit shown in Fig. 2.2-26b or rather

$$\tilde{z}_s = \frac{r_s}{1 + A(s)} \quad (2.2 - 77)$$

where $A(s)$ represents the finite frequency dependent open-loop gain of the OpAmp. If we assume a single pole model for the OpAmp and a large open-loop gain, such that

$$A(s) = \frac{GB}{s} \quad (2.2 - 78a)$$

then \tilde{z}_s can be written as follows:

$$\tilde{z}_s(s) = \frac{r_s s}{1 + \frac{s}{GB}} \quad (2.2 - 78b)$$

Comments:

- At low frequencies ($\omega \ll GB$), \tilde{z}_s looks inductive,
- At high frequencies ($\omega \gg GB$), \tilde{z}_s looks resistive and approaches the value r_s ,
- range: The magnitude of \tilde{z}_s is bounded such that $0 \leq |\tilde{z}_s| \leq r_s$,
- $|\tilde{z}_s|$ is a monotonically increasing function of frequency.

Thus the frequency dependent expression for the voltage gain between the input signal and the AC signal across v_h is

$$A_v \stackrel{\text{def}}{=} \frac{v_h(s)}{v_i(s)} = \frac{\frac{1}{\omega_z} (s + \omega_z)}{\frac{1}{\omega_o^2} (s^2 + BWs + \omega_o^2)} \quad (2.2 - 79a)$$

where

$$\omega_z = GB \quad (2.2 - 79b)$$

$$\omega_o = \sqrt{\frac{GB}{(r_t + r_s) C_h}} \quad (2.2 - 79c)$$

$$BW = \frac{1 + GB (r_t C_h)}{(r_t + r_s) C_h} \quad (2.2 - 79d)$$

The frequency response shown above consists of a zero at the Gain-Bandwidth product of the OpAmp (GB) and pair of complex poles related by a relationship involving GB , r_s , r_t , and C_h . To obtain a practical perspective of these limitations, typical values for the parameters will be assumed. These typical parameters are

$$GB \approx 2\pi(30MHz) \quad (2.2 - 80a)$$

$$r_s \approx 3.2k\Omega \quad (2.2 - 80b)$$

$$r_t \approx 1.5k\Omega \quad (2.2 - 80c)$$

$$C_h \approx 1.5pF \quad (2.2 - 80d)$$

and are based upon the device sizes shown in Table 2.2-13 and the physical OpAmp design documented in Section 2.2.2.3e. From these nominal values the transfer function characteristics are as follows:

$$\omega_z = 2\pi(30MHz) \quad (2.2 - 81a)$$

$$\omega_o = 2\pi(25MHz) \quad (2.2 - 81b)$$

$$BW = 2\pi(32MHz) \quad (2.2 - 81c)$$

Note the poles of this transfer function are complex with an associated pole Q of $\frac{3}{4}$. This transfer function is graphically represented in the BODE plots contained in Figs. 2.2-27a and 2.2-27b. This frequency response shows a notable change in slope of both curves in the 6 - 7MHz range, which implies a higher sensitivity to nonlinear components above these frequencies. Also observe that this frequency response represents almost an order of magnitude improvement over the frequency response of S/H-1 which was shown in Fig. 2.2-26.

Nonlinear Distortion

The results presented thus far are based upon the theoretical linearized track-mode frequency response. The term "linearized" refers to the use of nominal or zero-biased value for the voltage dependent components of the S/H design. The nonlinear effects of these components have not yet been considered. The following analysis will address these nonlinearities and show how these errors propagate through the Sampling Algorithm (as discussed in Section 2.2.1.1), and thus affect the overall obtainable accuracy of the Performance Measurement System.

Consider the following theoretical test system as shown in Fig. 2.2-28. This test setup consists of two identical S/H's, one sampling a sinusoidal input signal $v_I(t)$, and the other sampling a signal $v_O(t)$ which is equal in amplitude to v_I but shift in phase by some "random" quantity θ , i.e.,

$$v_I(t) = 2\sin(2\pi ft) \quad (2.2 - 82a)$$

$$v_O(t) = 2\sin(2\pi ft + \theta) \quad (2.2 - 82b)$$

where f corresponds to the input-frequency. Thus the ideal transfer function $v_o(s)/v_i(s)$ is unity gain with a phase of θ .

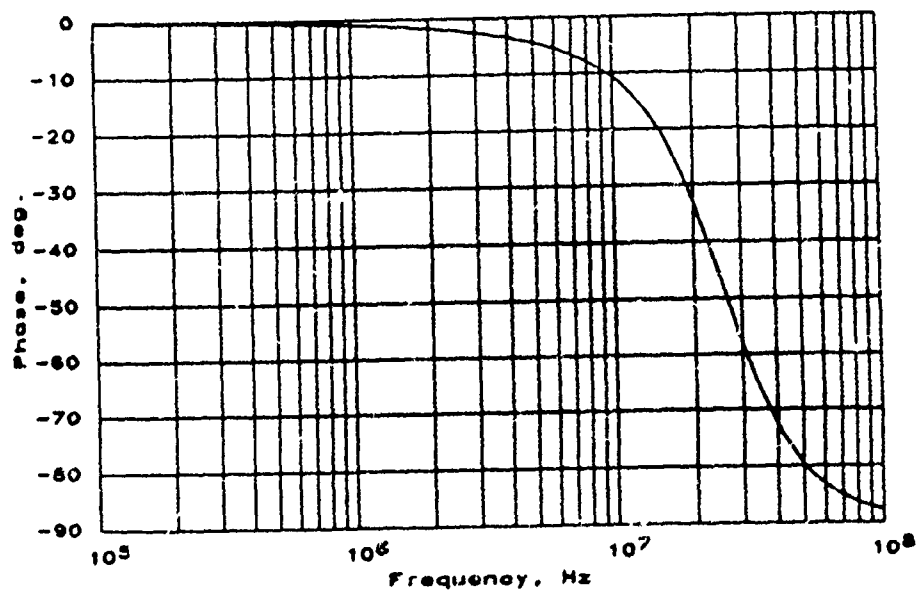
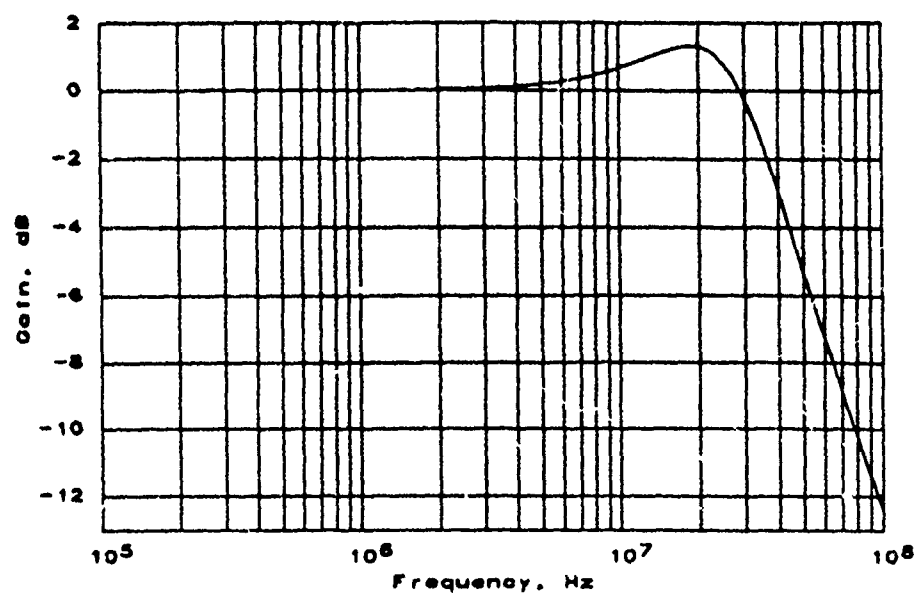


Fig. 2.2-27a. Frequency response of $v_h(s)/v_i(s)$ as contained in Eqs. (2.2-79) through (2.2-81) representing the S/H-2 operating in track-mode.

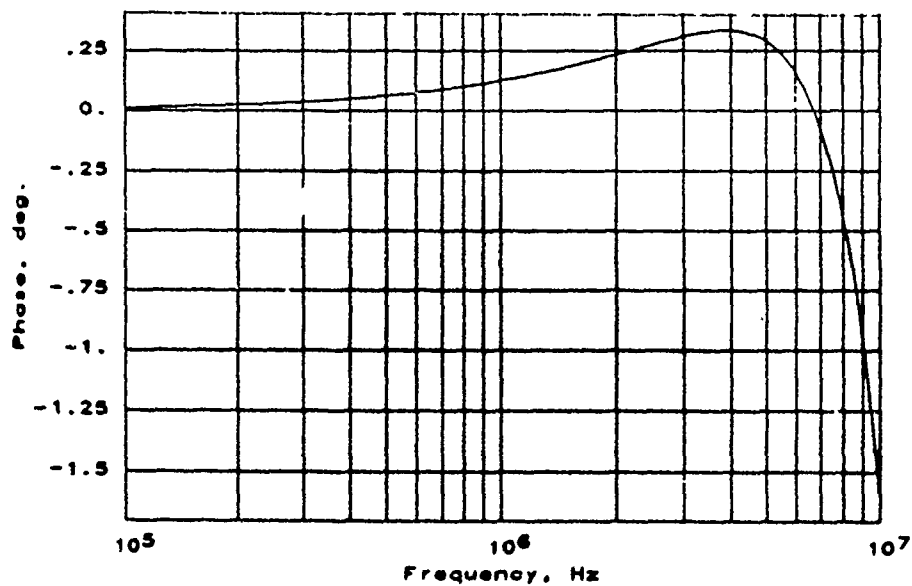
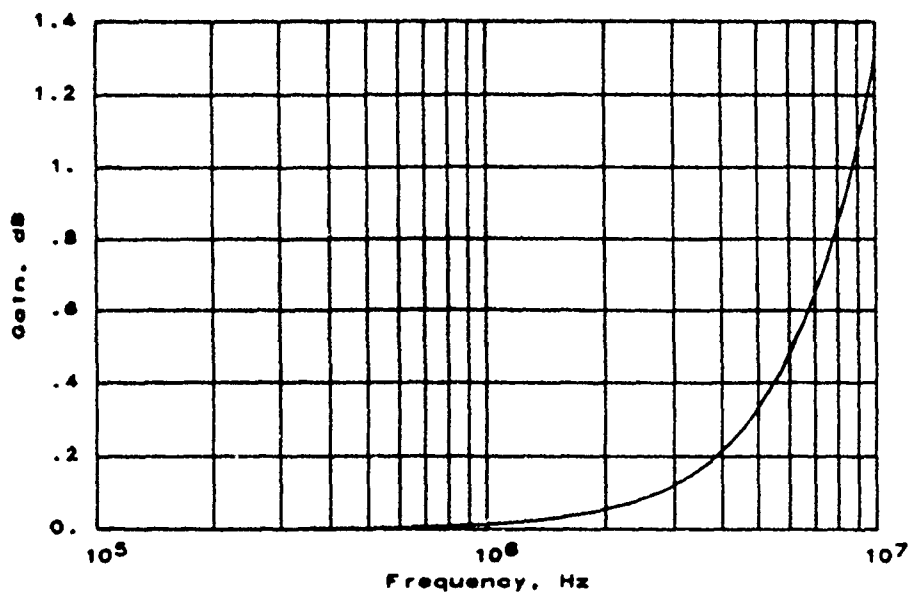


Fig. 2.2-27b. Zoomed in version of the S/H-2 track-mode BODE plot contained in Fig. 2.2-27a — focusing on the gain and phase distortion in the 5 – 10MHz range.

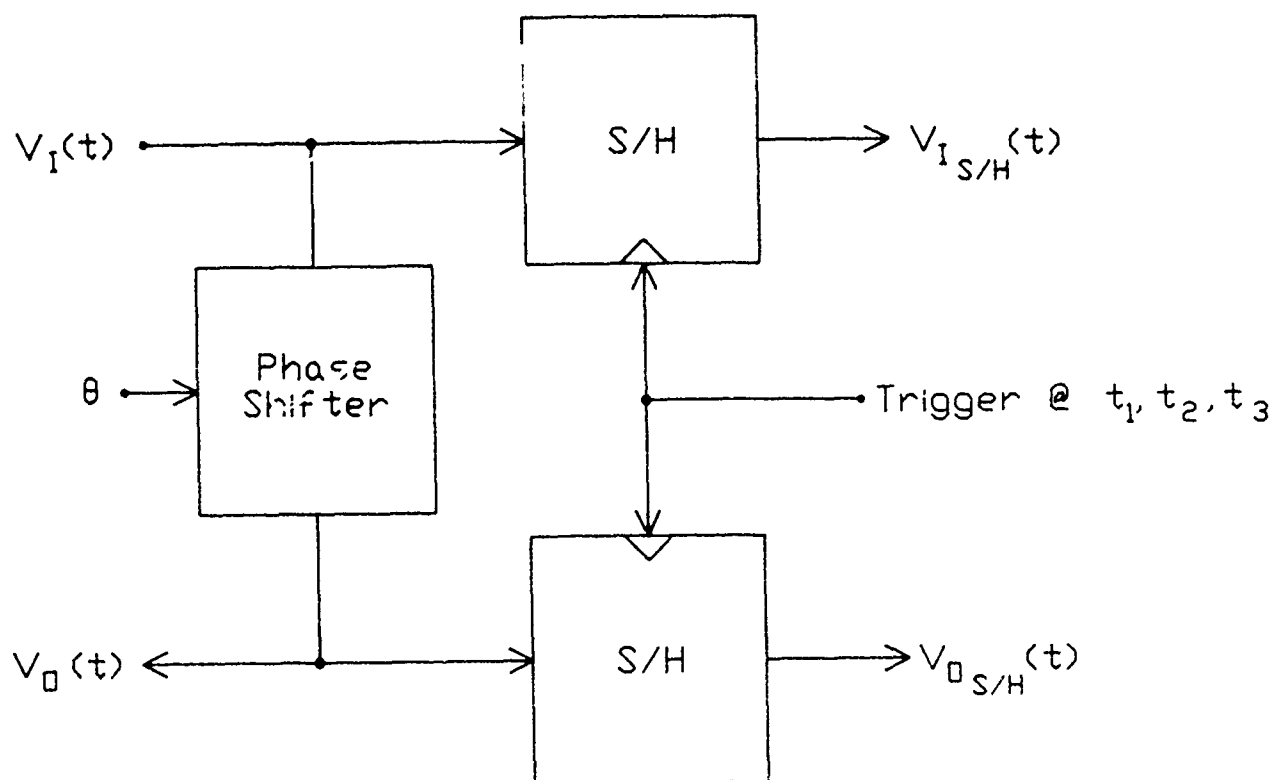


Fig. 2.2-28. Test configuration for simulating the Performance Measurement System's accuracy as a function of the track-mode nonlinearities of the S/H.

Now if we collect three sets of instantaneous and simultaneous samples of the input and output waveforms at random intervals, (i.e., $(v_{I/A}(t), v_{O/A}(t))$, for $t = t_1, t_2, t_3$) via the S/H's assuming they are ideal except for track-mode nonlinearities; then the gain and phase of the phase shifter as viewed by the nonideal S/H's can be computed from the Sampling Algorithm discussed in Sec. 2.2.1.1. Thus any deviation in gain from 0dB and phase from θ is interpreted as error contributed by these nonlinearities into the computed gain and phase of the Performance Measurement System — thus localizing these error terms.

Since the computed gain and phase by the Sampling Algorithm may inherently be dependent upon the specific phase shift θ and the exact time instances of the samplings t_1, t_2 and t_3 , these parameters were randomized and varied over a wide range as constrained by Eq (2.2-83). Thus if the worstcase computed gain and phase measurements were recorded over this range of test setup characteristics then any θ dependence or time sampling dependence will be removed from the simulation.

$$t_1 = \frac{\phi - 85^\circ}{2\pi f}, t_2 = \frac{\phi}{2\pi f}, t_3 = \frac{\phi + 85^\circ}{2\pi f} \quad \text{for } 0^\circ \leq \phi \leq 180^\circ \quad (2.2 - 83a)$$

$$0^\circ \leq \theta \leq 180^\circ \quad (2.2 - 83b)$$

As shown here, the three sample points are stongly correlated, but randomly aligned to the input and output waveforms via a random phase angle ϕ . The 85° interval between sample points was selected as a worstcase situation, such that for a so called "worstcase ϕ ", one sample point will be near the $+2V$ rail, one near $0V$ and one near the $-2V$ rail, thus resulting in a large variation in the voltage dependent nonlinearities between samples. Note a 90° sampling interval might be a more obvious selection, but this results in dependent samples and prevents the Sampling Algorithm from converging. The term "worstcase ϕ " refers to varying ϕ between 0° and 180° and recording the worstcase gain and phase measurement.

The primary nonlinear components being considered here are the two nonlinear on-resistance r_t and r_s , and the nonlinear junction capacitor (c_t) associated with the source/drain diffusions of S_t which is in parallel with the hold capacitor C_h . These three nonlinearities shall be modelled as follows:

$$\tilde{r}_t \stackrel{\text{def}}{=} r_{t_0} (1 + m_t v_I) \approx 1.5k\Omega (1 + 0.125v_I) \quad (2.2 - 84a)$$

$$\tilde{r}_s \stackrel{\text{def}}{=} r_{s_0} (1 + m_s v_G) \approx 3.2k\Omega (1 + 0.51v_G) \quad (2.2 - 84b)$$

$$c_t \stackrel{\text{def}}{=} f(v_I) \quad (2.2 - 84c)$$

where r_{t_0} and r_{s_0} represent the nominal values for these on-resistances as shown in Eq. (2.2-80); m_t represents a 50% variation in the on-resistance of the track-mode switch S_t over $\pm 2V$ operating range; m_s models the voltage dependence of the n-channel analog switch based upon those results presented in Table 2.2-10; v_G is the instantaneous potential on the negative-input of the OpAmp; f is a complex function involving the area and

perimeter of the p^+ and n^+ diffusions of the pass-transistors of S_t as discussed in Section 2.2.2.3a. This nonlinearity can be computed from Eq. (2.2-58), assuming both the area and perimeter of the n^+ and p^+ diffusions are equal and computed from the p-channel width of $23\mu\text{m}$ by Eqs. (2.2-59c) and (2.2-59d).

The results of this simulation are shown in Figs. 2.2-29 and 2.2-30, and summarized in Table 2.2-14. At low frequencies (sub-MHz) the nonlinearities discussed here contribute very little to the overall performance of the S/H. For frequencies greater than 6 - 7 MHz the errors induced by these nonidealities increase exponentially.

One last error term not discussed above, is that at high frequencies the on-resistance of S_s becomes even more voltage dependent than modelled by (2.2-84b), since the OpAmp will try to drive more current through the switch by increasing the output voltage (V_o of Fig. 2.2-25). Thus there is a strong possibility of driving S_s into weak inversion or possibly even saturation. If this occurs then the effective impedance \tilde{z}_s will look more like a current source than an impedance. The advantages and disadvantages of this effect will not be examined at this time.

Sampling Transition

This S/H architecture inherently reduces the clock feedthrough problem for the following reasons:

- (1) A simple n-channel analog switch can be used for S_s rather than a complimentary switch. Thus reducing the parasitic coupling capacitance between the clock *sample* and the signal path.
- (2) S_s can be sized much smaller than normally required because of the feedback techniques used here, thus further reducing the parasitic coupling capacitance and associated charge injection.
- (3) The charge stored in the channel of S_s is essentially constant since the charge injection side of the switch (the side attached to the hold capacitor) is tied to a null-port of an OpAmp and should be held at ground. This reduces the voltage dependency of the clock feedthrough problem, for this switch.
- (4) The bottom plate is electrically isolated when the switches S_t and S_h are opened and closed respectively. Furthermore, the charge injected by S_t should be absorbed by S_h since the switches, clock signals and source and drain load impedances are finely matched.

Based upon the above comments the primary contributor to sampling transition related errors and the only one quantized here, is the clock feedthrough generated by switch-

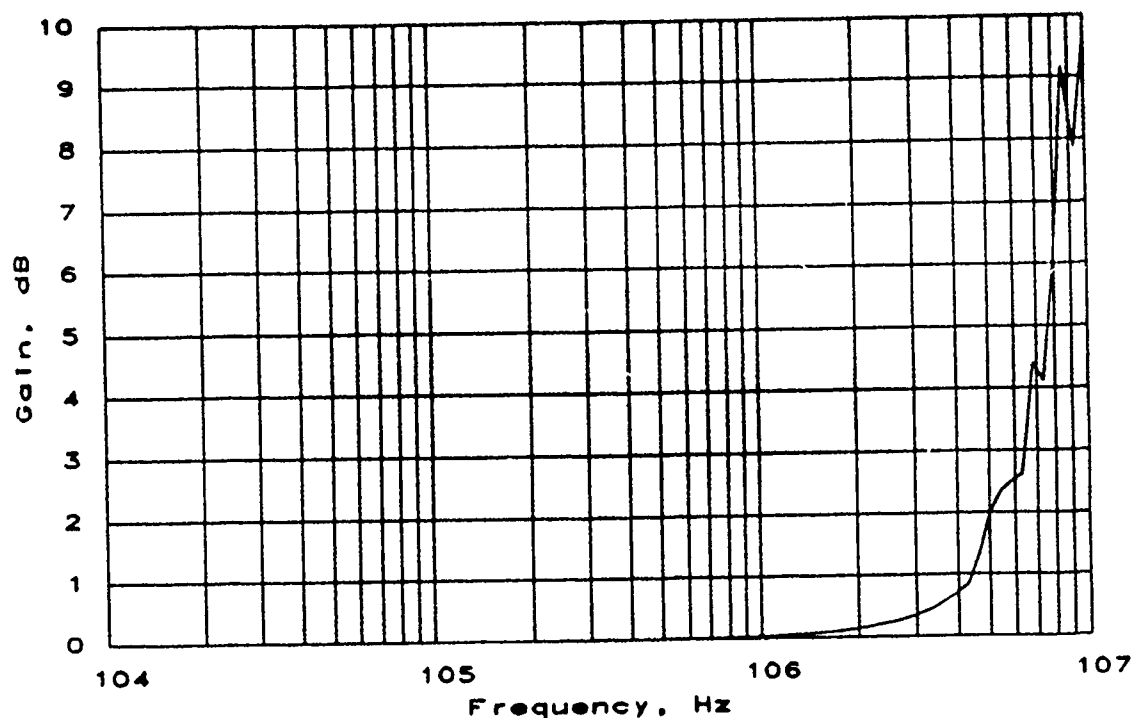


Fig. 2.2-29 Plot of predicted gain measurement error via errors induced into the Sampling Algorithm from track-mode nonlinearities in S/H-2. Specifically this is a plot of the extracted $|v_o(s)/v_i(s)|$ — ideally unity gain.

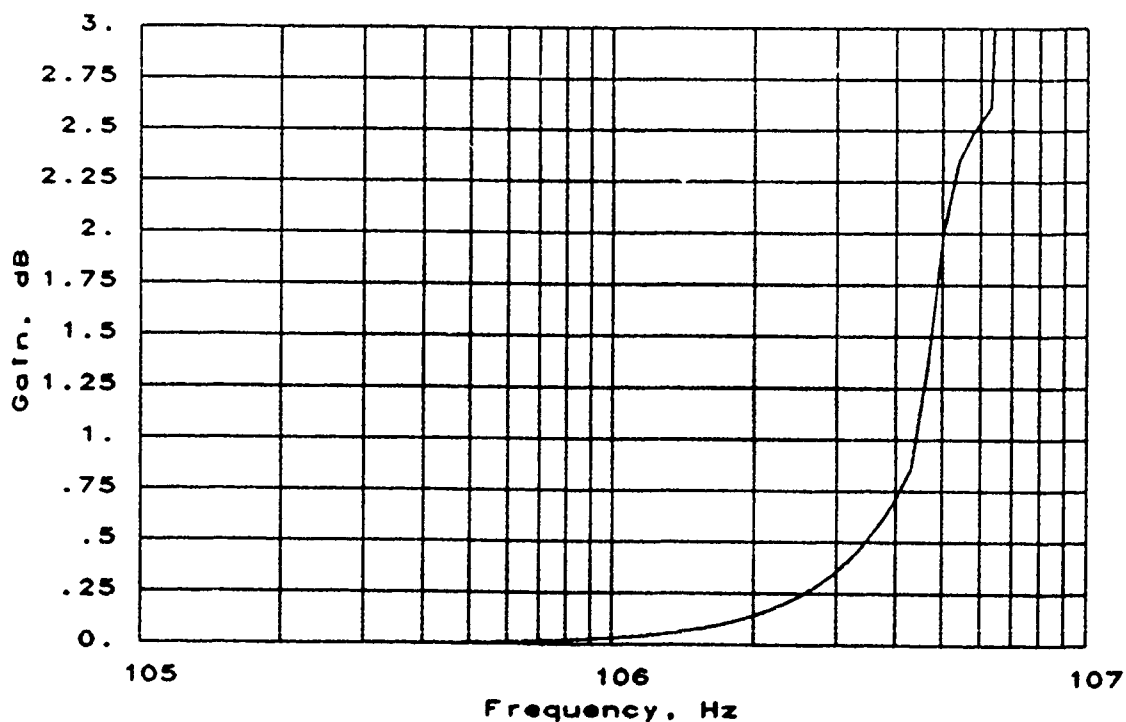


Fig. 2.2-29b Zoomed in version of Fig. 2.2-29a, focusing in on the 2 - 5 MHz range.

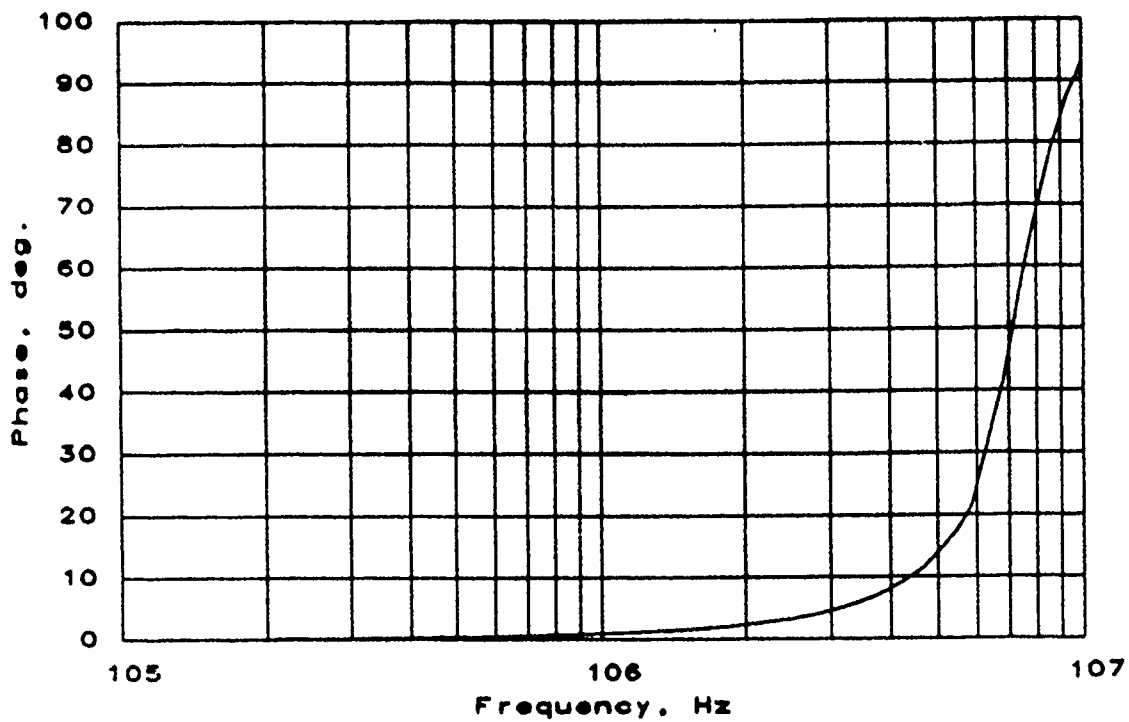


Fig. 2.2-30a Plot of predicted phase measurement error via errors induced into the Sampling Algorithm from track-mode nonlinearities in S/H-2. Specifically this is a plot of the extracted $(\angle(v_o(s)/v_i(s)) - \theta)$ — ideally zero.

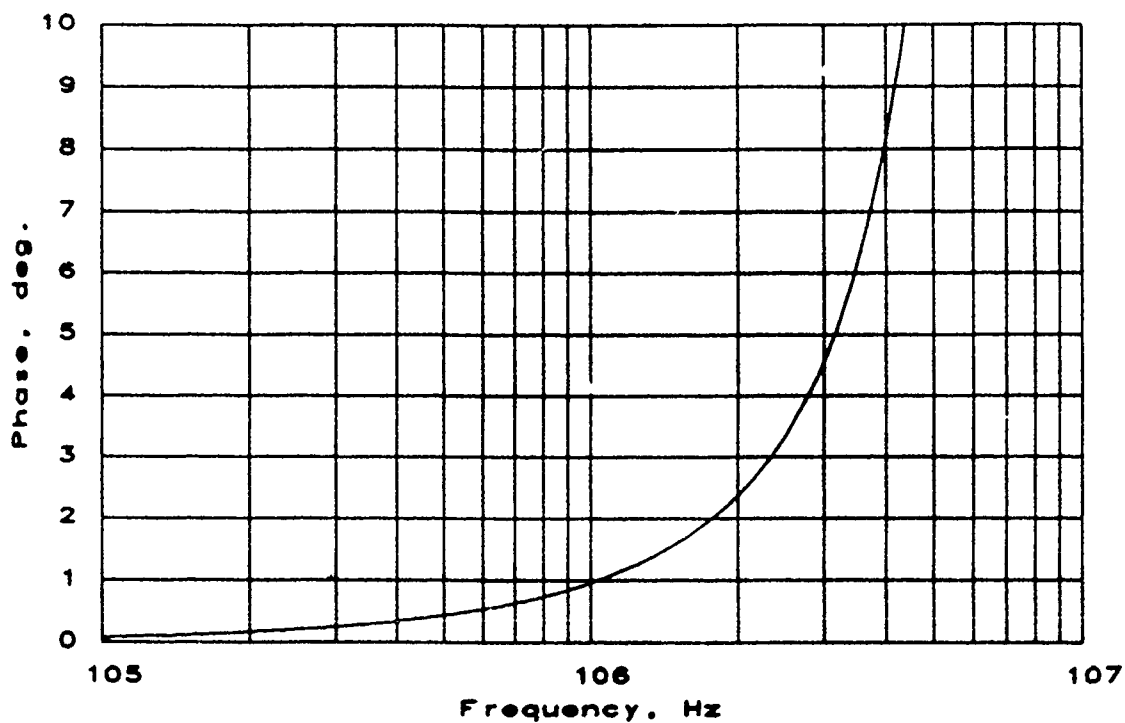


Fig. 2.2-30b Zoomed in version of Fig. 2.2-30a, focusing in on the 2 – 5MHz range.

Table 2.2-14. Summary of the simulation results presented in Figs. 2.2-29 and 2.2-30 of the errors induced in the extracted gain and phase by the Sampling Algorithm due to the track-mode nonlinearities of the S/H-2 circuit.

frequency	$\left \frac{v_o(s)}{v_i(s)} \right (dB)$	$\angle \left(\frac{v_o(s)}{v_i(s)} \right) - \theta$
10kHz	0.00006	0.0073°
100kHz	0.00047	0.074°
200kHz	0.00066	0.15°
500kHz	0.0065	0.40°
1MHz	0.031	0.87°
2MHz	0.14	2.1°
5MHz	2.0	13.°
10MHz	9.7	83.°

ing S_1 "off". This feedthrough component is proportional to the size of the pass-transistor devices, as discussed in Section 2.2.2.3a. From this discussion it was concluded that the worstcase variation in this offset voltage was estimated as that shown in Eq. (2.2-67). Thus for the specific device sizes as listed in Table 2.2-13, the overall worstcase clock feedthrough error would be approximately $\pm 0.8\%$ relative to a estimated worstcase variation of $\pm 0.5V$ in the instantaneous potential v_G of Fig. 2.2-25. The actual expected error is anticipated to be at most $\frac{1}{2}$ to $\frac{1}{3}$ of this value, since the actual variation in v_G is not anticipated to be this large, and the capacitor C_2 should provide some relief by absorbing some of this charge.

One interesting consequences of this architecture, is that the voltage dependence of the clock feedthrough component is frequency dependent, and for low frequencies this architecture is insensitive to this nonlinear effect and thus can be treated completely as a fixed DC offset.

Hold-Mode

Once in the hold-mode, only the leakage current associated with the source/drain diffusions attached to the top and bottom plate of the hold capacitor affect the overall sampling error of the S/H.

For this particular process the leakage current is directly proportional to the smallest area of the diffusions connected to either the top plate or bottom plate of the hold capacitor, as discussed in Section 2.2.2.3a. For the device sizes used in this particular design, the leakage current has been estimated at $21pA$ based upon Eq. (2.2-68a). This causes the hold voltage to drift at a rate of $10.5 \frac{\mu V}{\mu sec}$. That can be related to a 0.25% error relative to a full scale $4V_{p-p}$ input signal in a $1msec.$ time frame. This represents more than adequate time for the A/D to convert this sample and held signal to a digital word.

Conclusions:

Based upon the above performance analysis, the S/H-2 cell had a substantial reduction in error at higher frequencies over the previous design, S/H-1, but there were several underlying design limitations as listed below.

- (1) At higher frequencies, as the OpAmp started to roll off the effective on-impedance of \tilde{z}_s started increasing rapidly, thus increasing the overall impact of this nonlinearity drastically. Furthermore, increasing the effective on-impedance implies that the null-port is starting to breakdown (v_G to float away from ground) thus allowing more fluctuation in the voltage dependent component of this impedance, and thus inducing even more nonlinearities. Unfortunately the current OpAmp bandwidth of $30MHz$ is near state-of-the-art limits.

- (2) The finite voltage-dependent on-resistance of S_t distorted the track-mode operation of this S/H at higher frequencies when the null-port started to dysfunction. Unfortunately the current on-resistance and device sizes of this switch, can not be increased without sacrificing nonlinearity due to the voltage dependence of the clock feedthrough generated by this switch. With the current design values the estimated nonlinearity due to this clock feedthrough component is already 0.5% to 1% at high frequencies, and can not afford to be increased any more.
- (3) The finite voltage-dependent on-resistance of S_t also distorted the track-mode operation of this S/H at higher frequencies because of the RC time constant formed by r_t and C_h attenuated the amount of input signal across the hold capacitor. Thus modulation of this RC time constant by the instantaneous value of the input-signal, distorts the hold voltage. Obviously then it would be desired to decrease this on-resistance by increase the channel-width of the pass-transistors of this device, but this would increase the parasitic junction capacitor associated with the source/drain diffusions of these devices. Increasing this nonlinear capacitance will effectively modulate this same RC time constant. For the current design it was verified through simulations (not shown here) that the current devices sizes of S_t were near optimal under both of these constraints.

Simulation results shown here, predict that this architecture is very useful at low frequencies since all of the primary error effects are cancelled at these frequencies. Furthermore these results implies that 0.1dB accuracies can be obtain in the low MHz range, though it is hard to predict exactly how high in frequency this circuit can be pushed without knowing more specifics about the nonlinearities of the physical components. It is also evident that the current Sampling Algorithm may be highly sensitive to perturbations in the sampling hardware.

2.2.2.3d Sample/Hold-3

Driven by the frequency limitations of the S/H-2 architecture (specifically the finite and nonlinear on-resistance of the switch S_t), the following architecture is proposed as an extension of the feedback and offset cancellation techniques use in S/H-2 architecture. The new S/H structure discussed here reduces the effective on-resistance of the track-mode switch by placing the switch in the feedback path of a second additional OpAmp. The added offset voltage incurred by this second OpAmp is cancelled out during a new calibration-mode of the S/H. This S/H is refered to as S/H-3.

The basic architecture and its inherent performance limitations are described below, with corresponding experimental results contained in Section 5.14.

Description:

The circuit schematic for S/H-3 cell is shown in Fig. 2.2-31a with its associated timing diagram contained in Fig. 2.2-31b. The operation of this circuit is as follows.

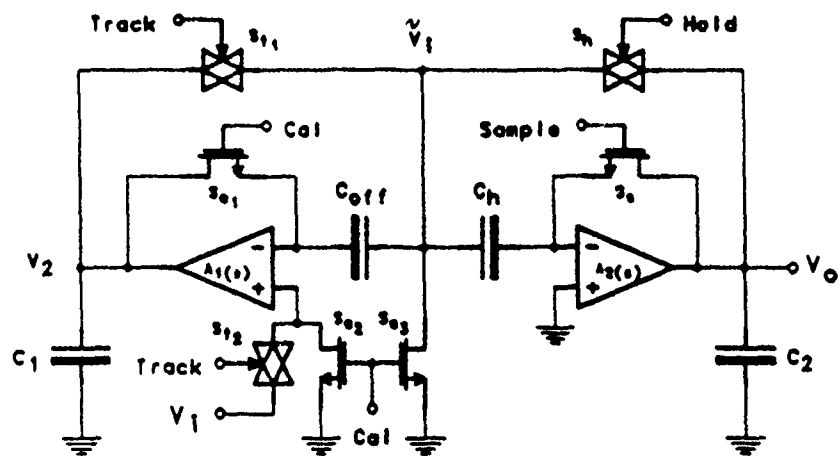
Consider initially the circuit configured in the calibration-mode, in which all of the track and hold switches are open (S_{t1} , S_{t2} , and S_h) and the calibration and sampling switches closed (S_{c1} , S_{c2} , S_{c3} , and S_s) and modelled as short-circuits as shown in the equivalent circuit contained in Fig. 2.2-31c. In this mode, OpAmp A_1 is biased so that its input offset voltage is across the capacitor C_{off} . After the system transients die out, the calibrate switches are opened, (isolating the bottom-plate of the C_{off} capacitor), thus trapping the offset voltage of A_1 , (V_{off}) on C_{off} . Note: the charge injected by the switch S_{c1} on the bottom-plate is cancelled by an equal amount of charge injected on the top-plate of C_{off} by the switch S_{c3} .

Now the track-mode switches (S_{t1} and S_{t2}) are closed, and the S/H is configured in track-mode, with the equivalent circuit shown in Fig. 2.2-31d. In this mode the OpAmp A_1 is configured as a noninverting unity gain buffer by the feedback path created by the closing of S_{t1} , with input to this buffer corresponding to the positive-input of the OpAmp A_1 and output attached to node v_I . When the input signal V_i is patched in through the analog switch S_{t2} , the input signal is buffered and tied to the top-plate of the hold capacitor C_h , with the bottom-plate essentially tied to ground through the null-port of A_2 . This results in the instantaneous voltage drop across the hold capacitor (v_H) equal to the instantaneous input-signal v_I , as is fundamental to the operation of a S/H.

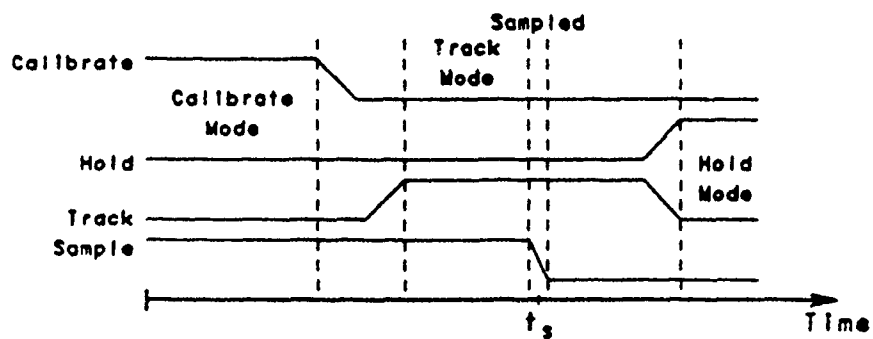
Observe that the voltage drop between the positive-input of A_1 and node v_I is essentially zero, since the input offset voltage of this amplifier is cancelled by the voltage drop across C_{off} .

If the switch S_s is opened at time t_s , the bottom plate of hold capacitor C_h is electrically isolated and the input voltage v_I is essentially "sampled". To complete the process, the top plate of the capacitor is isolated from the input signal by opening the switch S_{t1} , and then connected to the output by closing the switch S_h . This places the S/H in hold-mode, with the so called "sampled" input signal buffered and available on the V_O node, as shown in the equivalent circuit in Fig. 2.2-31e.

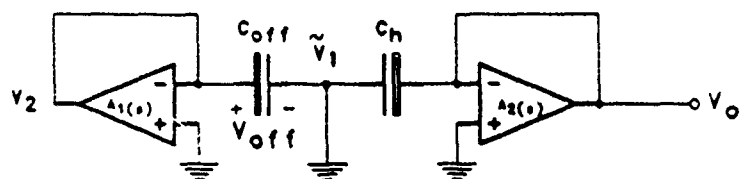
The analog switch S_s and the calibrate switches are all single n-channel MOSFET, while the other analog switches are the regular complimentary switches as shown in Fig. 2.2-11c. The device sizes for these analog switches and the other S/H components are shown in Table 2.2-15. The two capacitors C_1 and C_2 were added to the circuit to reduce switch charge injection.



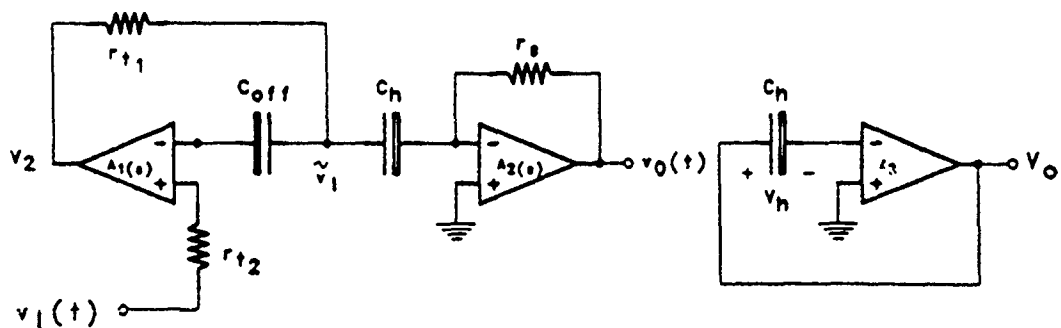
(a) Circuit Schematic



(b) Timing Diagram



(c) Calibrate Mode Equiv. Circuit



(d) Track Mode Equiv. Circuit

(e) Hold Mode Equiv. Circuit

Fig. 2.2-31. S/H-3

Table 2.2-15. Device sizes and component values for S/H-3 circuit schematic of Figures 2.2-31a.

Component	n-channel		p-channel		Value
	<i>W</i>	<i>L</i>	<i>W</i>	<i>L</i>	
S_{c_1}	$4\mu m$	$3\mu m$			
S_{c_2}	$4\mu m$	$3\mu m$			
S_{c_3}	$4\mu m$	$3\mu m$			
S_e	$12\mu m$	$3\mu m$			
S_{t_1}	$9\mu m$	$3\mu m$	$23\mu m$	$3\mu m$	
S_{t_2}	$18\mu m$	$3\mu m$	$46\mu m$	$3\mu m$	
S_h	$9\mu m$	$3\mu m$	$23\mu m$	$3\mu m$	
C_1					$5pF$
C_2					$5pF$
C_{off}					$1.5pF$
C_h					$1.5pF$

Performance Limitations:

This S/H architecture is an extension of the S/H-2 design and thus is subject to input signal swing of $\pm 2V$ and maximum input frequency in the neighborhood of 2 – 5 MHz. Since this design is similar to the previous design (S/H-2), only the track-mode performance limitations will be discussed.

Track-Mode

Consider the equivalent circuit contained in Fig. 2.2-31d. In this circuit the role of the switch S_{t_2} is to conduct the input-signal $v_i(s)$ through to the null-port of the OpAmp A_1 . Unfortunately, the finite on-resistance r_{t_2} of this analog switch in series with the input-capacitance of OpAmp A_1 (termed C_{in}), produces a single pole at the frequency $\frac{1}{r_{t_2} C_{in}}$. If the size of S_{t_2} is sufficiently large and the input-capacitance of the OpAmp minimized, then hopefully this parasitic pole can be neglected. For this design as documented in Table 2.2-15 and in the following section and for the nominal theoretical on-resistance of the complimentary switch as contained in Table 2.2-10 and for the typical input-capacitance of OpAmp as shown in Table 2.2-9, this pole is greater than 300 MHz. Obviously if this factor is of concern, the on-resistance of this switch can be reduced even further.

Similar to the analysis of S/H-2, the effective frequency dependent input-impedance looking into the two OpAmp's null-ports shall be denoted as \tilde{z}_t (representing the track-mode impedance associated with A_1 as shown in Fig. 2.2-32a) and \tilde{z}_s (representing the sampling switch impedance associated with A_2 as shown in Fig. 2.2-32b). Assuming a $\frac{GB}{s}$ model for the OpAmps, these frequency dependent impedances are mathematically modelled as follows:

$$\tilde{z}_t(s) = \frac{\frac{r_{t_2}}{GB} s}{1 + \frac{s}{GB}} \quad (2.2 - 85a)$$

$$\tilde{z}_s(s) = \frac{\frac{r_{t_2}}{GB} s}{1 + \frac{s}{GB}} \quad (2.2 - 85b)$$

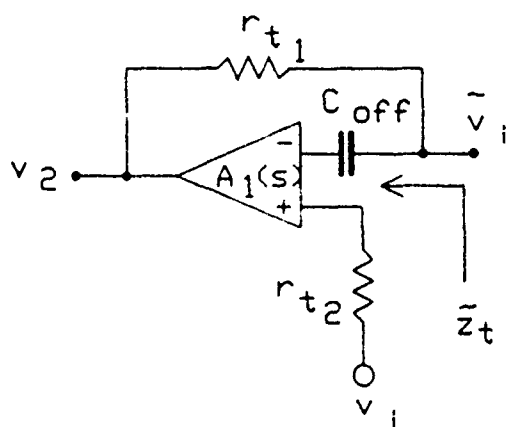
Thus the original track-mode equivalent circuit of Fig. 2.2-31d can be reduced to a simple RC network as shown in Fig. 2.2-32c.

From this simplified circuit, the AC voltage gain between the input signal v_i and the voltage drop across the hold capacitor v_h was computed to be

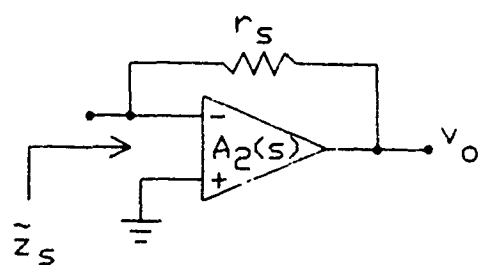
$$A_v \stackrel{\text{def}}{=} \frac{v_h(s)}{v_i(s)} = \frac{\frac{1}{\omega_z} (s + \omega_z)}{\frac{1}{\omega_o^2} (s^2 + BWs + \omega_o^2)} \quad (2.2 - 86a)$$

where

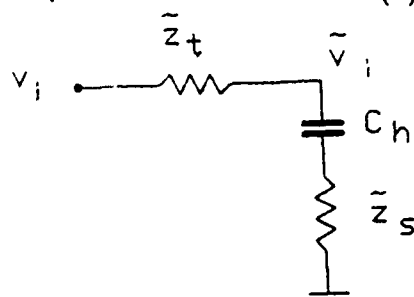
$$\omega_z = GB \approx 2\pi(30\text{MHz}) \quad (2.2 - 86b)$$



(a) \tilde{z}_t OpAmp circuit



(b) \tilde{z}_s OpAmp circuit



(c) reduced track-mode equivalent circuit.

Fig. 2.2-32. Circuit schematics for frequency-domain analysis of S/H-2 in track-mode.

$$\omega_o = \sqrt{\frac{GB}{(r_t + r_s) C_h}} \approx 2\pi(25MHz) \quad (2.2 - 86c)$$

$$BW = \frac{1}{(r_t + r_s) C_h} \approx 2\pi(22.5MHz) \quad (2.2 - 86d)$$

as based upon the device sizes shown in Table 2.2-15 and the physical OpAmp design documented in Section 2.2.2.3e

Observe that ω_z and ω_o are identical to the previously reported expressions for S/H-2, contained in Eq. (2.2-79). Interestingly enough the only significant change between the two transfer functions, was the pole-bandwidth or pole Q , in which the Q of S/H-3 was increased by 45% over the Q of S/H-2. This is a considerable factor as illustrated in the graphical comparison (in Fig. 2.2-33) and quantitative comparison (in Table 2.2-16) of the three different track-mode frequency responses for S/H-1 -2 and -3.

If we compare the three gain frequency responses, the S/H-2 design provided the largest 0.1dB-bandwidth with a factor of $2\frac{3}{4}$ increase in bandwidth over the simple S/H-1 architecture, and a 30% increase over the complex S/H-3 architecture. This slight degradation in the gain response of the S/H-3 design is attributable to the peaking associated with the higher Q circuit. Though if we consider the phase response of these three designs, the S/H-3 design is by far the best with a factor of six improvement in 1° -bandwidth over the S/H-2 design and a two orders of magnitude improvement over the S/H-1 architecture. This drastic improvement in performance by the S/H-3 cell is directly related to the decrease pole bandwidth of this design. Lastly if we wish to fairly compare these architectures, we must couple the phase and the gain specifications together, since they both affect the overall accuracy of the Sampling Algorithm. Thus for a specification of .1dB gain accuracy and 1° phase accuracy, the S/H-3 had the largest bandwidth of 2.8MHz, which is a factor of $2\frac{1}{3}$ increase over S/H-2 and a factor of 40 over S/H-1.

Nonlinear Distortion

The results presented thus far are based upon the theoretical *linearized* track-mode frequency response. The affects of the voltage dependent nonlinearities of the on-resistances of the analog switches and the parasitic diffusion capacitances have been neglected. The following analysis will address these nonlinearities and how they affect the overall obtainable accuracy of the Performance Measurement System, as previously addressed in the S/H-2 discussion.

The primary significant difference between the nonlinearities of S/H-2 and those of the S/H-3 architecture is not that one architecture is constructed from better, more linear components, but on the contrary one architecture (i.e., S/H-3) is inherently less sensitive to these nonlinearities; stemming from the attenuating affect of the A_1 feedback network in conjunction with the r_t nonlinearities. Thus if we apply the same nonlinear models as

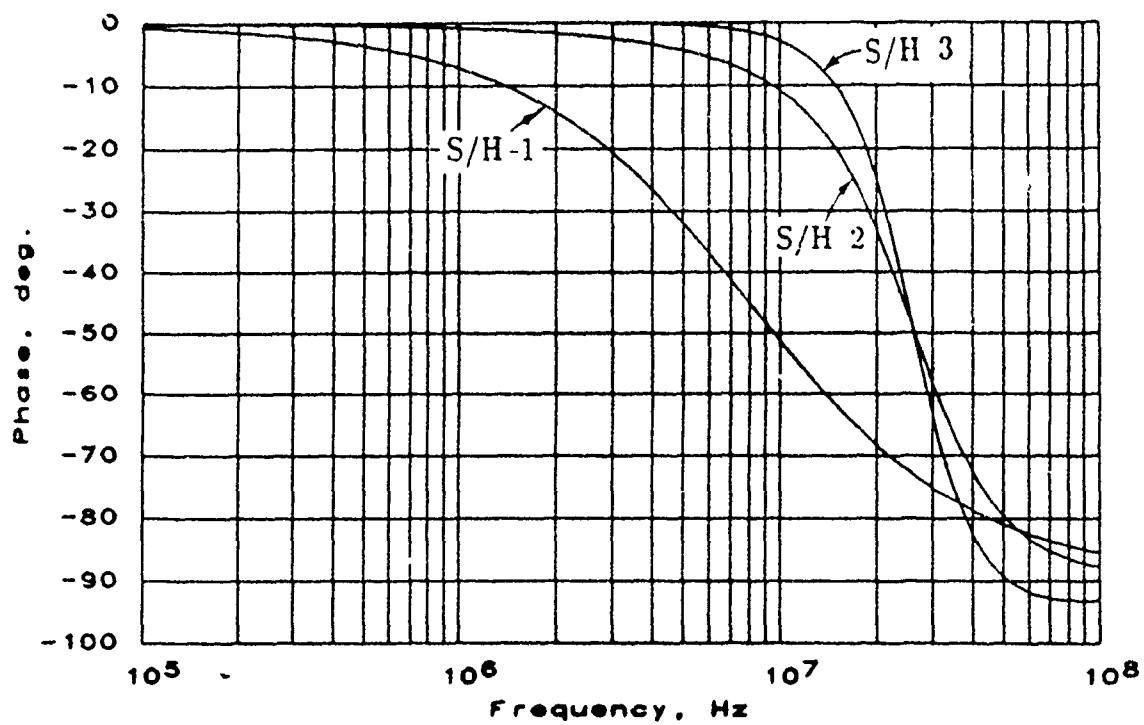
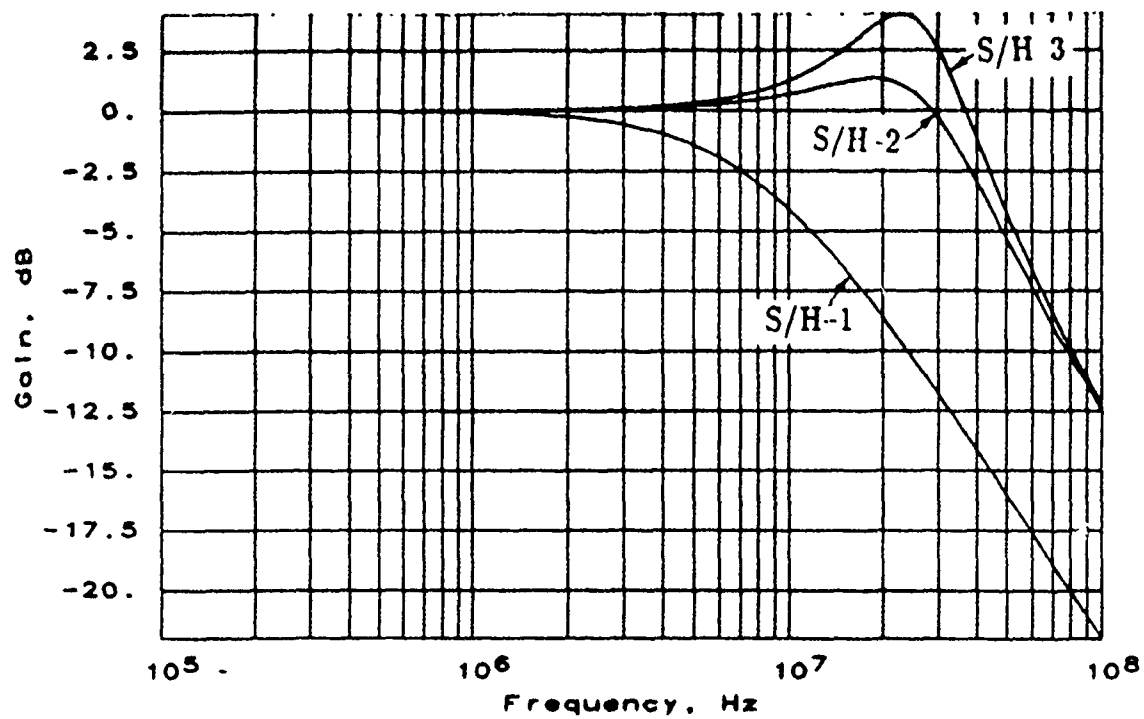


Fig. 2.2-33. Frequency response of $v_h(s)/v_i(s)$ for all three S/H's operating in track-mode.

Table 2.2-16. Comparison of usable frequency range or bandwidth for all three S/H's operating in track-mode, as a function of the gain or phase resolution specification. This data is graphically presented in Fig. 2.2-33.

Response Spec.	Bandwidth, <i>Hz</i>		
	S/H-1	S/H-2	S/H-3
0.01 <i>dB</i>	400 <i>k</i>	1.1 <i>M</i>	910 <i>k</i>
0.02 <i>dB</i>	550 <i>k</i>	1.6 <i>M</i>	1.2 <i>M</i>
0.05 <i>dB</i>	860 <i>k</i>	2.5 <i>M</i>	2.0 <i>M</i>
0.1 <i>dB</i>	1.3 <i>M</i>	3.6 <i>M</i>	2.8 <i>M</i>
0.2 <i>dB</i>	1.7 <i>M</i>	5.2 <i>M</i>	4.0 <i>M</i>
0.5 <i>dB</i>	2.8 <i>M</i>	8.5 <i>M</i>	6.3 <i>M</i>
1.0 <i>dB</i>	4.1 <i>M</i>	13.0 <i>M</i>	9.1 <i>M</i>
0.02°	2.8 <i>k</i>	25 <i>k</i>	1.9 <i>M</i>
0.05°	7.0 <i>k</i>	62 <i>k</i>	2.6 <i>M</i>
0.1°	14 <i>k</i>	120 <i>k</i>	3.3 <i>M</i>
0.2°	28 <i>k</i>	250 <i>k</i>	4.1 <i>M</i>
0.5°	70 <i>k</i>	630 <i>k</i>	5.6 <i>M</i>
1.0°	140 <i>k</i>	1.2 <i>M</i>	7.1 <i>M</i>
2.0°	280 <i>k</i>	2.4 <i>M</i>	8.9 <i>M</i>
5.0°	700 <i>k</i>	5.7 <i>M</i>	12.0 <i>M</i>
10.0°	1.4 <i>M</i>	9.5 <i>M</i>	15.0 <i>M</i>

contained in Eqs. (2.2-84), and simulate the complete Performance Measurement System with the intended Sampling Algorithm as performed on the S/H-2 architecture, then the overall impact of these nonlinearities can be studied and quantitized.

The results of this analysis for the S/H-3 circuit as defined in Fig. 2.2-31 and Table 2.2-15, are provided graphically in Fig. 2.2-34, and quantitatively in Table 2.2-17. Also repeated here, for the sake of comparison are the aforementioned results of the S/H-2 architecture as originally provided in Figs. 2.2-39 and 2.2-40.

The results shown here, indicate that the S/H-3 architecture greatly out performs the S/H-2 design by a factor of 2-4 in the accuracy of predicting the gain and a factor of 10 in the accuracy of predicting the phase at high frequencies (2-5MHz). This improvement is attributed to the improved phase response of the track-mode operation of this S/H.

Conclusions:

The S/H-3 architecture out performed each of the previous designs, with a factor of 2 increase in usable frequency range over the S/H-2 design and almost a decade beyond the S/H-1 design. This architecture greatly minimizes the parasitic effects due to inherent component nonlinearities and thus removes these nonidealities from affecting its performance. The design strategy used here of eliminating nonidealities by better circuit design techniques produced a design that is less sensitive to poorly predicted and poorly controlled circuit nonlinearities and is preferred over strategies that rely heavily on a priori knowledge of these nonidealities and careful cancellation of these effects. This is not the case here.

One last comment is in order. The complex input offset voltage cancellation technique used here is not necessary if this S/H is to be used in the DCASP architecture since this nonideality is voltage independent and can easily be cancelled by the Sampling Algorithm. In particular, the excitation and response signals of the CSP are already perturbed by offsets, and must be incorporated in the Sampling Algorithm anyway. It is recommended that future generations of this circuit remove the extra calibration clock phase, thus simplifying the overall architecture and the required random logic to interface to this device.

2.2.2.3e Sample/Hold operational amplifier

Purpose:

The S/H structures, S/H-1, S/H-2 and S/H-3 discussed previously require high performance operational amplifiers in order to sample high frequency (2 - 5MHz) and high amplitude ($4V_{p-p}$) signals with 0.1% accuracy. Based upon the design trade-offs and performance issues as detailed previously in this section, the CMOS OpAmp specifications of

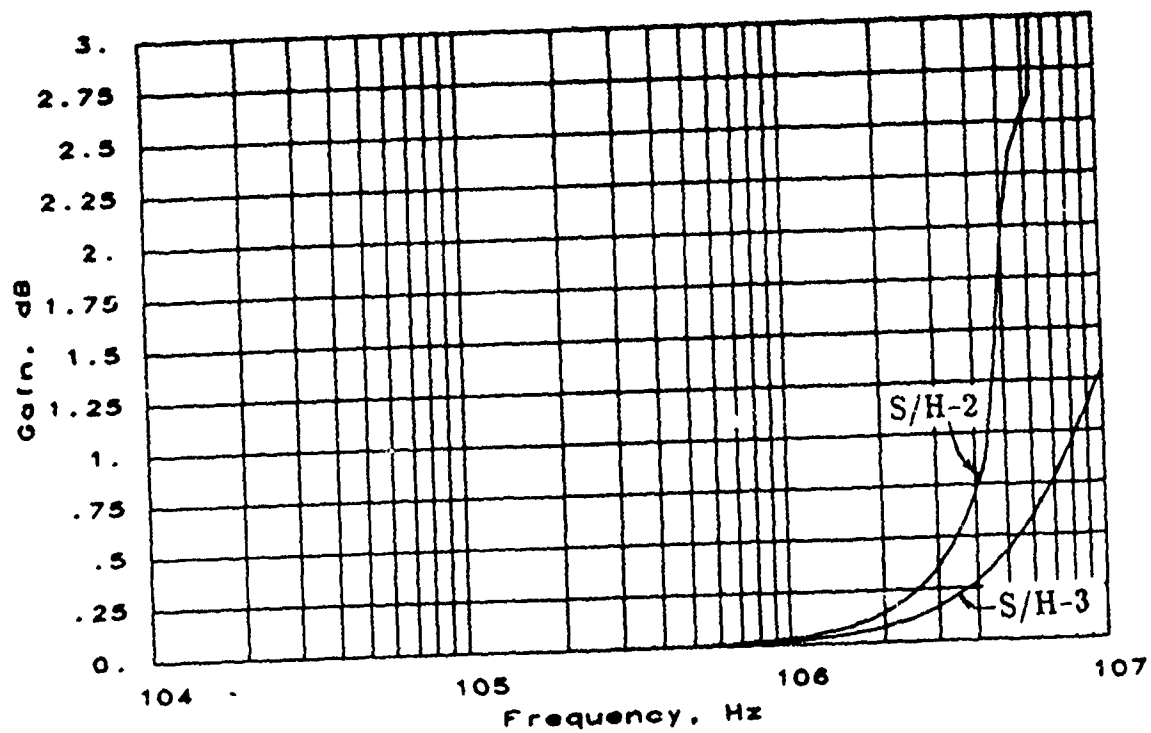


Fig. 2.2-34a Plot of predicted gain measurement error via errors induced into the Sampling Algorithm from track-mode nonlinearities in S/H-2 and -3. Specifically this is a plot of the extracted $|v_h(s)/v_i(s)|$ — ideally unity gain.

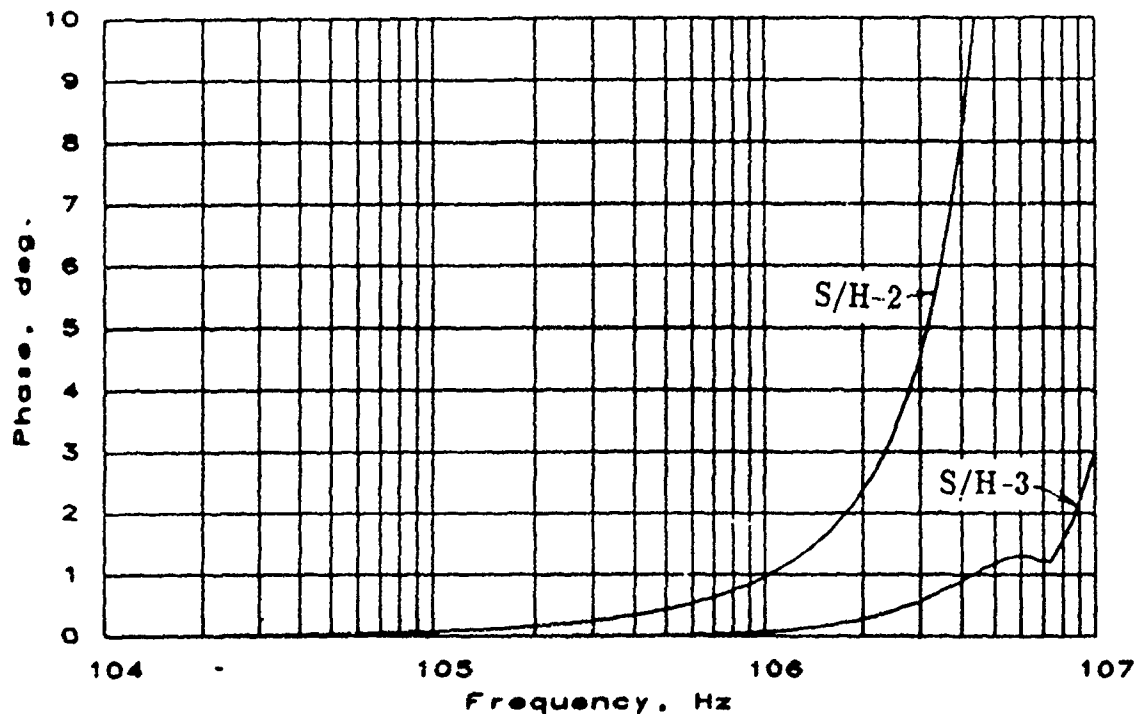


Fig. 2.2-34b Plot of predicted phase measurement error via errors induced into the Sampling Algorithm from track-mode nonlinearities in S/H-2 and -3. Specifically this is a plot of the extracted $(\angle(v_o(s)/v_i(s)) - \theta)$ — ideally zero.

Table 2.2-17. Summary of the simulation results presented in Figs. 2.2-29 of the errors induced in the extracted gain and phase by the Sampling Algorithm due to the track-mode nonlinearities of S/H-2 and -3.

frequency	$\left \frac{v_h(s)}{v_i(s)} \right (dB)$		$\angle \left(\frac{v_o(s)}{v_i(s)} \right) - \theta$	
	S/H-2	S/H-3	S/H-2	S/H-3
10kHz	0.00006	0.00000	0.0073°	0.00001°
100kHz	0.00047	0.00019	0.074°	0.00079°
200kHz	0.00066	0.00075	0.15°	0.0031°
500kHz	0.0065	0.0047	0.40°	0.019°
1MHz	0.031	0.019	0.87°	0.075°
2MHz	0.14	0.074	2.1°	0.28°
5MHz	2.0	0.43	13.°	1.2°
10MHz	9.7	1.3	93.°	3.1°

Table 2.2-18 were established as a design goal.

The most challenging of these specifications are the high bandwidth, the low input capacitance, the large input signal swing and the large load-capacitance.

Description:

The basic OpAmp architecture used in the design of the CMOS OpAmp is shown in Fig. 2.2-35. This is a scaled down version of a 40MHz CMOS buffer design of Van-Peteghem [26] with an added source-follower input stage. This additional source-follower input stage will provide a much lower input-capacitance to the OpAmp and help drive the large input-capacitance of the differential-pair, which is primarily due to the Miller Effect. The original buffer design of VanPeteghem had a semi-low input-capacitance ($0.5pF$) since the common source node of the differential pair bootstraps the major portion of the input-capacitance when feedback is applied to the negative input node of the OpAmp. Ideally, in this configuration, the differential pair has no differential signal across its inputs, but rather only common-mode signal, [27] thus bootstrapping the Miller Capacitor as discussed later in this section.

The original buffer design can be summarized as follows: The n-channel differential-pair was chosen as the input stage due to its high device mobility and thus typically higher bandwidths. The current-source, I_{SS} , must be a single n-channel MOSFET to prevent the voltage drop across the source-follower from distorting the signal as the input signal swings towards the negative rail. The modified cascode current-mirror with common-mode feedback provides a high output impedance and a large PSRR with little degradation to the common-mode input range [28] The source-follower output stage drives the large external load capacitor seen on the output of the OpAmp. In order to drive large capacitive loads at high frequency, large bias currents and large device sizes are required. The bias currents shown in Fig. 2.2-35 are set at

$$I_O = I_{I-} = I_{I+} = 0.5mA \quad \text{and} \quad I_{SS} = 0.2mA. \quad (2.2 - 87)$$

The complete circuit schematic is shown in Fig. 2.2-36 with the corresponding device sizes provided in Table 2.2-19. V^- and V^+ are the differential inputs and the node labeled V_{out} is the low impedance output node. The current I_{bias} is an externally provided bias current, nominally set at $0.1mA$. The input source-follower consists of devices M_{i1} and M_{i2} which drive the differential-pair, M_{d1} and M_{d2} . The current-mirror consists of devices M_{m1} through M_{m4} . The output source-follower is the n-channel MOSFET, M_{o1} . The remaining devices, M_{b1} through M_{b6} , are current sinks and bias transistors.

The devices, M_{m1} and M_{m2} are biased in the linear region with M_{b7} and M_{b8} . They serve as an active resistor whose resistance and thus output current is a function of their gate to source voltage. Since the gates of these two devices are feeding off of the same

Table 2.2-18. S/H OpAmp design specifications.

3dB Bandwidth	$\geq 30MHz$
Slew Rate	$60V/\mu sec$
Open Loop Gain	≥ 50
Input Capacitance	$\leq 100fF$
Load Capacitance	$5 - 7pF$
Signal Levels	to $\pm 2V$ with $\pm 5V$ sup.
Input Signal BW.	$\leq 5MHz$

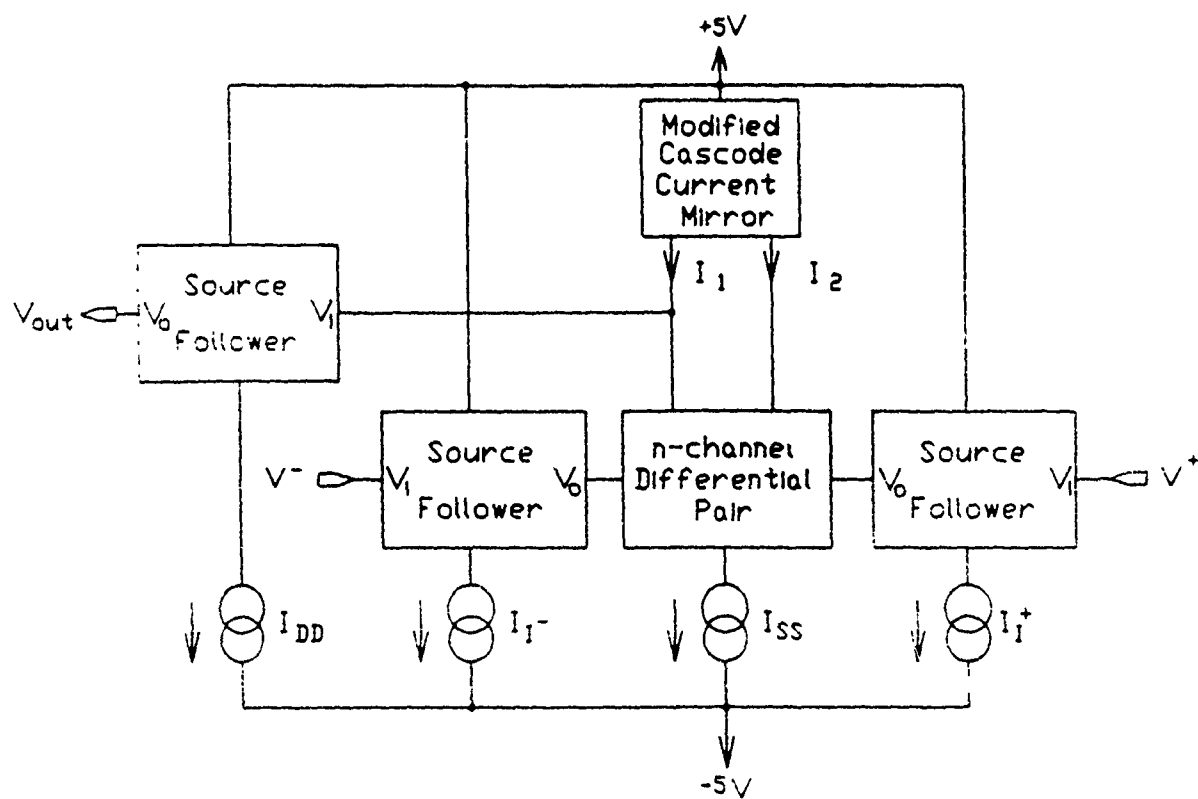


Fig. 2.2-35. S/H OpAmp block diagram.

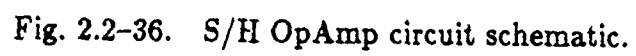


Table 2.2-19. S/H OpAmp devices sizes for Fig. 2.2-36.

DEVICE	SIZE		DEVICE	SIZE	
	W	L		W	L
M_{i_1}, M_{i_2}	174μ	3μ	$M_{b_1}, M_{b_2}, M_{b_4}$	74μ	3μ
M_{d_1}, M_{d_2}	300μ	3μ	M_{b_3}	30μ	3μ
$M_{m_1}, M_{m_2}, M_{b_8}$	100μ	3μ	M_{b_5}, M_{b_6}	15μ	3μ
$M_{m_3}, M_{m_4}, M_{b_7}$	25μ	3μ	M_{o_1}	498μ	3μ

internal node, the pair function as a typical current mirror. The cascode devices, M_{m3} and M_{m4} , are biased in saturation and provide a large output impedance and thus increased isolation from any power-supply injected noise from V_{DD} .

Source-Follower

The source-follower, as shown in Fig. 2.2-37, is a key subcircuit of the OpAmp, as it buffers the inputs and output of the OpAmp. Also shown in this figure are the load capacitor, C_l , and the parasitic overlap capacitors, C_{gs} and C_{gd} . The device M_1 should be biased in saturation for a unity small signal gain. From the simplified Sah model of M_1 , the DC bias current, I_D , is given by

$$I_{DD} = I_D = \frac{K'_n W_1}{2 L_1} (V_I - V_O - V_{th1})^2 \quad (2.2 - 88)$$

In order to minimize the DC voltage drop across the source-follower and not to overly restrict the signal swing, we have decided to require $V_I - V_O < 1.6V$.

Defining the over-drive voltage, V_{OD} , by the equation

$$V_{OD} \stackrel{\text{def}}{=} \sqrt{\frac{2I_D L_1}{K'_n W_1}} \quad (2.2 - 89)$$

it follows from eqn. (2.2-88) that V_O can be expressed in terms of V_{OD} as

$$V_O = V_I - V_{th1} - V_{OD} \quad (2.2 - 90)$$

From this expression it can be observed that if the bulk were tied to V_{SS} , then the bulk-effect (γ effect) would have the tendency to modulate V_{th1} between 0.8V and 2.5V as the input swings between $\pm 2V$. This would cause both signal distortion and signal swing limitation. The effects of γ can be eliminated by connecting the bulk to the source of M_1 . Making this connection comes at the expense of adding more parasitic capacitance to the output node of the source-follower. With V_{th1} restricted to approximately 0.8V, and $V_{OD} \leq 0.8V$, we can achieve our goal of making $V_I - V_O < 1.6V$.

The AC small signal model for this subcircuit is shown in Fig. 2.2-38, where g_m and g_{ds} correspond to the small signal model parameters for the device M_1 and g_d represents the parasitic output admittance of the current sink, I_{DD} . From this circuit, we can calculate the frequency domain transfer function as shown below in eq. (2.2-91).

$$\frac{v_o}{v_i} = \left(\frac{g_m}{g_m + g_{ds} + g_d} \right) \frac{1 + \frac{C_{gs}s}{g_m}}{1 + \frac{C_l + C_{gs}}{g_m + g_{ds} + g_d}s} \approx A_v \frac{1 + \frac{C_{gs}s}{g_m}}{1 + \frac{C_l}{g_m}s} \quad (2.2 - 91a)$$

$$A_v = \frac{g_m}{g_m + g_{ds} + g_d} \approx 1 \quad (2.2 - 91b)$$

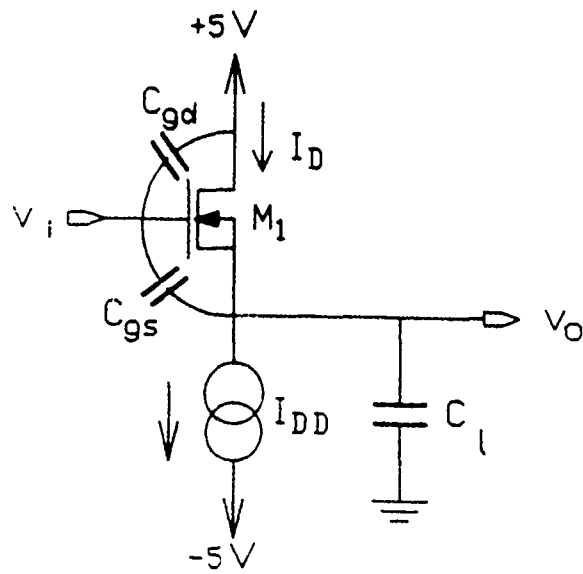


Fig. 2.2-37. Source-follower circuit schematic.

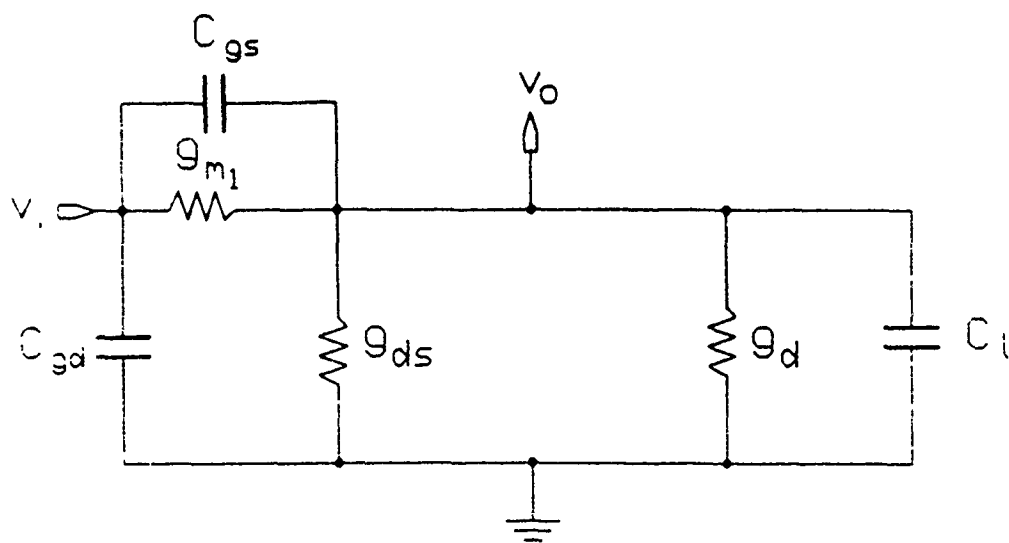


Fig. 2.2-38. Source-follower AC small-signal model.

Assuming $g_m \gg g_{ds} + g_d$ and $C_l \gg C_{gs}$, yields a unity gain amplifier with a pole at ω_p and a zero at ω_{z_1} such that $\omega_p \approx \frac{g_m}{C_l}$ and $\omega_{z_1} \gg \frac{g_m}{C_{gs}}$.

The small signal input capacitance is composed of two components, the overlap capacitance, C_{gd} and the Miller Capacitor due to C_{gs} . Since the device M_1 is in saturation, the C_{gs} capacitance is modeled as $\frac{2}{3}$ of the gate capacitance [21]. Thus, if it is assumed $C_l \gg C_{gs}$, $C_{gs} \gg C_{gd}$ and $g_m \gg g_{ds} + g_d$, then the input-capacitance for the source-follower can be expressed as

$$C_{in} = C_{gd} + C_{gs} \left(1 - \frac{v_o}{v_i} \right) \quad (2.2 - 92a)$$

$$= C_{in_o} \frac{1 + \frac{s}{\omega_{z_2}}}{1 + \frac{s}{\omega_p}} \quad (2.2 - 92b)$$

$$= C_{in_\infty} \frac{1 + \frac{\omega_{z_2}}{s}}{1 + \frac{\omega_p}{s}} \quad (2.2 - 92c)$$

where,

$$C_{in_o} \approx C_{gd} + C_{gs} \frac{g_{ds} + g_d}{g_m} \quad (2.2 - 92d)$$

$$C_{in_\infty} = C_{gd} + C_{gs} \quad (2.2 - 92e)$$

$$\omega_{z_2} \approx \frac{g_{ds} + g_d + g_m \frac{C_{gd}}{C_{gs}}}{C_l} \quad (2.2 - 92f)$$

$$\omega_p \approx \frac{g_m}{C_l} \quad (2.2 - 92g)$$

$$C_{gs} \approx \frac{2}{3} C_{ox} W_1 L_1 \quad (2.2 - 92h)$$

and

$$C_{ds} = C_{ox} W_1 L_d \quad (2.2 - 92i)$$

The variable C_{in_o} and C_{in_∞} represent respectively, the input capacitance at DC and at extremely high frequencies. The constant C_{ox} represents the gate to channel capacitance density (typically $0.7 fF/\mu^2$ in a generic 3μ CMOS process) and L_d represents the lateral diffusion length (typically around 0.3μ in the same process).

The Miller Effect greatly reduces the input-capacitance by attenuating the dominate parasitic capacitance, C_{gs} . This attenuation is due to the boot-strapping effect of the unity-gain configuration. This capacitance cancellation technique is very sensitive to any phase

shift between the input node and the boot-strapping node. This is apparent from the above analysis, since the location of the zero, ω_{z2} , was at a significantly lower frequency than the pole, ω_p .

The small-signal parasitic load capacitance is composed of many different components as listed in eq. (2.2-93)

$$C_l = C_s + C_w + C_d + C_{gs} \left(1 - \frac{v_i}{v_o} \right) + C_{in2} \quad (2.2 - 93a)$$

$$\cong C_s + C_w + C_d - C_{gs} \left(\frac{g_{ds} + g_d}{g_m} \right) + C_{in2} \quad (2.2 - 93b)$$

where, C_s and C_d are the parasitic capacitance due to the source diffusion of M_1 and the drain diffusion of the current sink, I_D , respectively. C_w is the parasitic well capacitance of the p-well containing the device M_1 and C_{in2} is the input capacitance of the next stage. Note, the Miller Capacitor was reduced to a small negative load capacitor which should exhibit the same phase distortion sensitivity problem that the input-capacitance exhibited; and thus is not a very useful technique for reducing the overall effective load capacitance at high frequencies.

For the design documented in Table 2.2-19 above, the characteristics of both the input and output source-follower stages are shown in Table 2.2-20 as computed from equations (2.2-89) through (2.2-93) and SPICE generated small-signal model parameters.

Note, the pole locations of the input and output stages are currently marginal to yield the desired input capacitance.

Simulation Results:

The parasitics of the layout of the design described above were extracted and a SPICE simulation file was generated. This SPICE deck in combination with the MOSIS analog SPICE model were used in simulations which are summarized below.

- (a) Open-Loop frequency response from both the inverting and noninverting inputs of the OpAmp. From the resulting Bode-Plots shown in Fig. 2.2-39, the open-loop gain, gain-margin and phase margin can be extracted.
- (b) Closed-Loop step response for the OpAmp configured in a unity gain buffer configuration. These are shown in Fig. 2.2-40. From this plot, the settling time, percent overshoot and slew rate can be determined.
- (c) Small-signal AC analysis. From a small-signal ac analysis, the input current as a function of the input voltage and input frequency can be used to determine the small-signal complex input-impedance of the OpAmp. That is

Table 2.2-20. Source-Follower theoretical characteristics.

Parameter	Output	Input
I_D	$0.5mA$	$0.5mA$
g_m	$2.2mS$	$1.3mS$
g_{ds}	$29\mu S$	$19\mu S$
g_d	$18\mu S$	$18\mu S$
C_{gs}	$0.56pF$	$0.19pF$
C_{gd}	$0.10pF$	$0.03pF$
C_w	$0.45pF$	$0.17pF$
C_s	$0.38pF$	$0.14pF$
C_d	$0.06pF$	$0.06pF$
A_v	0.979	0.972
C_{in2}	$6pF$	$6pF$
C_l	$6.8pF$	$6.3pF$
C_{in_o}	$0.11pF$	$0.04pF$
C_{in_∞}	$0.66pF$	$0.22pF$
ω_{z_1}	$625MHz$	$1.1GHz$
ω_p	$51MHz$	$33MHz$
ω_{z_2}	$10MHz$	$6MHz$
V_{OD}	$0.4V$	$0.7V$

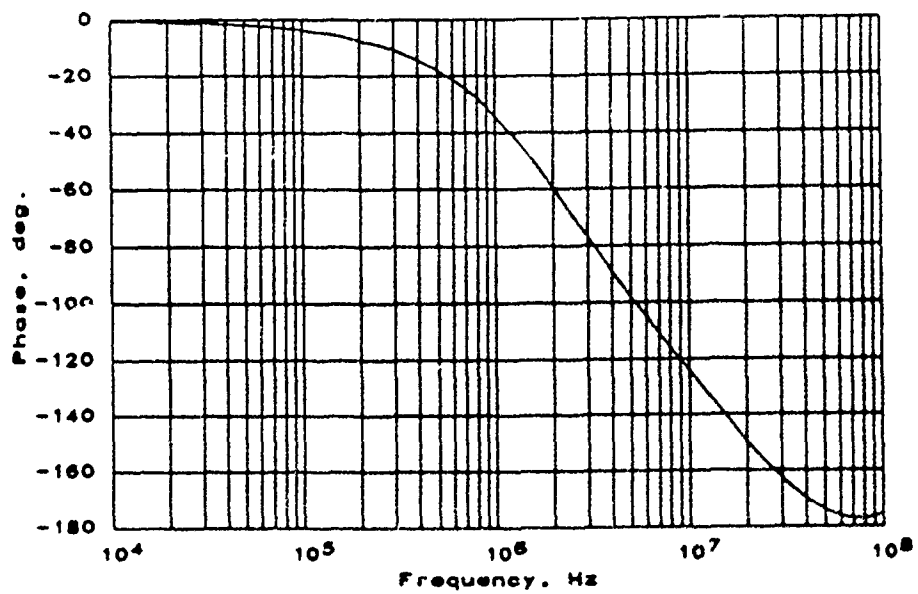
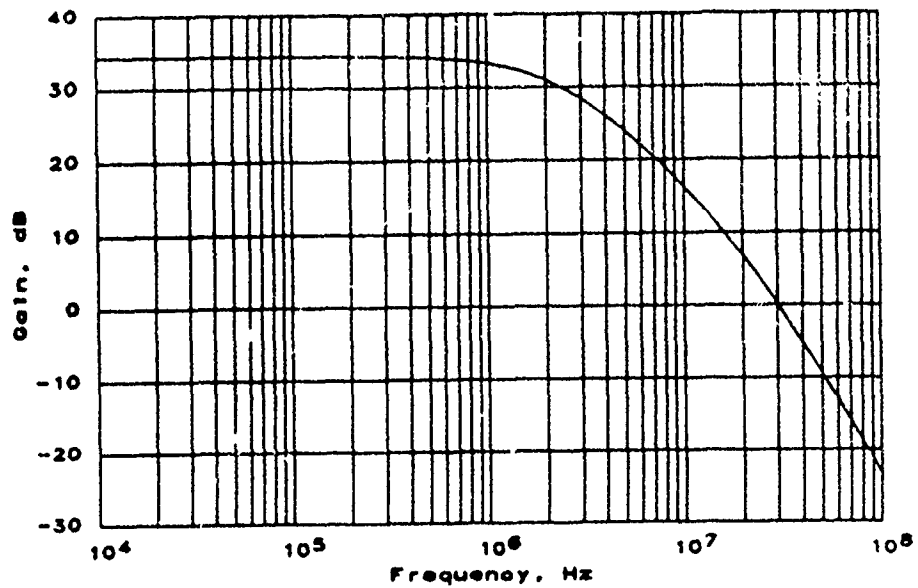


Fig. 2.2-39a. Simulated open-loop freq. resp. for the V^+ input of S/H OpAmp.

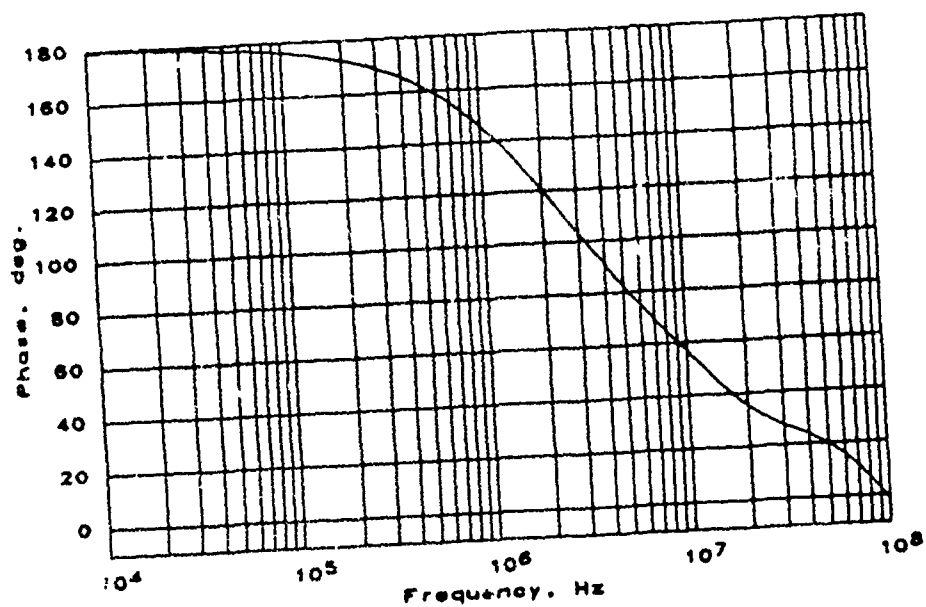
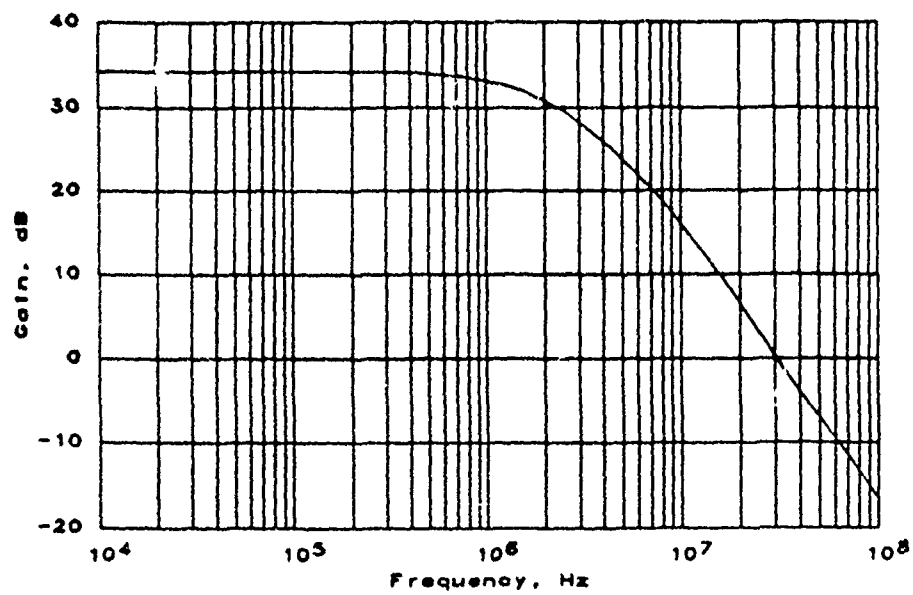


Fig. 2.2-39b. Simulated open-loop freq. resp. for the V^- input of S/H OpAmp.

$$Z_{in}(j\omega) \stackrel{\text{def}}{=} \frac{v_{in}(j\omega)}{i_{in}(j\omega)} \quad (2.2 - 94)$$

where i_{in} and v_{in} represent in the small-signal input current and voltage, respectively and $\omega = 2\pi f$. The input impedance of the OpAmp is a function of frequency and not purely capacitive, as illustrated by eq. (2.2-92), and supported by simulation results graphically presented in Fig. 2.2-41. From this plot, it can be concluded that at low frequencies, the input impedance looks totally capacitive with a phase angle of -90° up to about 300kHz. The magnitude plot shown here is $\| \frac{1}{j\omega Z_{in}} \|$ which represents capacitance when the phase angle of Z_{in} is exactly -90° . For phase angles other than this, it is difficult to interpret — a purely resistive impedance would be represented by a phase angle of 0° and a magnitude plot resembling a $\frac{1}{x}$ function.

The simulation results are summarized in Table 2.2-12. Each of the original design specifications were met. The phase margins are less than desired. The input capacitance predicted by the simulation differed significantly from the theoretical calculations. The source of this discrepancy has not been resolved. Further reductions in input capacitance with this circuit can be obtained at the expense of a reduced bandwidth. Alternatively, a different architecture of the Op Amp may deserve consideration if the experimentally measured input capacitance is unacceptable.

2.2.2.3f Sample/Hold operational amplifier with added zero

In the previous section, the Sample/Hold operational amplifier had a simulated phase margin of 18° (29°) for V^+ (V^-). This is borderline stable. Thus in this section we will discuss a modified OpAmp design, that should improve stability.

The approach is to add an additional load capacitance (C_z) to the common-source node of the differential amplifier and a feed-forward zero, as shown in Fig. 2.2-42. It is hoped that

- (1) the added capacitance on this node will decrease the dominant pole location slightly, and
- (2) at ultra high-frequencies this added capacitor will act as a short circuit between the node V_1 and the common-source node, and thus introduce an ultra high-frequency zero into the transfer function.

The size of the capacitor C_z was intended to be in the range of $1 - 2pF$, and was actually implemented as a $1.37pF$ poly-I/poly-II capacitor because of layout area restrictions.

The results of modifying this design are shown in the BODE plots contained in Fig-

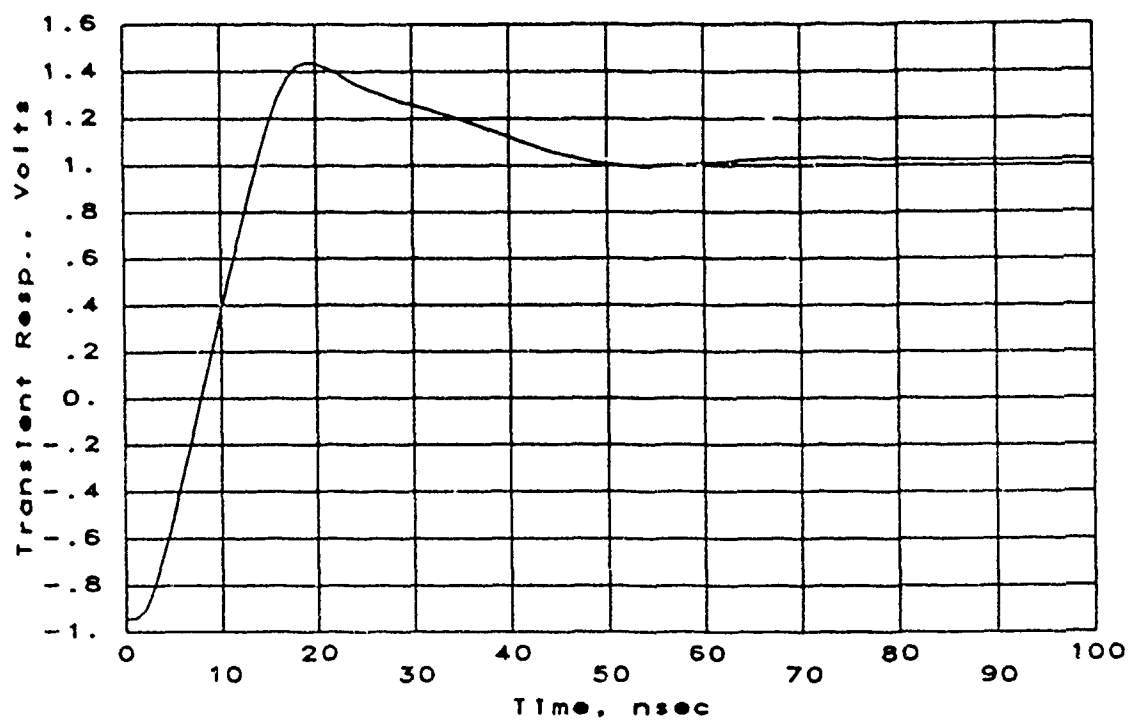
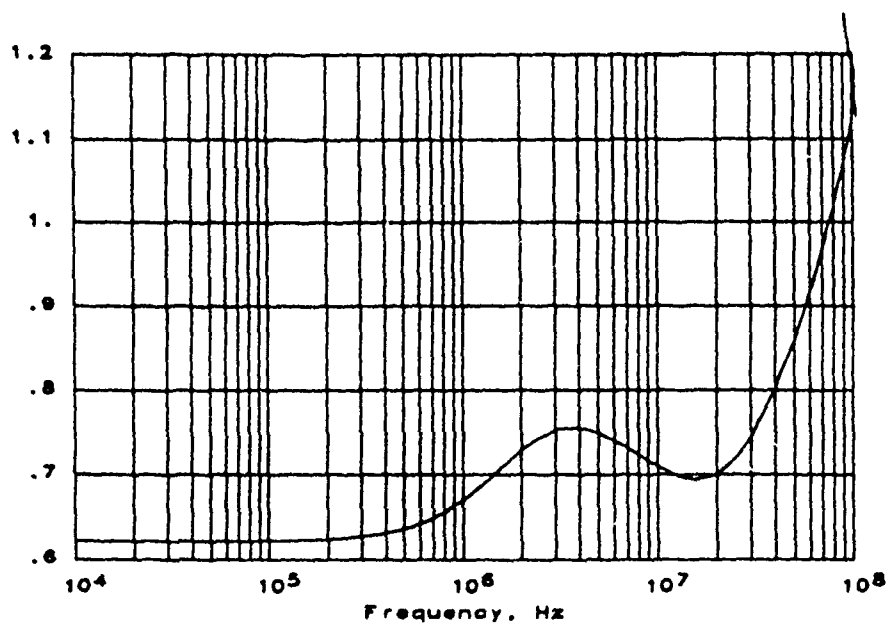


Fig. 2.2-40. Simulated close-loop step response for the S/H OpAmp.

$$\left| \frac{1}{j\omega Z_{in}} \right|, pF$$



$$\angle (Z_{in}), ^\circ$$

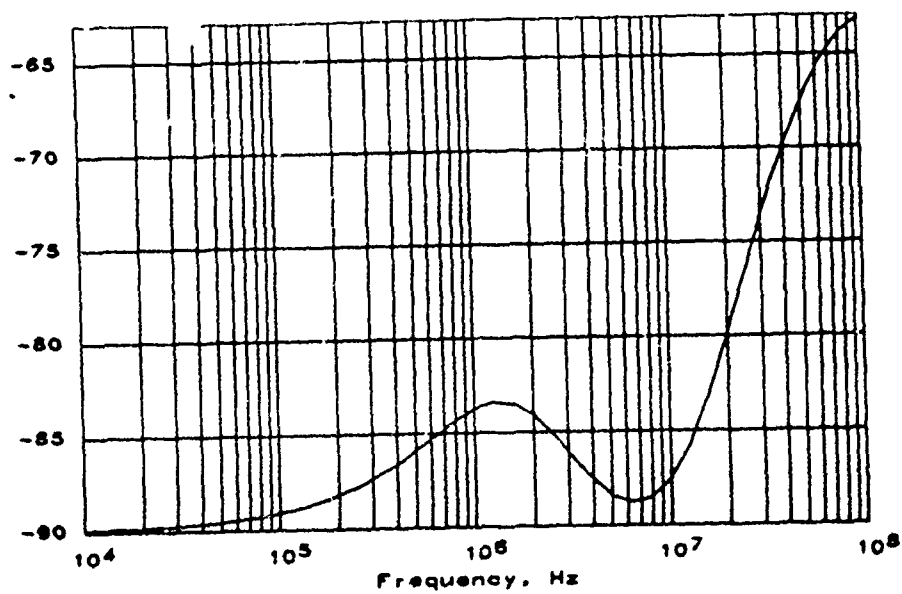


Fig. 2.2-41. Simulated input impedance for the S/H OpAmp.

Table 2.2-21. S/H OpAmp simulated design specifications.

Open-Loop 3dB Bandwidth	30.5MHz
Gain Margin (V^+)	$\leq -20dB$,
Gain Margin (V^-)	$-16dB$,
Phase Margin (V^+)	18°
Phase Margin (V^-)	29°
Settling Time (1%)	70 η sec
Percent Overshoot	20%
Slew Rate	160V/ μ sec
Open Loop Gain	52
Input Capacitance	620fF – 860fF

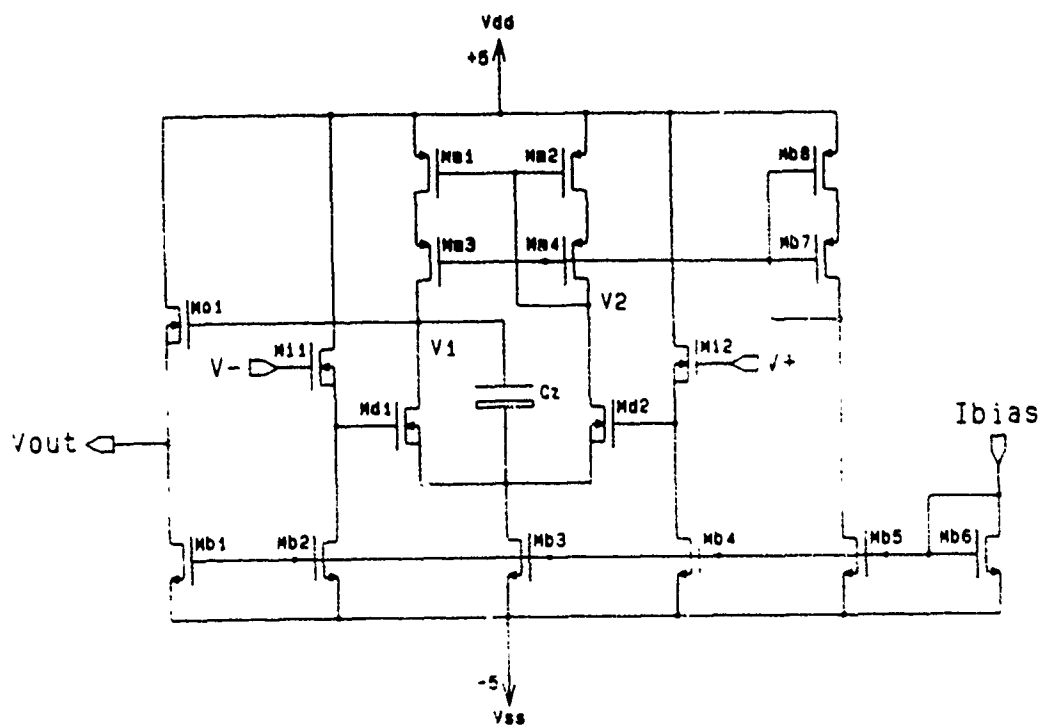


Fig. 2.2-42. S/H OpAmp with added zero circuit schematic.

ures. 2.2-43a and b. Shown here is an improved gain and phase margin at the expense of reduced open-loop 3dB bandwidth. These results are summarized in Table. 2.2-22.

2.2.2.3g Other gain Performance Detector systems.

Over the decades many solutions to the performance detection problem have been proposed, primarily in Hybrid, discrete, Bipolar or technologies other than MOS. Finally in the 80's we are beginning to see these architectures translated into a MOS environment. In this section, we will discuss some of these alternative gain measurement approaches.

Peak Detectors:

Peak detection is one of the more conventional techniques. It requires little post processing of the measured data in order to compute the gain, but is restricted to applications not requiring phase measurement. Obviously, the basic strategy of this approach is to compute the peak amplitude of both the excitation and response signals, and then compute the gain from the ratio. Two Peak Detector architectures are presented below.

Conventional Peak Detector

A standard approach given an ideal diode is shown in Fig. 2.2-44. Here the input signal (V_i) turns "on" the ideal diode (D_1) whenever the input voltage exceeds the peak voltage (V_{peak}) held on the hold capacitor (C_{peak}). The hold capacitor is electrically isolated by a FET input unity-gain buffer whose output is supplied to an analog-to-digital converter (A/D), for conversion to a digital word. Thus this digital word represents the peak amplitude of the analog input signal. The switch (S_1) is used to reset the hold capacitor prior to the detection process. The challenging aspects of this design is building D_1 , the ideal diode, such that

- (1) the voltage drop across the diode must be much less than an LSB of the A/D;
- (2) the diode must turn "on" and "off" almost instantaneously, relative to the frequency of the input signal;
- (3) the diode must be able to turn "off" without deviating V_{peak} by more than a fraction of an LSB due to the borrowing of charge off of hold capacitor; and
- (4) once the diode is turned "off", the hold capacitor must be electrically isolated while the A/D is converting this signal to a digital word.

Also, it is assumed that the A/D and the analog buffer are ideal and do not contribute any errors (e.g., offset voltage, gain errors, etc.).

Table 2.2-22. Comparison of simulated performance for S/H OpAmp with and without added feed-forward zero.

Performance Specification	Without Zero	With Zero
Open-Loop $3dB$ Bandwidth	$30.5MHz$	$25MHz$
Gain Margin (V^+)	$\leq -20dB$	$\leq -20dB$
Gain Margin (V^-)	$-16dB$	$-13dB$
Phase Margin (V^+)	18°	39°
Phase Margin (V^-)	29°	34°

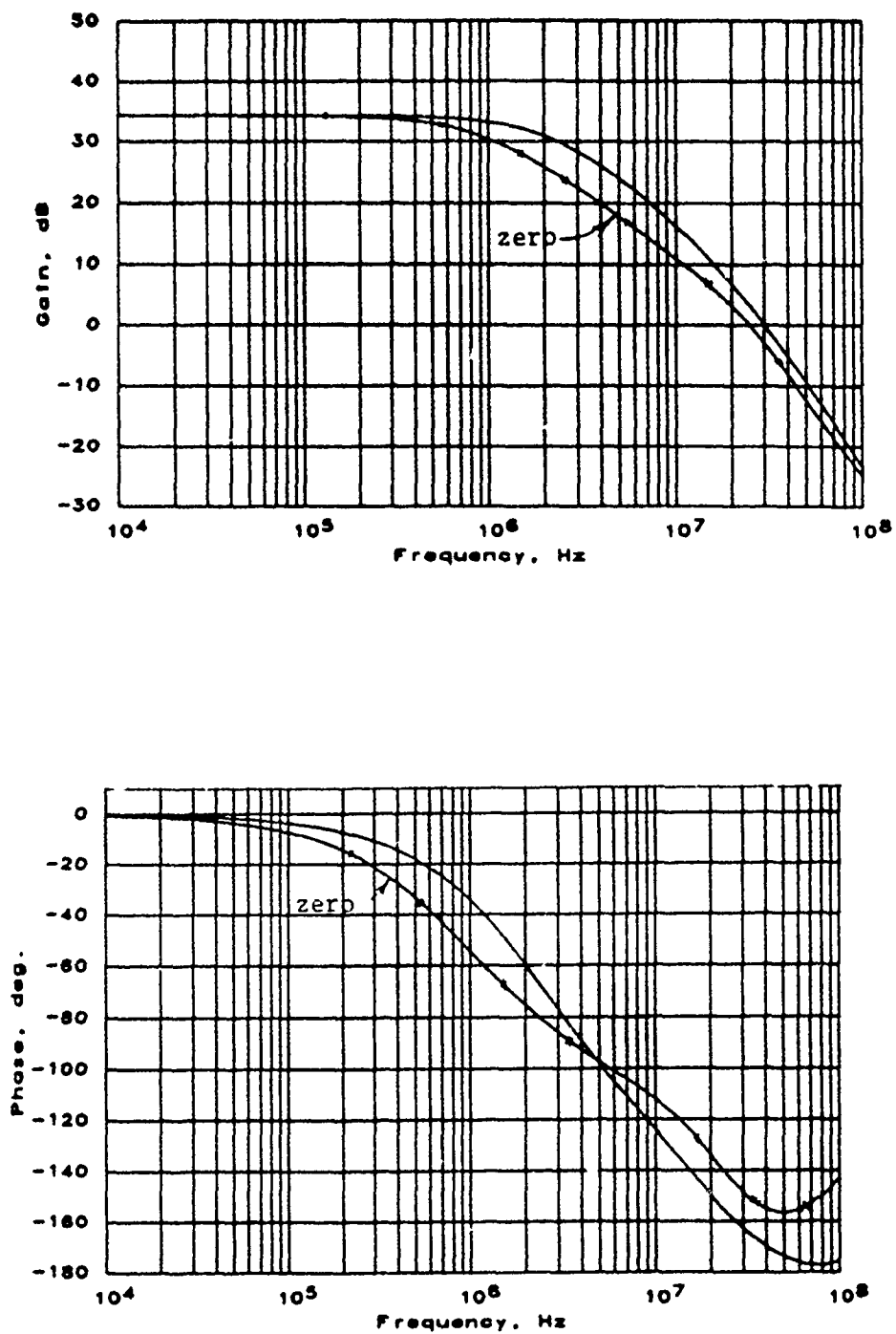


Fig. 2.2-43a. Simulated open-loop freq. resp. for $V+$ input of S/H OpAmp with added zero.

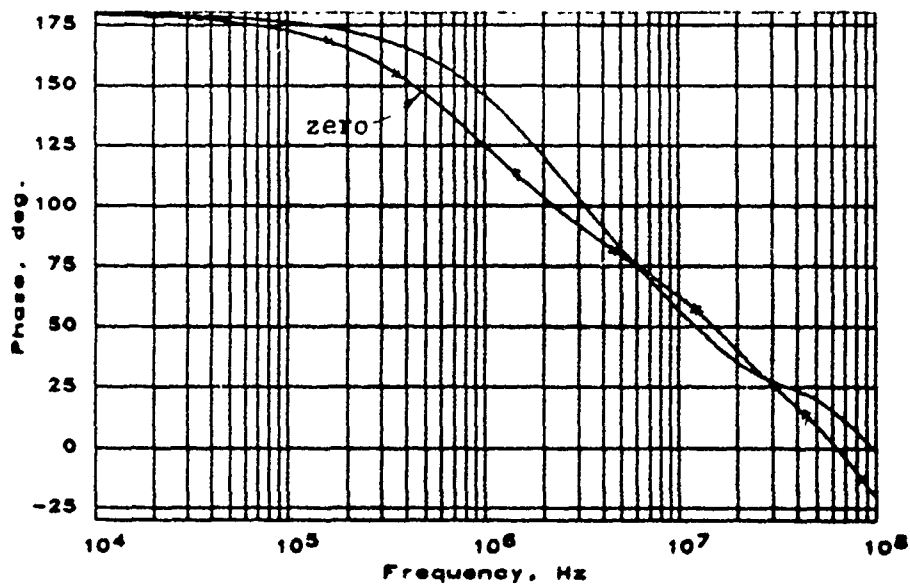
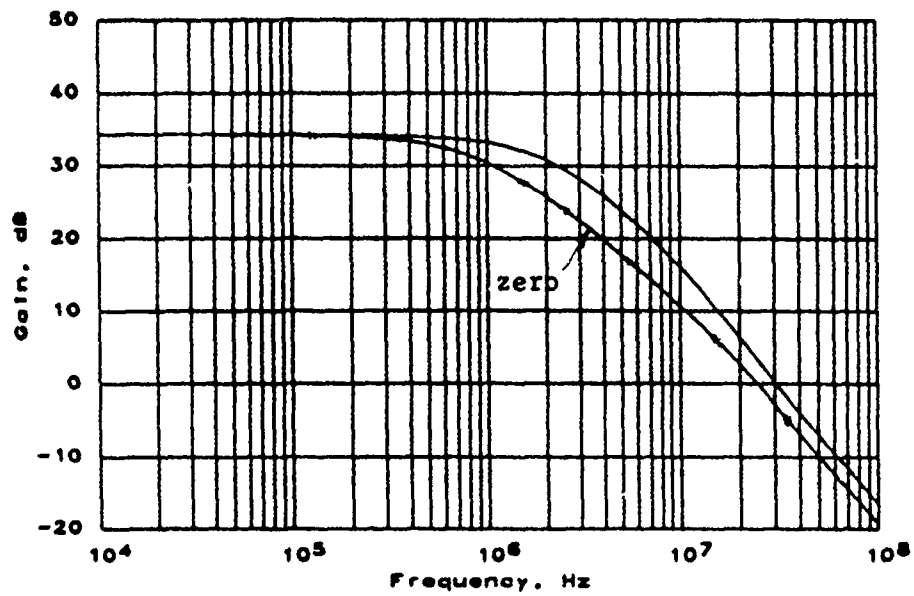


Fig. 2.2-43b. Simulated open-loop freq. resp. for V^- input of S/H OpAmp with added zero.

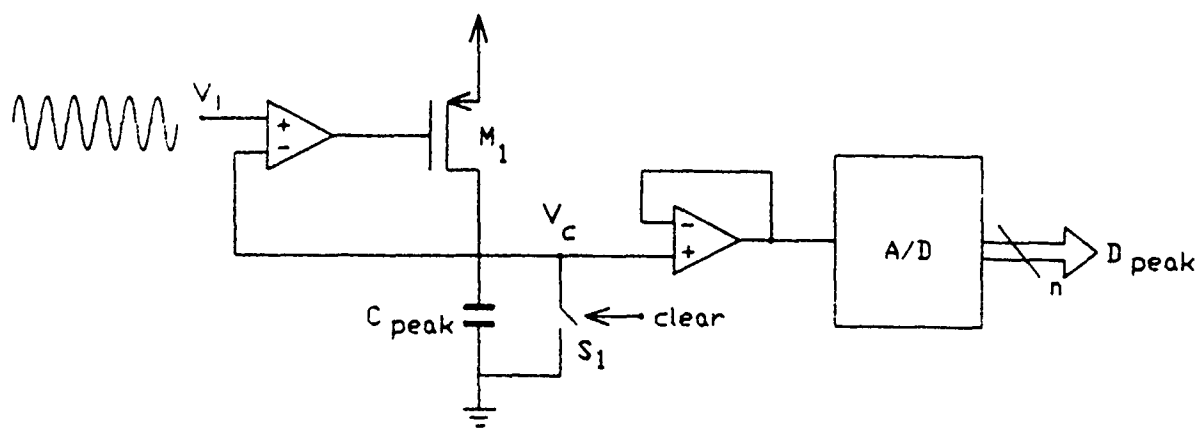


Fig. 2.2-44. Conventional Peak Detector block diagram.

The MOS version of this circuit is shown in Fig. 2.2-45, where the ideal diode is realized with an comparator or OpAmp driving the gate of a MOSFET. In this circuit if the input voltage, V_i ever gets bigger than the hold voltage, V_{peak} , then the OpAmp output will go low, turn "on" the MOSFET, charge up the hold capacitor till $V_{peak} = V_i$, at which time the OpAmp will turn "off" the MOSFET and stop the charging process.

This circuit calls for a very high-speed comparator. To better understand the speed requirements placed on the comparator/MOSFET design, consider the following mathematical representation of the time-interval in which the peak amplitude occurs in.

Given a sinusoidal signal $V_i(t) = V_{max} \cos(\omega t)$, we are interested in computing the interval of time that the amplitude of $V_i(t)$ is within $\frac{1}{2}$ an LSB (for an N bit A/D) of the peak or maximum amplitude, V_{max} . Mathematically this interval is

$$t \in (-t_o, +t_o) \text{ such that } V_i(t_o) = V_{max} \left[1 - \frac{1}{2^{N+1}} \right]. \quad (2.2 - 95)$$

Thus the length of the interval is

$$\begin{aligned} \Delta t &\stackrel{\text{def}}{=} 2t_o \\ &= \frac{2}{\omega} \cos^{-1} \left(1 - \frac{1}{2^{N+1}} \right) \\ &\approx \frac{1}{\omega \left(2^{(\frac{N}{2}-1)} \right)} \end{aligned} \quad (2.2 - 96)$$

Quantitatively, the impact of Eq. (2.2-96) is illustrated in Table 2.2-23. Nanosecond and sub-nanosecond time intervals are extremely challenging for a process technology with typical gates delays of 5-10 η sec. Thus the inherent speed requirement of turning "on" and "off" device M_1 combined with the switch feed-through effects of this devices, greatly limits the overall accuracy of this performance detection scheme and the maximum frequency of the input signal that can be properly handled.

Serial Peak Detector

The so called Serial Peak Detector as shown in Fig. 2.2-46 is an extension of the previous circuit, by replacing the analog feedback loop with a digitally controlled one. In the block diagram of Fig. 2.2-46, the input signal is continuously being compared by a high-speed high-performance comparator to a reference signal, V_{peak} which is generated by a D/A from the digital word D_{peak} . Whenever V_i exceeds V_{peak} , the output of the comparator rises rapidly, triggering an SR flip-flop, which in turns increments the digital word, D_{peak} at the end of that clock period. Thus as soon as the counter stops incrementing, the conversion process is complete and the digital representation of the peak amplitude is D_{peak} . This approach relies only on having an extremely sensitive and fast comparator and flip-flop combo.

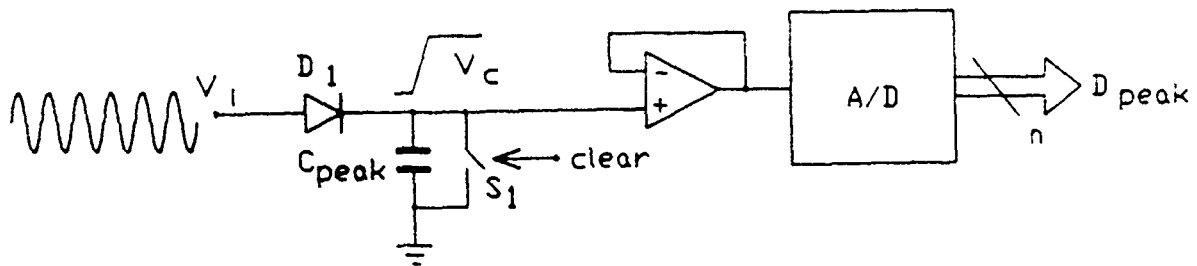


Fig. 2.2-45. Conventional MOS Peak Detector circuit schematic.

Table 2.2-23. Δt , as a function of the number of bits and input signal frequency.

N bits	frequency, ω			
	1MHz	2MHz	5MHz	10MHz
6	39.8 η sec	19.9 η sec	7.96 η sec	3.98 η sec
7	28.1 η sec	14.1 η sec	5.63 η sec	2.81 η sec
8	19.9 η sec	9.95 η sec	3.98 η sec	1.99 η sec
9	14.1 η sec	7.03 η sec	2.81 η sec	1.41 η sec
10	9.95 η sec	4.97 η sec	1.99 η sec	995psec
11	7.03 η sec	3.52 η sec	1.41 η sec	703psec
12	4.97 η sec	2.49 η sec	995psec	497psec

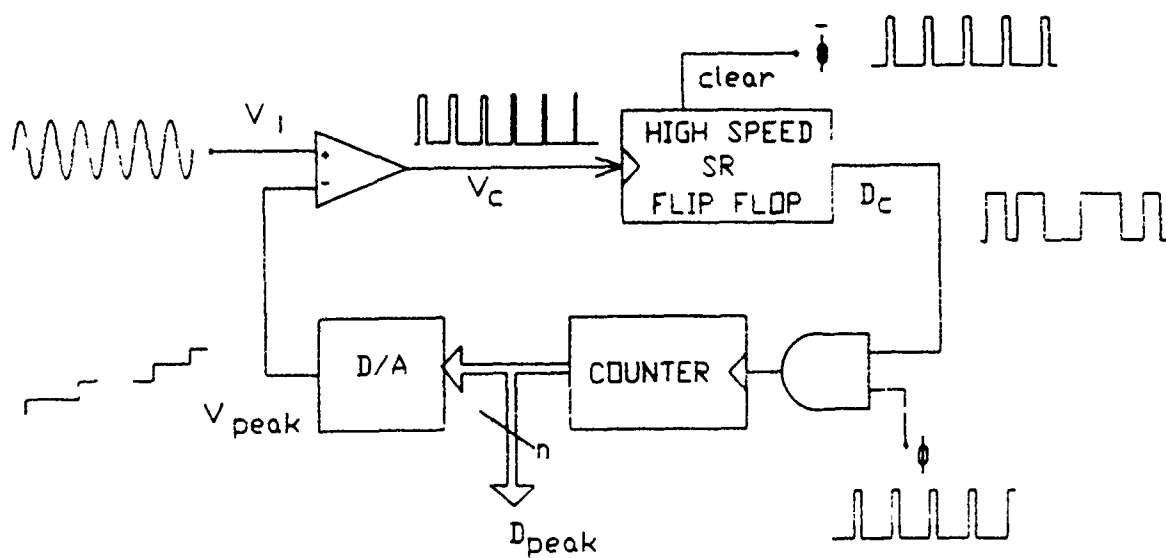


Fig. 2.2-46. Serial Peak Detector block diagram.

This same idea could be extended to a successive approximation type architecture, where the D/A is controlled by successive approximation register and logic. This would greatly reduce the conversion time, without any loss of accuracy.

Neither the conventional nor the serial architectures have been designed or fabricated at this time, only the theoretical aspects have been investigated, as depicted here.

2.3.1 The Tuning Problem-Rigorous Formulation

2.3.1. Mathematic Formulation of Tuning Problem

Assume, initially, a linear lumped system that has a transfer function

$$\frac{x_o}{x_i} = T_{ACT}(s, X) \quad (2.3.1 - 1)$$

where s is the complex frequency variable and X is the vector containing all passive and active component values/variables in the circuit. Assume further that X can be partitioned as

$$X = \begin{bmatrix} \alpha_1 \\ \dots \\ \alpha_2 \\ \dots \\ \alpha_3 \end{bmatrix} \quad (2.3.1 - 2)$$

where α_1 , α_2 , and α_3 are column vectors of lengths n_1 , n_2 , and n_3 , respectively, and where the partitioning is such that α_1 are the controllable parameters in the circuit, α_2 are the additional parameters contributing to $T(s, X)$ which have been identified and α_3 are the remaining parameters which remain unidentified.

By assumption of a linear lumped system, $T_{ACT}(s, X)$ can be written in rational fraction form as

$$T_{ACT}(s) = \frac{\sum_{i=1}^m a_i s^i}{\sum_{i=1}^n b_i s^i} \quad (2.3.1 - 3)$$

where, in general, the a_i and b_i coefficients are all functions of X . It is almost always the case that the functional expression for $T(s)$ is unknown. This will always be the case if the vector α_3 has dimension greater than or equal to 1.

Since the vector α_1 contains all controllable parameters, we can write

$$\alpha_1 = h(D) \quad (2.3.1 - 4)$$

where D is the vector of digital control variables and where the dimension of D is less than or equal to the dimension of α_1 . For the problem at hand (DCASP), the function $h(D)$ is of the form

$$\alpha_{1i} = h_i(d_i) \quad \text{for} \quad 1 \leq i \leq n_1 \quad (2.3.1 - 5)$$

where the elements of D are d_i , $i = 1, \dots, n_1$. Actually, $h_i(d_i)$ is probably monotone with d_i .

For notational convenience, it may be more convenient to express $T_{ACT}(s, X)$ in (1) in terms of D rather than in terms of X . Thus defining

$$Y = \begin{bmatrix} D \\ \dots \\ \alpha_2 \\ \dots \\ \alpha_2 \end{bmatrix} \quad (2.3.1 - 6)$$

we can write x_o/x_i as

$$\frac{x_o}{x_i} = T(s, Y) \quad (2.3.1 - 7)$$

Again, for notational convenience, if the role of D on the transfer function is to be emphasized, we will use the expression $T(D)$ where it is understood that

$$T(D) = T(s, Y) \quad (2.3.1 - 8)$$

A vector D_A or correspondingly the vector Y_A

$$Y_A = \begin{bmatrix} D_A \\ \dots \\ \alpha_2 \\ \dots \\ \alpha_3 \end{bmatrix} \quad (2.3.1 - 9)$$

where D_A is in the domain of D it is said to be an acceptable vector if $T(s, Y_A)$ meets the given specifications.

The goal in tuning is to select an acceptable vector, D_A , so that the transfer function $T(D_A)$ meets the given specifications. That is $T(D_A)$ is an acceptable transfer function. We will denote this acceptable transfer function as $T_A(s)$.

For some specifications, there may not be a vector D_A that will yield an acceptable transfer function whereas for others there may be a large number of acceptable D_A vectors. Thus, D_A is not necessarily unique.

A standard tuning strategy denoted as Strategy 1, is as outlined below.

1. Select an initial value of D , denoted as D_0 .
2. Measure some characterization parameters of $T(D_0)$, say $\phi(T(D_0))$.
3. Evaluate a cost function based upon these measurements, say $C(\phi(T(D_0)))$.
4. If C is acceptable, the tuning is complete and the acceptable transfer function realized is $T_A(s) = T(D_0)$.

5. If C is not acceptable, obtain a new estimate of D , say D_1 .

6. Repeat steps 2-5 as often as necessary.

The cost function C must be defined so as to realistically quantify the required performance specifications. With this in mind, a range of values of C can be specified such that the performance of the system is acceptable provided the cost function lies in this range. Any value of C in this range is called an acceptable value of C and any value of C outside this range is unacceptable. This is summarized more formally in the flowchart of Fig. 1.

Following Strategy 1, the tuning problem thus reduces to determining a sequence $\langle D_i \rangle$ which converges to an acceptable value of D , D_A .

Although $T_{ACT}(s, X)$ is unknown, a good model of the system is often readily available.

Returning to (1) and (2), assume that a model of the system has been obtained. That is

$$\frac{x_o}{x_i} \cong T_M(s, X_M) \quad (2.3.1 - 10)$$

where X_M is a sub vector of X which includes part or all of α_1 and part or all of α_2 . Without loss of generality, we can partition x as

$$x = \begin{bmatrix} \alpha_{1M} \\ \dots \\ \alpha_{1MC} \\ \dots \\ \alpha_{2M} \\ \dots \\ \alpha_{2MC} \\ \dots \\ \alpha_3 \end{bmatrix} \quad (2.3.1 - 11)$$

where $X_M = \begin{bmatrix} \alpha_{1M} \\ \dots \\ \alpha_{2M} \end{bmatrix}$. α_{1M} and α_{2M} are thus those parts of α_1 and α_2 respectively which are included in the model and α_{1MC} and α_{2MC} are the remaining elements of α_1 and α_2 . The reason that α_{1M} may not be all of α_1 and that α_{2M} may not be all of α_2 is to provide a simplification of the model to maintain mathematical tractability.

Again, for notational convenience, we define

$$Y_M = \begin{bmatrix} D_M \\ \dots \\ \alpha_{2M} \end{bmatrix} \quad (2.3.1 - 12)$$

where D_M are the digital control variables used to determine α_{1M} in the model. Correspondingly, the vector D_{MC} is the digital control variable used to determine α_{1MC} . The models $T_M(s, Y_M)$ and $T_M(D_M)$ are defined notationally as

$$T_M(D_M) = T_M(s, Y_M) = T_M(s, X_M) \quad (2.3.1 - 13)$$

Returning to the tuning algorithm, there is generally a desired value of the characterization parameter $\phi(D)$ or, more precisely, $\phi(T(s, X))$, say ϕ_D . The expression

$$\phi(T_M(D_M)) = \phi_D \quad (2.3.1 - 14)$$

is often mathematically tractable and the initial value of D , D_0 , is often obtained by solving (14) for D_M and then defining

$$D_0 = \begin{bmatrix} D_M \\ \vdots \\ \hat{D}_{MC} \end{bmatrix} \quad (2.3.1 - 15)$$

where \hat{D}_{MC} is some simple estimation of D_{MC} . Often \hat{D}_{MC} is of dimension 0 (i.e., all digital control variables are used in the model).

Although not shown in Fig. 1, the tuning problem is somewhat complicated because there are errors associated with the measurement of the characterization parameters; in particular,

$$\phi(D_i) = \phi_A(D_i) + e_i \quad (2.3.1 - 16)$$

where $\phi_A(D_i)$ is the actual value of the characterization parameter and e_i is the error associated with this parameter measurement.

Varying tuning algorithms based upon the above tuning strategy differ only in the way the sequence $\langle D_i \rangle$ is determined. Although this is a seemingly simple problem, the task of obtaining a optimal tuning sequence or even any sequence which converges to an acceptable value, D_A , is quite challenging. A few comments about the tuning problem follow.

First, the tuning problem can be strictly viewed as an optimization problem with the goal to determine the sequence $\langle D_i \rangle$ which minimizes the cost function. Various forms of a deepest descent algorithm are widely available for this problem. Unfortunately, even for relatively low order systems these types of algorithms tend to converge to local minimums which do not meet the desired specifications. These algorithms are typically independent of the functional form of $T_{ACT}(s, X)$ and, as such, ignore much information about the system.

Second, the tuning problem in the literature is often based upon the assumption that $T_{ACT}(s, X)$ is precisely known. Three algorithms based upon this assumption were summarized by Hoocevor and Trick [33] in 1982. Even in this case, the tuning problem is non trivial. Most of these works were based upon the assumption that all trims were to be through the unidirectional adjustment of resistor values.

2.3.3 "Simplified" System Model based Tuning Algorithm

A heuristic tuning algorithm is discussed in this section. This tuning algorithm is based upon obtaining a good model of the system which can be used in conjunction with measured parameter values to predict optimal changes in the tuning parameters. This tuning algorithm will converge in two iterations if the system model is close to the actual system. Deviations in the system model from the actual system will limit tuning accuracy. The tuning algorithm at this stage will be restricted to the second-order OTA-based biquad of Fig. 2.2-3' which is repeated in Fig. 2.3.3-1. This circuit is configured to implement the bandpass transfer function. Extension of this approach to more general system functions can be made.

The Algorithm

Assume that the filter specifications of interest are the center frequency, quality factor and maximum gain defined respectively by the equations

$$\omega'_o = \sqrt{\omega_{3dB1}\omega_{3dB2}}$$

$$Q' = \frac{\omega'_o}{\omega_{3dB1} - \omega_{3dB2}}$$

$$H'_{max} = \omega^x |T_{ACT}(j\omega)|$$

where ω_{3dB1} and ω_{3dB2} are the 3dB cutoff frequencies and $T_{ACT}(s)$ is the actual system transfer function.

If the system is exactly second-order, then ω'_o , Q' and H'_{max} are equal to the pole resonant frequency, pole Q and peak gain respectively. In the presence of parasitics which cause over-ordering of the system transfer function or other factors which cause the model to deviate from the actual system function, ω'_o and Q' will differ from the ω_o and Q of the dominant pole pair and H'_{max} will differ from the actual resonant frequency gain.

It is assumed here that ω'_o , Q' and H'_{max} , or more appropriately, estimates of these parameters denoted by $\hat{\omega}'_o$, \hat{Q}' and \hat{H}'_{max} respectively will be determined from a small number of measured samples of the system transfer function at a finite set of frequencies. Various methods of obtaining these estimates are available. Details of obtaining these estimates will not be addressed here.

The system of Fig. 11b will be assumed to be ideally modelled by the system transfer function

$$T(s) = \frac{H_{max} \frac{\omega_o^2}{Q} s}{s^2 + s \frac{\omega_o}{Q} + \omega_o^2} \quad (2.3.3 - 1)$$

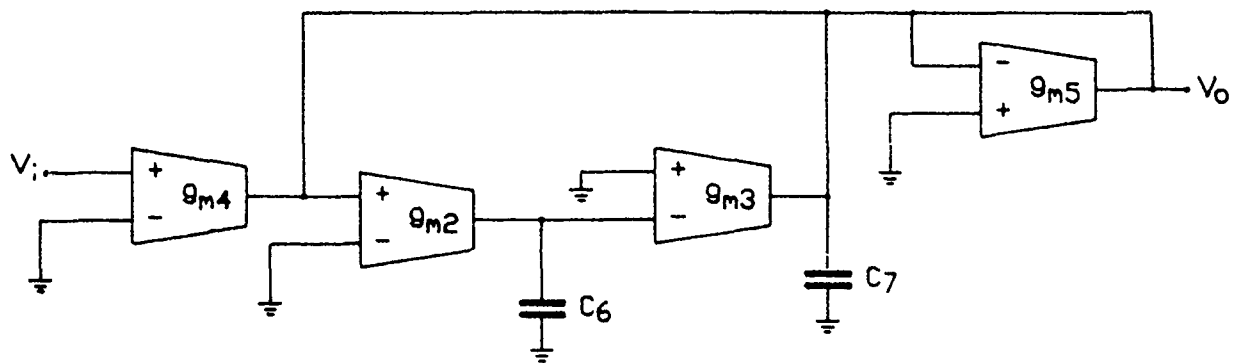


Fig. 2.3.3-1: TAC Bandpass Filter

$$\frac{V_o}{V_i} = \frac{g_{m4}C_6s}{s^2C_6C_7 + sC_6g_{m5} + g_{m2}g_{m3}}$$

$$\omega_o = \sqrt{\frac{g_{m2}g_{m3}}{C_6C_7}}$$

$$BW = \frac{g_{m5}}{C_7}$$

$$\begin{aligned}
\omega_o &= \sqrt{\frac{g_{m2}g_{m3}}{C_6C_7}}, \\
Q &= \omega_o \frac{C_7}{g_{m5}} = \frac{g_{m2}}{g_{m5}} \sqrt{\frac{C_7}{C_6}}, \\
H_{max} &= \frac{g_{m4}}{g_{m5}}.
\end{aligned} \tag{2.3.3 - 2}$$

The transconductance parameters, g_{mi} , are each controlled via two digital control words. One of these corresponds to the fine adjustment which establishes the analog output voltage of the DAC (V_c) and the other corresponds to the coarse adjustment which selects the appropriate mirror stage of the OTA. As was described in Section 2.1.3, the capacitor values, C_6 and C_7 are also digitally controllable. At this stage, we will leave C_6 and C_7 fixed and implement the proposed tuning algorithm by only adjusting the g_m parameters.

Since only three system parameters, ω_o , Q and H_{max} , are of interest, we will further reduce the degrees of freedom in our tuning algorithm to the adjustment of the parameters, g_{m2} , g_{m3} , g_{m4} and g_{m5} subject to the constraint that g_{m2} and g_{m3} are equal and adjusted together. If the system is ideal, it thus follows from (2.3.3-2) that ω_o adjustment is achievable by adjusting $g_{m2} = g_{m3}$. Q adjustment is then achievable by adjusting g_{m5} . Note that adjusting Q does not affect ω_o . Finally, H_{max} adjustment is achievable by adjusting g_{m4} . Note that adjusting H_{max} via g_{m4} ideally does not affect either the previous ω_o or Q adjustment.

In the presence of over-ordering due to inclusion of parasitics in the system model, the complete independence of adjustment of the three system parameters will be lost. For modest parasitics, however, the interdependence between these control parameters will be weak but may force iteration during tuning to obtain good system performance. At this stage we shall consider only V_c , the fine control of the OTA, as the control parameter for tuning the filters. The control mechanism relating the g_m of the OTA's to their control voltage or tail voltage, V_{ci} , is characterized by the linear equation

$$g_{m_i}(V_{c_i}) = M_i K'_i \frac{W_i}{L_i} [V_{c_i} - V_{SS} - V_{T_i}], \quad \text{for } i = 1, \dots, 5, \tag{2.3.3 - 3}$$

where K'_i , and V_{T_i} are the process dependent transconductance and threshold voltage parameters M_i is the output stage mirror gain and W_i , L_i , are the width and length of the input differential pair devices. This can also be expressed as,

$$g_{m_i}(V_{c_i}) = m_i(K'_i, M_i, W_i, L_i) [V_{c_i} + b_i(V_{T_i})] \tag{2.3.3 - 4}$$

where m_i and b_i model the slope and x-intercept of g_{m_i} as a function of the control voltage (V_{c_i}) and the process and design parameters (K'_i , V_{T_i} , M_i , W_i and L_i).

Capacitors, C_6 and C_7 are selected from an array of discrete capacitor values modelled by the following expression

$$C_j = A_j C_{polyj}, \quad \text{for } j = 6, 7 \tag{2.3.3 - 5}$$

where A_j is the designed capacitor area for each element of the capacitor array, and C_{poly_j} is the process dependent capacitance density of poly-1 to poly-2.

If the parameters m_i and b_i are known and if the system is perfectly characterized by (2.3.3-1) and (2.3.3-2), then (2.3.3-4), (2.3.3-1) and (2.3.3-2) can be solved simultaneously for the control voltages V_{c2} , V_{c3} , V_{c4} , and V_{c5} thus solving the tuning problem. Unfortunately, process parameter variations in K'_i , V_{Ti} , W_i , L_i and the mirror gains makes exact tuning by deterministic solution of these equations impossible.

A discussion of a sequential tuning algorithm based upon measurements of the actual system transfer function follows. If the system model (2.3.3-1) is ideal and if system function measurements are errorless, this algorithm will converge after two iterations. In practice, modelling and measurement errors do exist thus necessitating additional iteration. A systematic discussion of the tuning algorithm based upon assuming an ideal system model follows.

- (1) Set the initial process (control) parameters ($M'_i{}^{(1)}$, $K'_i{}^{(1)}$, V_{Ti} , L_i and W_i or, alternately, $m_i{}^{(1)}$ and $b_i{}^{(1)}$ to their ideal (nominal) values.
- (2) Measure $\omega_o'{}^{(1)}$, $Q'{}^{(1)}$ and $H'_{max}{}^{(1)}$ of the physical filter.
- (3) Make an improved estimate of the system process parameters m_i and b_i of (2.3.3-4) for $i = 1, 3, 4, 5$.
- (4) Theoretically adjust ω_o' , Q' and H'_{max} to their design values using the simplified model for the control system with the updated estimates for control parameters.
- (5) Measure $\omega_o'{}^{(2)}$, $Q'{}^{(2)}$ and $H'_{max}{}^{(2)}$ of the physical filter.
- (6) Update parameters of step (3). Make an improved estimate of the system process parameters m_i and b_i based upon the measurements at Steps (2) and (5).
- (7) Repeat the adjustments or tuning process of Step (4) with a more exact model for the control system.

Thus after two sets of measurements the complete system model has been extracted and the system "tuned".

The following is a more detailed step by step procedure, describing the specific system models and design equations used by this tuning algorithm.

- (1) Set the initial control parameters g_{m_2} through g_{m_5} of the OTA's, and the capacitors C_6 , C_7 to their ideal values, assuming $g_{m_2} = g_{m_3}$, using the equation (2.3.3-2).

From (2.3.3-3) and (2.3.3-4), the parameters m_i and b_i at the first iteration, denoted

by $m_i^{(1)}$ and $b_i^{(1)}$, are given by

$$b_i^{(1)} = - \left(V_{SS} + V_{T_i}^{(1)} \right) \quad i = 2, 3, 4, 5 \quad (2.3.3 - 6)$$

$$m_i^{(1)} = \frac{M_i^{(1)} K_i^{(1)} W_i^{(1)}}{L_i^{(1)}} \quad i = 2, 3, 4, 5 \quad (2.3.3 - 7)$$

where $V_{T_i}^{(1)}$, $M_i^{(1)}$, $K_i^{(1)}$, $\omega_i^{(1)}$, and $L_i^{(1)}$ are the nominal values of the process and design parameters.

From (2.3.3-2) and (2.3.3-4), the control voltages at the first iteration thus become,

$$V_{c_i}^{(1)} = \frac{\bar{\omega}_o C^{(1)}}{m_i^{(1)}} - b_i^{(1)} \quad i = 2, 3 \quad (2.3.3 - 8)$$

where $C^{(1)}$ is the nominal value of C_6 and C_7 which are assumed equal.

To obtain Q control via g_{m_5} , observe from (2.3.3-2) that with $C_6 = C_7$

$$g_{m_5} = \frac{g_{m_2}}{Q} = \frac{\omega_o C}{Q} \quad (2.3.3 - 9)$$

Thus from (2.3.3-4) and (2.3.3-9)

$$V_{C_5}^{(1)} = \frac{C^{(1)} \bar{\omega}_o}{\bar{Q} m_5^{(1)}} - b_5^{(1)} \quad (2.3.3 - 10)$$

Note that the coarse adjustment, $M_5^{(1)}$, needs to be set so that V_{C_5} , as provided by (2.3.3-10) can assume an acceptable value. Typically, one would set, to within the available quantization range,

$$M_5^{(1)} \simeq \frac{M_2^{(1)}}{Q} \quad (2.3.3 - 11)$$

Finally, from (2.3.3-2) the control voltage $V_{C_4}^{(1)}$, must be set so that

$$g_{m_4} = g_{m_5} H_{max} = \frac{H_{max} \omega_o C}{Q} \quad (2.3.3 - 12)$$

which, from (2.3.3-4) becomes

$$V_{C_4}^{(1)} = \frac{C^{(1)} \bar{\omega}_o \bar{H}_{max}}{\bar{Q} m_4^{(1)}} - b_4^{(1)} \quad (2.3.3 - 13)$$

As for $M_4^{(1)}$, the coarse mirror gain should be set so that, to within the available quantization range,

$$M_4^{(1)} \simeq \frac{M_2^{(1)} \bar{H}_{max}}{\bar{Q}} \quad (2.3.3 - 14)$$

(2) Measure the actual $\omega_o^{(1)}$, $Q^{(1)}$ and $H_{maz}^{(1)}$ of the physical filter.

(3) and (4) The updated values of m_i and b_i will be denoted as $m_i^{(2)}$ and $b_i^{(2)}$. Since only three measurements have been made, $\omega_o^{(1)}$, $Q^{(1)}$ and $H_{maz}^{(1)}$, we have only three degrees of freedom from which to estimate the 6 parameters $m_2^{(2)}$, $m_4^{(2)}$, $m_5^{(2)}$, $b_2^{(2)}$, $b_3^{(2)}$ and $b_5^{(2)}$. At this iteration step it will be assumed that

$$b_i^{(2)} = b_i^{(1)} \quad i = 2, 3, 4, 5 \quad (2.3.3 - 15)$$

To obtain $m_2^{(2)}$, observe from (2.3.3-2) and (2.3.3-4) that if $g_{m_2} = g_{m_3}$, then

$$\omega_o = \frac{m_2(V_{C2} + b_2)}{\sqrt{C_6 C_7}} \quad (2.3.3 - 16)$$

Solving for m_2 with the measured value of $\omega_o'(\omega_o'^{(1)})$ and assuming $C_6 = C_7 = C^{(1)}$, we obtain the approximate expression for the updated values of m_2 and m_3

$$m_2^{(2)} = m_3^{(2)} = \frac{\omega_o'^{(1)} C^{(1)}}{V_{C2}^{(1)} + b_2^{(1)}} \quad (2.3.3 - 17)$$

Substituting this for m_2 in (2.3.3-16), we obtain

$$V_{C2}^{(2)} = V_{C3}^{(2)} = \frac{\bar{\omega}_o}{\omega_o'^{(1)}} \left[V_{C2}^{(1)} + b_2^{(1)} \right] - b_2^{(1)} \quad (2.3.3 - 18)$$

To obtain $m_5^{(2)}$, observe from (2.3.3-2) and (2.3.3-4) that

$$m_5 = \frac{\omega_o C_7}{(V_{C5} + b_5) Q} \quad (2.3.3 - 19)$$

Thus, we may approximate the next iterate for m_5 by

$$m_5^{(2)} = \frac{\omega_o'^{(1)} C_7}{(V_{C5}^{(1)} + b_5^{(1)}) Q^{(1)}} \quad (2.3.3 - 20)$$

Substituting this into (2.3.3-19), we obtain a new estimate of V_{C5} denoted by

$$V_{C5}^{(2)} = \frac{Q'^{(1)} \bar{\omega}_o}{\bar{Q} \omega_o'^{(1)}} \left(V_{C5}^{(1)} + b_5^{(1)} \right) - b_5^{(1)} \quad (2.3.3 - 21)$$

Finally, to obtain $m_4^{(2)}$, observe from (2.3.3-2) and (2.3.3-4) that

$$m_4 = H'_{maz} m_5 \left(\frac{V_{C5} + b_5}{V_{C4} + b_4} \right) \quad (2.3.3 - 22)$$

Thus, we may approximate the next iterate for m_4 by

$$m_4^{(2)} \simeq H'_{maz} m_5^{(1)} \left(\frac{V_{C5}^{(1)} + b_5^{(1)}}{V_{C4}^{(1)} + b_4^{(1)}} \right) \quad (2.3.3 - 23)$$

Substituting this into (2.3.3-22) for m_4 and solving for V_{C4} , we obtain a new estimate for V_{C4} denoted by

$$V_{C4}^{(2)} = \frac{\bar{H}_{maz} m_5^{(1)}}{H'_{maz} m_5^{(2)}} \left(V_{C4}^{(1)} + b_4^{(1)} \right) - b_4^{(1)} \quad (2.3.3 - 24)$$

(5) Measure $\omega_o'^{(2)}$, $Q'^{(2)}$ and H'_{maz} of the physical filter with the updated control voltages, $V_{ci}^{(2)}$.

(6) and (7) To obtain $m_2^{(3)}$ and $b_2^{(3)}$ when $g_{m_2} = g_{m_3}$, observe from (2.3.3-16) that

$$\omega_o'^{(1)} = \frac{m_2(V_{C2}^{(1)} + b_2)}{\sqrt{C_6 C_7}} \quad (2.3.3 - 25)$$

$$\omega_o'^{(2)} = \frac{m_2(V_{C2}^{(2)} + b_2)}{\sqrt{C_6 C_7}} \quad (2.3.3 - 26)$$

Solving these two equations simultaneously, we obtain the exact values for m_2 and b_2 which are denoted by $m_2^{(3)}$ and $b_2^{(3)}$ as given by the expressions

$$b_2^{(3)} = \frac{V_{C2}^{(2)} \omega_o'^{(1)} - V_{C2}^{(1)} \omega_o'^{(2)}}{\omega_o'^{(2)} - \omega_o'^{(1)}} \quad (2.3.3 - 27)$$

$$m_2^{(3)} = \sqrt{C_6 C_7} \frac{(\omega_o'^{(1)} - \omega_o'^{(2)})}{(V_{C2}^{(1)} - V_{C2}^{(2)})} \quad (2.3.3 - 28)$$

Thus from (2.3.3-16)

$$V_{C2}^{(3)} = \frac{\bar{\omega}_o(V_{C2}^{(1)} - V_{C2}^{(2)})}{(\omega_o'^{(1)} - \omega_o'^{(2)})} - b_2^{(3)} \quad (2.3.3 - 29)$$

To obtain $m_5^{(3)}$ and $b_5^{(3)}$, observe from (2.3.3-19) that

$$\frac{\omega_o^{(1)} C_7}{Q^{(1)}} = m_5(V_{C5}^{(1)} + b_5) \quad (2.3.3 - 30)$$

$$\frac{\omega_o^{(2)} C_7}{Q^{(2)}} = m_5(V_{C5}^{(2)} + b_5) \quad (2.3.3 - 31)$$

Solving these two equations simultaneously, we obtain the exact values for m_5 and b_5 which are denoted by $m_5^{(3)}$ and $b_5^{(3)}$ as given by the expressions

$$b_5^{(3)} = \frac{V_{C5}^{(1)} Q'^{(1)} \omega_o'^{(2)} - V_{C5}^{(2)} Q'^{(2)} \omega_o'^{(1)}}{\omega_o'^{(1)} Q'^{(2)} - Q'^{(1)} \omega_o'^{(2)}} \quad (2.3.3 - 32)$$

$$m_5^{(3)} = C_7 \frac{(\omega_o'^{(1)} Q'^{(2)} - \omega_o'^{(2)} Q'^{(1)})}{Q'^{(1)} Q'^{(2)} (V_{C5}^{(1)} - V_{C5}^{(2)})} \quad (2.3.3 - 33)$$

Thus from (2.3.3-19)

$$V_{C5}^{(3)} = \frac{\bar{\omega}_o}{\bar{Q}} \frac{C_7}{m_5^{(3)}} - b_5^{(3)} \quad (2.3.3 - 34)$$

Finally, from (2.3.3-22) we obtain

$$H_{maz}'^{(1)} = \frac{m_4(V_{C4}^{(1)} + b_4)}{m_5(V_{C5}^{(3)} + b_5)} \quad (2.3.3 - 35)$$

$$H_{maz}'^{(2)} = \frac{m_4(V_{C4}^{(2)} + b_4)}{m_5(V_{C5}^{(3)} + b_5)} \quad (2.3.3 - 36)$$

where m_5 and b_5 are the exact values for m_5 and b_5 as denoted by $m_5^{(3)}$ and $b_5^{(3)}$ in (2.3.3-32) and (2.3.3-33). Solving these two equations simultaneously, we obtain the exact values for m_4 and b_4 which are denoted by $m_4^{(3)}$ and $b_4^{(3)}$ as given by the expressions

$$b_4^{(3)} = \frac{V_{C4}^{(1)} H_{maz}'^{(2)} - V_{C4}^{(2)} H_{maz}'^{(1)}}{H_{maz}'^{(1)} - H_{maz}'^{(2)}} \quad (2.3.3 - 37)$$

$$m_4^{(3)} = m_5(V_{C5}^{(3)} + b_5) \frac{(H_{maz}'^{(1)} - H_{maz}'^{(2)})}{V_{C4}^{(1)} - V_{C4}^{(2)}} \quad (2.3.3 - 38)$$

Thus from (2.3.3-22)

$$V_{C4}^{(3)} = \frac{\bar{H}_{maz}(m_5)(V_{C5}^{(3)} + b_5)}{m_4^{(3)}} - b_4^{(3)} \quad (2.3.3 - 39)$$

Discussion

The main advantage of this algorithm, is that it converges to a solution with only two sets of frequency response measurements. This offers an improvement in speed over other approaches.

There are limitations associated with this algorithm, since it relies heavily on a priori knowing the exact model for the physical control system. The primary limitations are

- (a) mismatches in g_{m_2} and g_{m_3}
- (b) measurement or computational errors
- (c) transfer function over-ordering
- (d) high sensitivities to measured parameters

These limitations become more severe at the second stage of the iteration (e.g., Step (6) above) thus justifying stopping after the first stage in some applications. This algorithm will be most useful for obtaining an initial approximation (coarse adjustment) or a tune when the system model very closely approximates the actual system. This initial coarse adjustment may be very important if a standard optimization algorithm is used since many optimization algorithms are inherently plagued by convergence to local minimums when the initial characteristic parameters are not sufficiently close to those corresponding to the global minimums.

2.3.4 TUNING ALGORITHM USING CONVENTIONAL OPTIMIZATION

There are several general tuning algorithms for conventional active RC filters reported in the literature [33] - [34]. Optimization has been used in many aspects of circuit design [35-38]. One of these methods, the least squares method [33, 39] consists of minimizing the error, E , between the actual and the desired transfer function. This is formulated as:

$$E = \|F_{ACT}(\omega, \alpha_1, \alpha_{20} + \Delta\alpha_{20}) - F_{DES}(\omega, \alpha_{10}, \alpha_{20})\|_2 \quad (2.3.4 - 1)$$

$$E_{min} = \min_{\alpha_1} E = \min_{\alpha_1} \|F_{ACT}(\omega, \alpha_1, \alpha_{20} + \Delta\alpha_{20}) - F_{DES}(\omega, \alpha_{10}, \alpha_{20})\|_2 \quad (2.3.4 - 2)$$

where F_{DES} is the desired transfer function, F_{ACT} is the actual transfer function, ω is the radian frequency, α_1 is the vector of controllable (tuning) parameters, α_2 is the vector of remaining components (assumed measurable), α_{10} and α_{20} are the nominal values, and $\Delta\alpha_{20}$ is assumed to be the undesired but measurable change in the untuned values. The norm specified in (2.3.4-1) is based upon sampling F_{ACT} and F_{DES} at a predetermined fixed and finite set of frequencies, $\omega_1, \dots, \omega_k$. In this work, the norm was restricted to the sum of the squares of the functional differences and the functions themselves were the desired and actual transfer function magnitudes. The functional form of F_{ACT} may be unknown with the values of F_{ACT} being obtained by actual measurements. Later, we will discuss the tuning problem when α_2 consists not only of measurable but several unmeasurable components.

The general solution of (2.3.4-2) (following Strategy 1 presented in Section 2.3.1) using conventional optimization consists of:

Step 1) Select initial vectors α_{10} and α_{20} to obtain F_{DES} .

Step 2) Select the tuning frequencies and measure F_{ACT} and calculate F_{DES} .

Step 3) Evaluate (2.3.4-1), if E is an acceptable predetermined small value the tuning is complete, then go to Step 6.

Step 4) If E is not acceptable modify α_1 as $\alpha_{1k} + \Delta\alpha_1$. Note that $\Delta\alpha_1$ must be chosen according to an optimization strategy. α_{1k} is the previous value of α_1 obtained at the $k - 1$ step in the iteration. By definition, this iteration starts with α_{10}

Step 5) Go back to Step 2.

Step 6) Tuning has been completed and the correction vector $\Delta\alpha_1$ has been found that minimizes (2.3.4-1).

The optimization strategies used in this report include:

- (i) Methods using only the functional values, denoted as *direct methods* [39, 40].
- (ii) The methods making use of both functional values as well as the first-order derivatives. These methods are called *gradient methods* [39, 41, 42].

The methods in category (i) are often less efficient than methods in category (ii). However, there are situations where methods in category (ii) cannot be applied because no first-order derivative information is available. In other cases, where the error (or cost) function has many local extrema, the methods in (ii) may be more prone to converge to unacceptable local extrema.

The *direct methods* explore a neighborhood of a chosen initial point α_{10} . If a promising direction is found, then the error function is evaluated in the same direction by increasing the step size until no points α_1 with lower error function is located. After several consecutive step size decreases, a new exploratory search is initiated. These methods try to find directions that minimize the error function and follow those directions. The fundamental differences among the direct methods is the way they generate the exploratory directions.

Rosenbrock's method [39] involves an exploratory search by generating n mutually orthogonal directions in each cycle. A cycle ends when at least one trial has been successful and one trial failed in every direction.

Powell's method [40] is different from Rosenbrock's in that the exploratory search tries to locate the minima rather than points with lower error functional values and that search along the conjugate directions rather than orthogonal directions.

Gradient Methods [39, 41, 42] use the fact that the negative of the gradient vector r_k gives the direction of the fastest decrease of the error function $E(\alpha_1)$ in the neighborhood of α_1 . Assume that starting from α_{10} , vectors $\alpha_{11}, \dots, \alpha_{1n}$ have been generated. The next vector $\alpha_{1(k+1)}$ is chosen as

$$\alpha_{1(1+k)} = \alpha_{1(k)} - t_k r_k \quad (2.3.4 - 3)$$

where $r_k = \nabla E(\alpha_{1k})$ and t_k is some positive scalar quantity and is determined by solving the one-dimensional minimization problem

$$\min_{t_k > 0} E(\alpha_{1k} - t_k r_k) \quad (2.3.4 - 4)$$

This version of the gradient method is called the optimal gradient method. Some of the most popular gradient methods have been reported by Fletcher and Powell [41]. In particular, for the steepest descent, we have

$$r_k = \frac{\nabla E_k}{\|\nabla E\|} \quad (2.3.4 - 5)$$

for the Fletcher and Powell Technique [41]

$$r_k = H_k \nabla E_k \quad (2.3.4 - 6)$$

where H_k is the k^{th} approximation to the inverse of the Hessian matrix H , ($H_{ij} = \partial^2 E / \partial \alpha_{1i} \partial \alpha_{1j}$). A linear search is required for this approximation. R. Fletcher [42] in 1970 reported an approach based upon a variable metric method (VMM) in which the linear search sub-problem no longer becomes necessary.

A "hard" problem with respect to optimization can be characterized in a number of ways:

- i) Large number of independent variables
- ii) Large number of local minima
- iii) Large number of solutions, many of which are unacceptable
- iv) Little knowledge of the solution or whether it exists
- v) Complicated constraints on the variables
- vi) Highly nonlinear space in the region of the solution
- vii) The order of the system model is lower than the (physical) system to be optimized (Over-Ordering).

Characteristic vii) is due to the fact that all (or some) parasitic components are neglected or can not be measured in the physical system model of systems such as the DCASP structure discussed previously. The problem of functionally tuning most filter structures in general and specifically, the problem of tuning OTA-C filters using optimization techniques is difficult, since most of the above characteristics are inherent in these circuit structures.

Remarks

• Selection of Optimization Algorithm

It is important that a good starting point (initial guess) be determined for a given circuit before an attempt is made to tune that circuit. Observe that for a poor initial guess, gradient information is far too local and aids very little. In fact, in very nonlinear problems, truncated Taylor Series methods using derivative information perform poorly. Besides, in these cases a Hessian approximation by first derivatives is as ineffective, mathematically, as any quasi-Newton technique. Direct methods in many cases can provide, in particular when a poor initial guess is available, feasible solutions, although they have poor convergence properties close to the solution. An optimum switching procedure for changing from one algorithm to another may be desirable.

•Selection of Frequency Points and Weighting

Indiscriminate use of excess points might lead to ill conditioning of the resulting system of non-linear equations. It is often recommended to take twice the number of variable elements as an acceptable number of frequency points. On the other hand, the number of evaluations of the error function as well as the number of frequency points must be kept small to reduce the tuning time. Besides, weighting applied to a few optimally placed frequency points is usually needed. There are cases where a fixed weighting or sampling strategy is not convenient over the entire optimization process.

Results and Discussion

Conventional direct optimization algorithms of Rosenbrock [39] and Powell [40] were applied to tune several sample filters. Convergence for second-order transfer functions or cascade of second-order transfer functions was relatively easy to obtain for good initial guesses.

For high-order transfer functions we have applied the direct optimization techniques to a fourth-order transfer function. We split this problem into two cases; a) Product of two second-order transfer functions, and b) Ratio of two fourth-order polynomials. In both cases, for poor initial guesses the convergence was poor. For good initial guesses, the ratio of polynomials (Case b)) model presented convergence problems.

For illustration purposes consider the following cases. Consider initially a 4th order Chebyshev Bandpass Filter scaled at $\omega_o = 1$. The general form of the transfer function is characterized by:

$$H_{DES1}(s) = \frac{b_{11}s}{a_{21}s^2 + a_{11}s + a_{01}} \cdot \frac{b_{12}s}{a_{22}s^2 + a_{12}s + a_{02}} \quad (2.3.4 - -7)$$

H_{DES} can also be expressed in rational fraction form as:

$$H_{DES2}(s) = \frac{B_2s^2}{A_4s^4 + A_3s^3 + A_2s^2 + A_1s + A_0} \quad (2.3.4 - -8)$$

The desired coefficient values are assumed to be:

$$\{b_{11}, a_{21}, a_{11}, a_{01}\} = \{0.146, 1, 1.1069, 0.08706\}$$

$$\{b_{12}, a_{22}, a_{12}, a_{02}\} = \{0.130, 1, 0.88149, 0.07751\}$$

$$\{B_2, A_4, A_3, A_2, A_1, A_0\} = \{0.01898, 1, 0.16457, 1.9951, 0.16254, 0.97572\}$$

The importance of the initial guess (preliminary design) in filter design optimization is

emphasized by the following numerical examples. In all cases 16 frequency points were chosen and the Rosenbrock Optimization Technique was employed to obtain the final design.

Fig. 2.3.4-1 shows the frequency responses of the initial design, desired and final design for the rational fraction form of the response (2.3.4-8) $H_{DES2}(s)$. The final design is based upon convergence of the Rosenbrock algorithm to a local minimum. Similarly, Fig. 2.3.4-2 and Fig. 2.3.4-3 illustrate the optimization for $H_{DES1}(s)$ of (2.3.4-7). The initial guess for the later two optimizations were close enough to provide a final design matching very well the desired response for $H_{DES1}(s)$.

Observations

Solutions are very much dependent on the initial (guess) design. Even though an initial design $\{b_{11}, a_{21}, a_{11}, a_{01}\}^0 = \{0.09, 1, .06, 1.0\}$ and $\{b_{12}, a_{22}, a_{12}, a_{02}\}^0 = \{0.095, 1.0, .056, .08\}$ for the optimization depicted in Fig. 2.3.4-1 has a shape very similar to that of the desired response, the final response differs significantly from the desired response.

The initial guess $\{b_{11}, a_{21}, a_{11}, a_{01}\}^0 = \{0.9, 1, 0.5, 40\}$ and $\{b_{12}, a_{22}, a_{12}, a_{02}\}^0 = \{0.8, 1, 0.487, 50\}$ for the optimization depicted in Fig. 2.3.4-2 is relatively far from the desired response; however, convergence to the desired response was achieved. The initial guess for the optimization of Fig. 2.3.4-3 $\{b_{11}, a_{21}, a_{11}, a_{01}\}^0 = \{0.14, 1.0, 0.088, 100\}$ and $\{b_{12}, a_{22}, a_{12}, a_{02}\}^0 = \{0.12, 1.0, 0.076, 0.98\}$ has a very different shape from the desired response but the algorithm is capable of meeting specifications in the final design.

The optimization problem is difficult, in particular, when one or more of the following conditions exist:

- Large number of independent variables
- Large number of local minima
- Little knowledge of the solution or whether it exists
- Complicated constraints on the variables
- Highly nonlinear space in the region of the solution
- The order of the system model is lower than the (physical) system to be optimized.

The tuning of OTA-C filters involves most of the problems above mentioned.

When a good model of the system is available the convergence of the optimization algorithm improved drastically. These results are presented in Section. 2.3.3, with a modified Newton-Raphson technique. However, when the order of this physical system is greater than the order of the simplified model, severe problems of convergence arise.

CHEBYSHEV BANDPASS FILTER

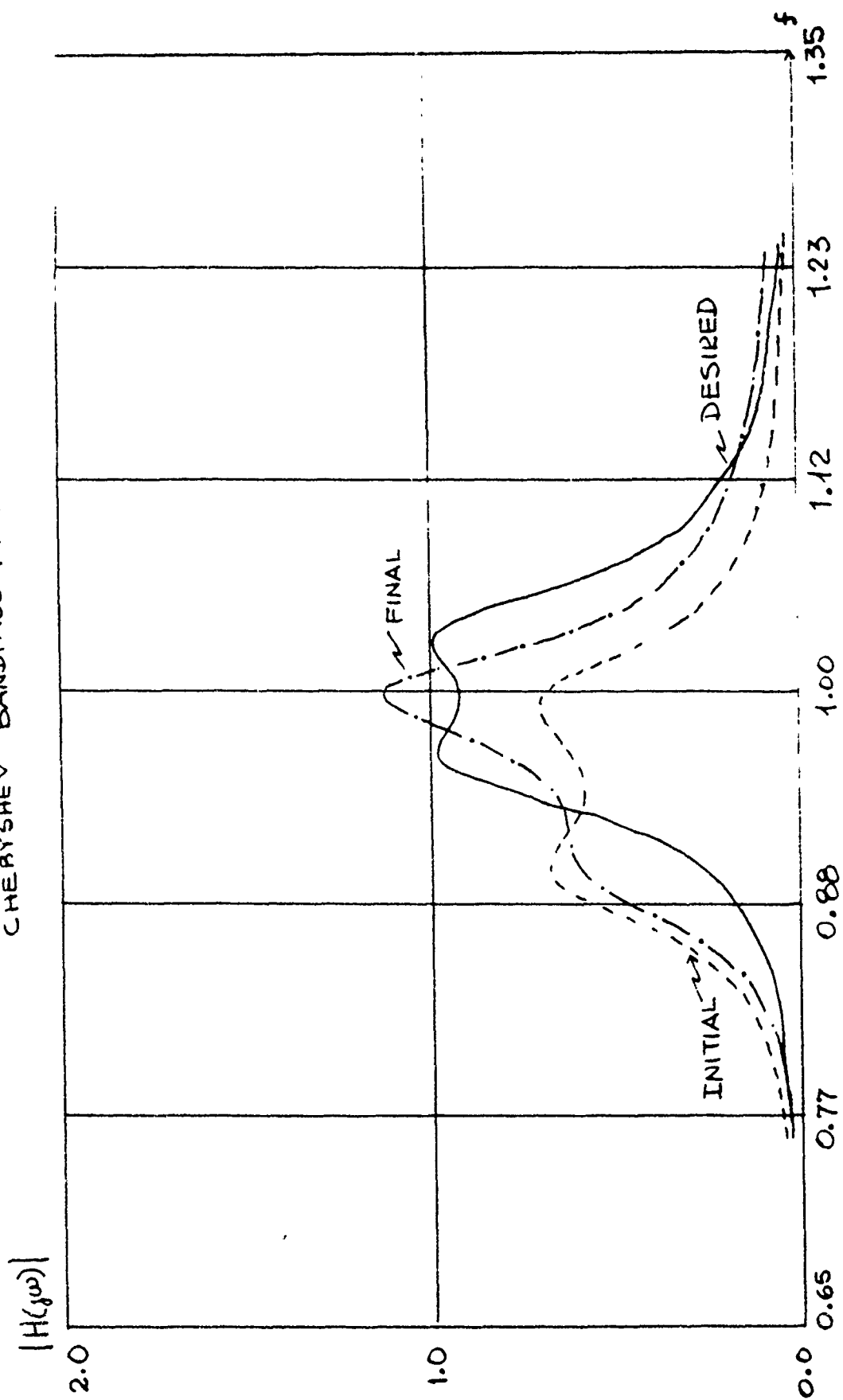


Fig. 2.3.4-1 Chebyshev Bandpass Filter

Chebyshev BP FILTER

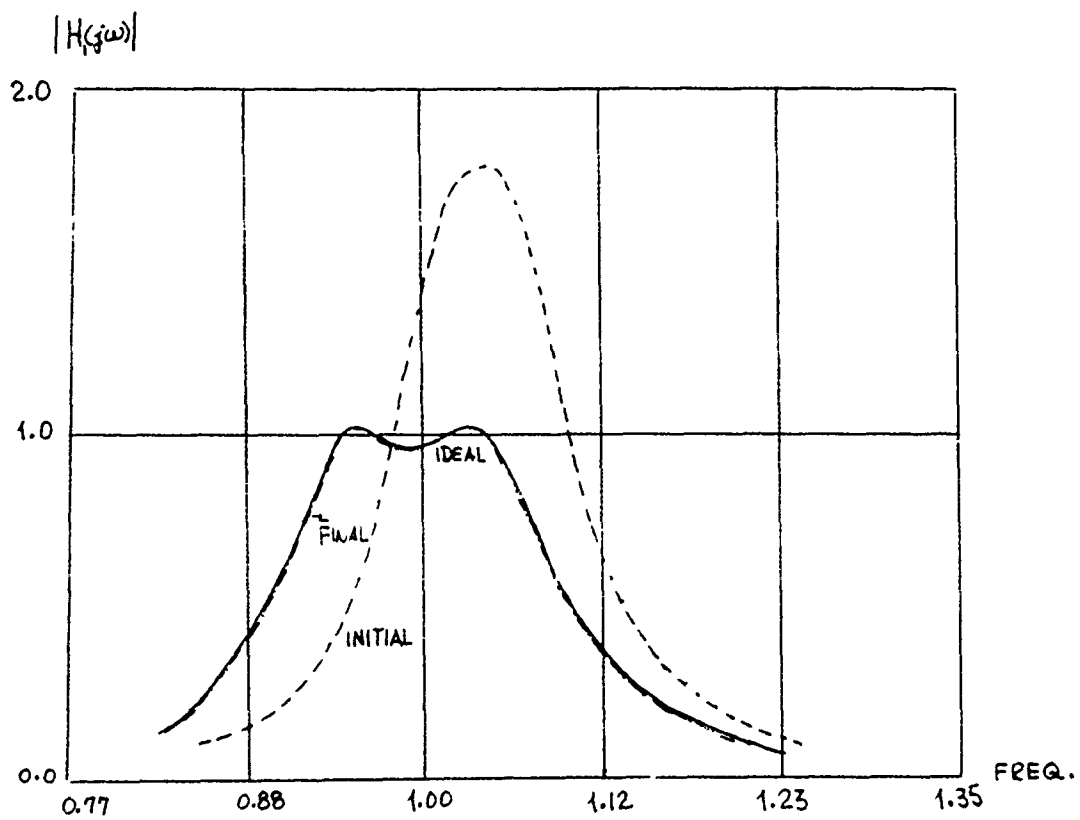


Fig. 2.3.4-2 Chebyshev BP Filter

Chebyshev BP Filter

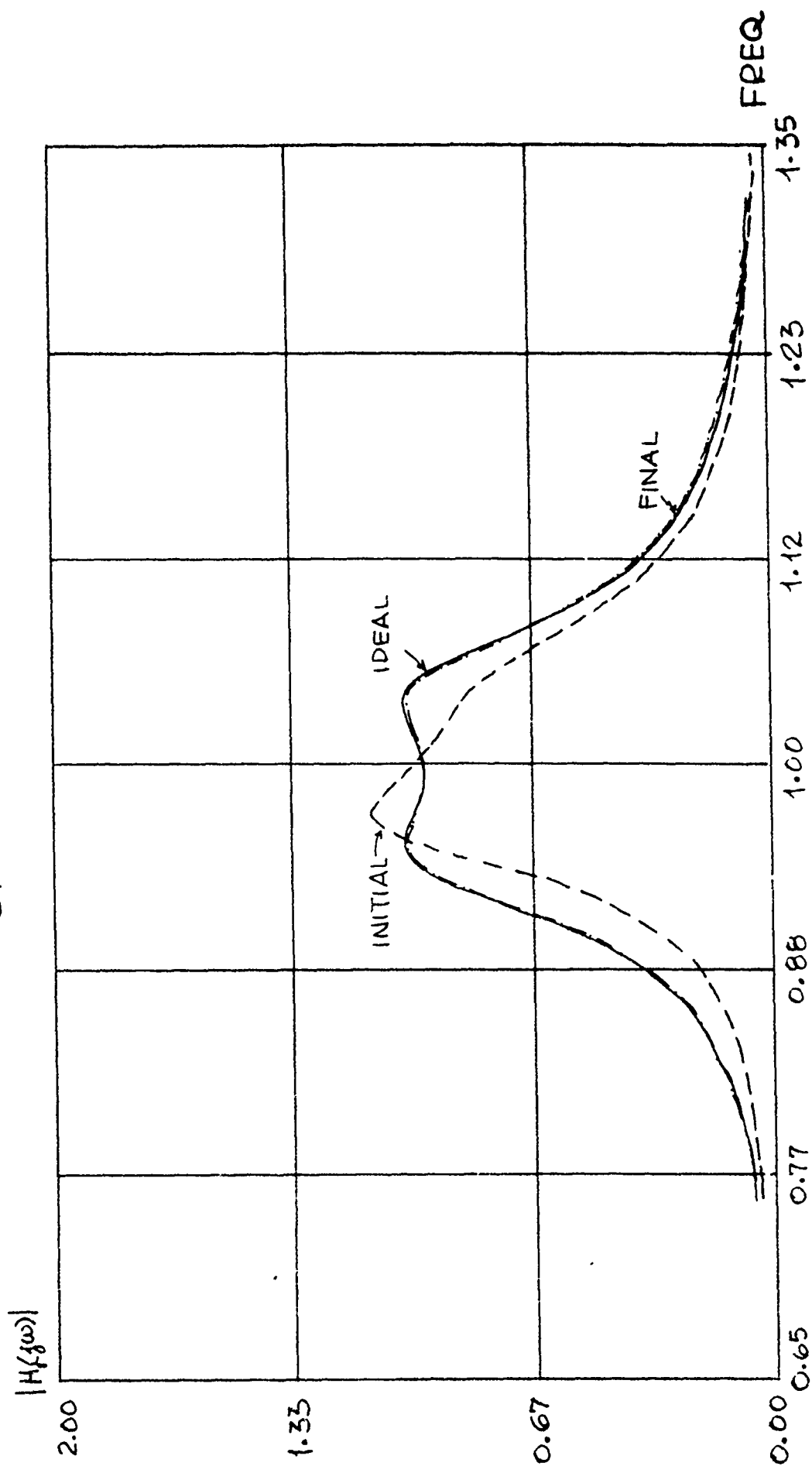


Fig. 2.3.4-3 Chebyshev BP Filter

2.4 DCASP TUNING HOST

The purpose of the tuning host is to provide an environment for the development and testing of tuning algorithms as well as hardware confirmation of the CSP and performance detector. In previous sections, we have investigated the basic architecture and control algorithms of a digital controller/performance detector/CSP scheme. The tuning host plays the role of a preliminary version of the digital controller which will be used during the development stage.

The characterization of the CSP and performance detector will be handled sequentially. Initially, the tuning host will be configured to test the CSP. In this characterization, both the exciter and the performance detector will be standard external test equipment. The tuning host is a PC-based measurement and control system which interfaces several pieces of test equipment.

2.4-1 Hardware and Software

A block diagram of the DCASP Tuning Host System is shown in Figure 2.4-1. This configuration includes: An HD6801 Single Chip Microcomputer, as the CSP controller; an HP Vectra Personal Computer (IBM AT compatible), as the tuning host controller; an HP3585A Spectrum Analyzer, as the Performance Detector; and an HP plotter to provide graphical output.

The HP Vectra is an 80286-based personal computer which is widely used for instrumentation purposes. As a tuning host, this system is configured as follows:

1. 20 Mb Hard disk
2. 1 Mb RAM
3. HP-IB Instrument Interface Bus
4. Interface Bus
5. Serial Communication Port
6. Parallel Port
7. 80287 Co-processor

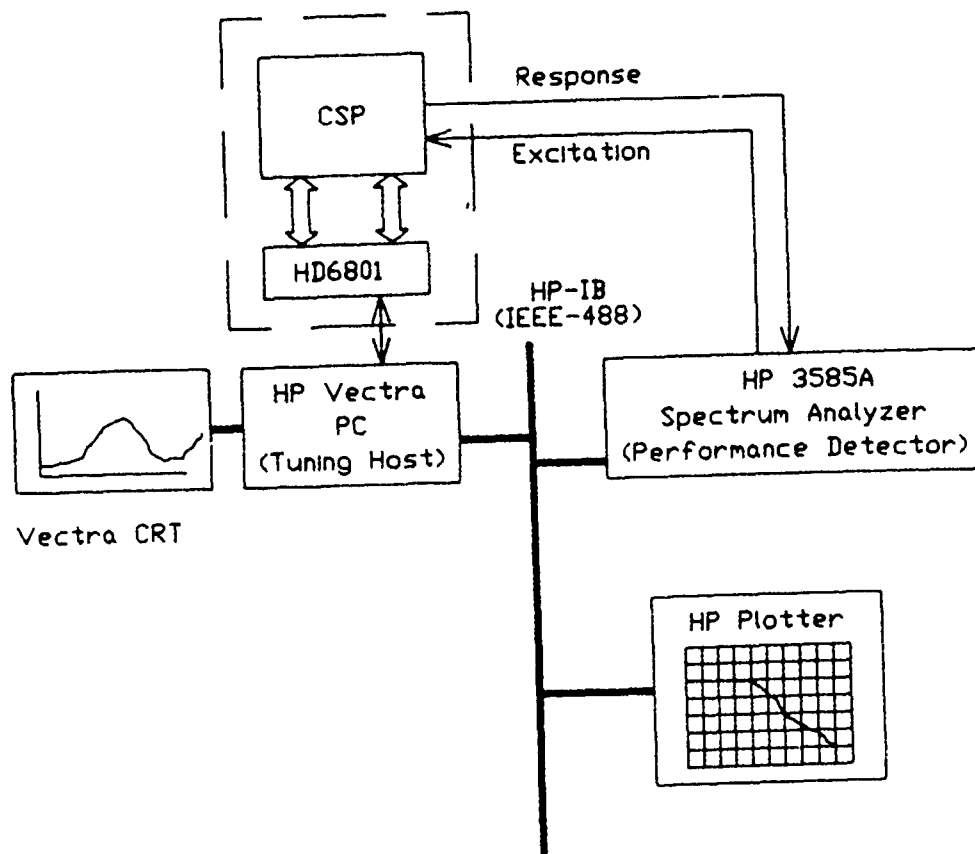


Fig. 2.4-1: Tuning Host Block Diagram

As shown in Fig. 2.4-2(a), the HD 6801 is an 8-bit single chip microcomputer unit which includes 128 bytes of RAM, Serial Communication Interface (SCI), four Parallel I/O ports, a three-function programmable timer, and 2068, 4096 or 8192 bytes of EPROM on a single package. The HD 6801 is used to provide mechanisms for controlling the CSP. A schematic diagram of CSP Controller circuit is shown in Figure 2.4-3, where Port 3 (P3) and Port 4 (P4) of the HD6801 computer are used to address controlling data to program the CSP chip. There is a row of seven switches on board, 3 of which determine the operating mode of the HD6801 and the remainder of which determine which program is to be run. The on-chip Serial Communication Interface (SCI) is also used to provide linkings between the CSP and the host computer. The SCI includes four addressable registers as depicted in Figure 2.4-2(b). It is controlled by the Rate and Mode Control Register (RMCR) and the Transmit/Receive Control and Status Register (TRCSR). Data is transmitted and received utilizing a write-only Transmitted Data Register (TDR) and a read-only Transmitted Data Register (TDR) and a read-only Received Data Register (RDR). The shift registers are not accessible to software. In addition, a 4.9152 MHz clock is used to provide the right baud rate for communication. The HP 3585A Spectrum Analyzer (see Fig. 2.4-4) covers the 10Hz to 40.1 MHz frequency range. It can be used as a stand-alone bench instrument, or, through its IEEE-488 interface, it can be connected to a computer controller (the Vectra PC in this application). The 3585A provides a graphic display of the spectral components of the input signal. Its tracking generator can be used as a drive signal for the test circuit. In addition, the parameters are entered by keyboard instead of more conventional knobs. The keyboard controls are completely programmable through its IEEE-488 interface.

2.4.1.1 Software Environment:

Various software has been developed on both the Host computer and the CSP controller to provide some basic functions to support tuning development. They are classified into the following groups in accordance with their usages:

1. Data link Modules:

This library is written for asynchronous serial communication between the HD6801 and the Vectra host. The data link protocol adopted here is a subset of the Semi Equipment Communication Standard 1 (SECS-1) data link protocol. This standard defines point-to-point communication of messages utilizing RS-232-C and voltage levels. The operation of the protocol is best understood by following the flow diagram in Figure 2.4-5 assuming that the same protocol is implemented on both Vectra and HD6801 sides. There are five major functions (subroutines) which have been written. On the Vectra side, the C language is used; while on the CSP side, 6801 Assembly language is used:

(i) Initialization (Subroutine "Comm-init()" on Vectra, "INITSCP" on HD6801)

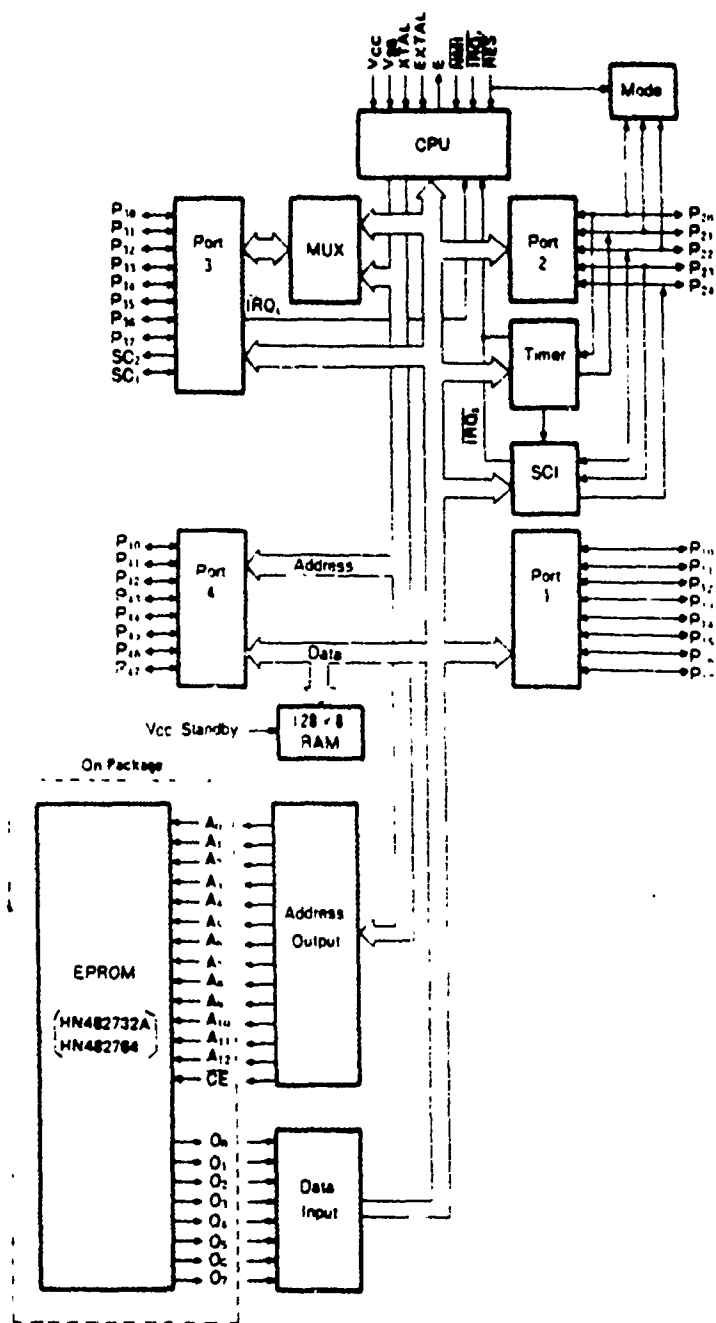


Fig. 2.4-2a: Block Diagram of HD 6801 Microcomputer.

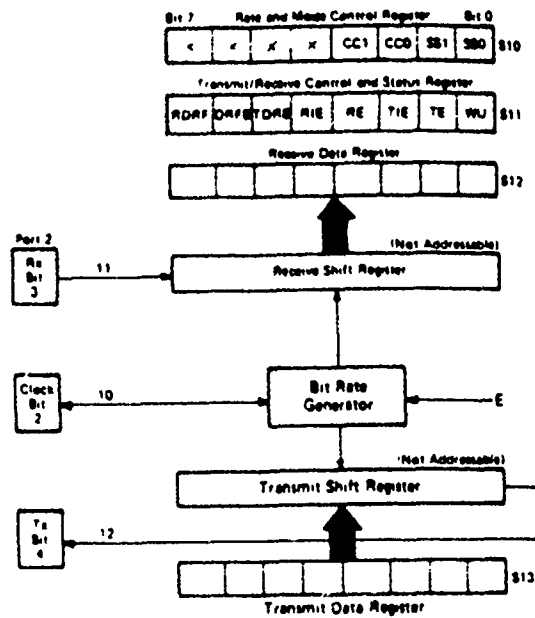


Fig. 2.4-2b: SCI Registers in HD 6801.

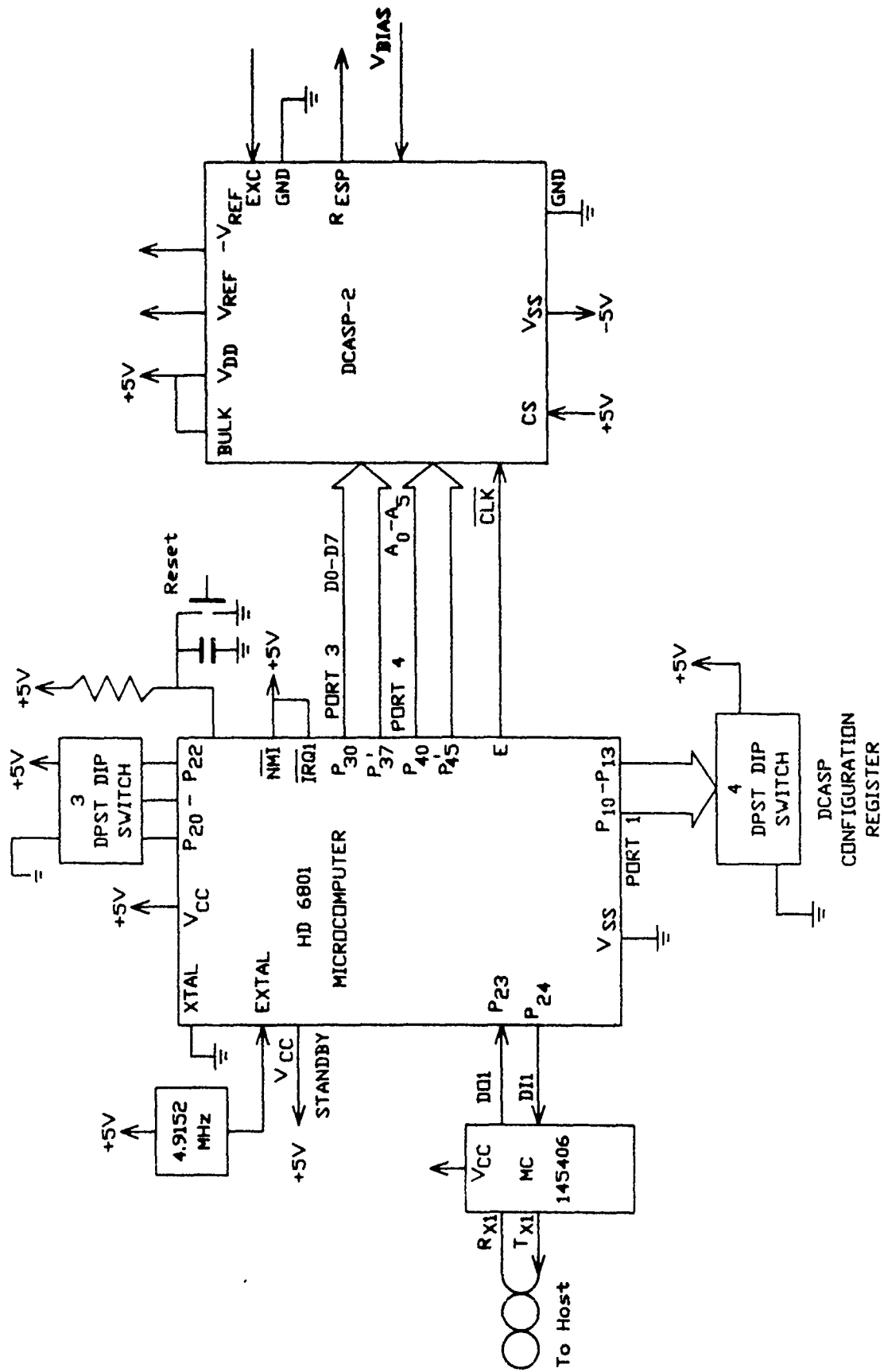


Fig. 2.4-3: Digital Controller Board

Both the communication port on Vectra and the SCI on HD6801 should be initialized to the same parameters such that they can communicate each other. These parameters are:

Baud Rate = 9600 bps

Parity Checking = None

Stop bits = 1

Data bits = 8

On the Vectra side, the initialization of the serial asynchronous communication port can be done by using the internal interrupt (Interrupt vector = 14H) supported by the Basic Input and Output System (BIOS) on the PC. The 9interrupt uses three parameters and passes them by registers AH, AL, and DX, where DX contains the current serial port address and AH contains the operation code. When the initialization is desired, AH is set to zero and AL is loaded with the parameters. After initializing, the completion status of the serial port will be returned in registers AH and AL.

On the HD6801 side the "INITSCI" routine initializes the SCI port (See Fig. 2.4-2(b)) by sending parameters to the RMCR (Rate and Mode Control Register) and enabling the TRCSR (Transmit/Receive Control and Status Register) with Transmit/Receive modes. A status code can also be read after completion of initialization.

- (ii) Send-single-character ("send (c)" on Vectra, "SEND" on HD6801) This function transmits a single character to the serial output line. On the Vectra side, the interrupt 14H is used by setting DX = 0; AH = 1 (indicates transmitting); and the AL register is loaded with the character to be transmitted. On the HD6801 side, the character is sent to the TDR (Transmitted Data Register) on the SCI port.
- (iii) Listen-single-character ("listen (c)" on Vectra, "RCVA" on HD6801) This function receives a single character from the serial input line. On the Vectra side, the interrupt 14H is used by setting DX = 0; AH = 2 (which means receiving). On the HD6801 side, the character is read from the RDR (Received Data Register) on the SCI port.
- (iv) Transmitting ("link-transmit (N, buffer)" on Vectra, "TRLINK" on HD6801) The routines allow transmitting a block of characters with length N using the data link protocol as shown in Figure 2.4-5. The data link is initiated by sending an ENQ to request the other end to receive. The sender waits for the EOT character which should be replied by the receiver. Once a send or receive state has been properly established, both ends of the data link are prepared for communication. The first character sent is a length byte (N), then the following N bytes are sent. A 16-bit checksum calculated by summing these N bytes is then transmitted. A correctly received message should cause the receiver respond an ACK character, otherwise, an NAK character will be returned.

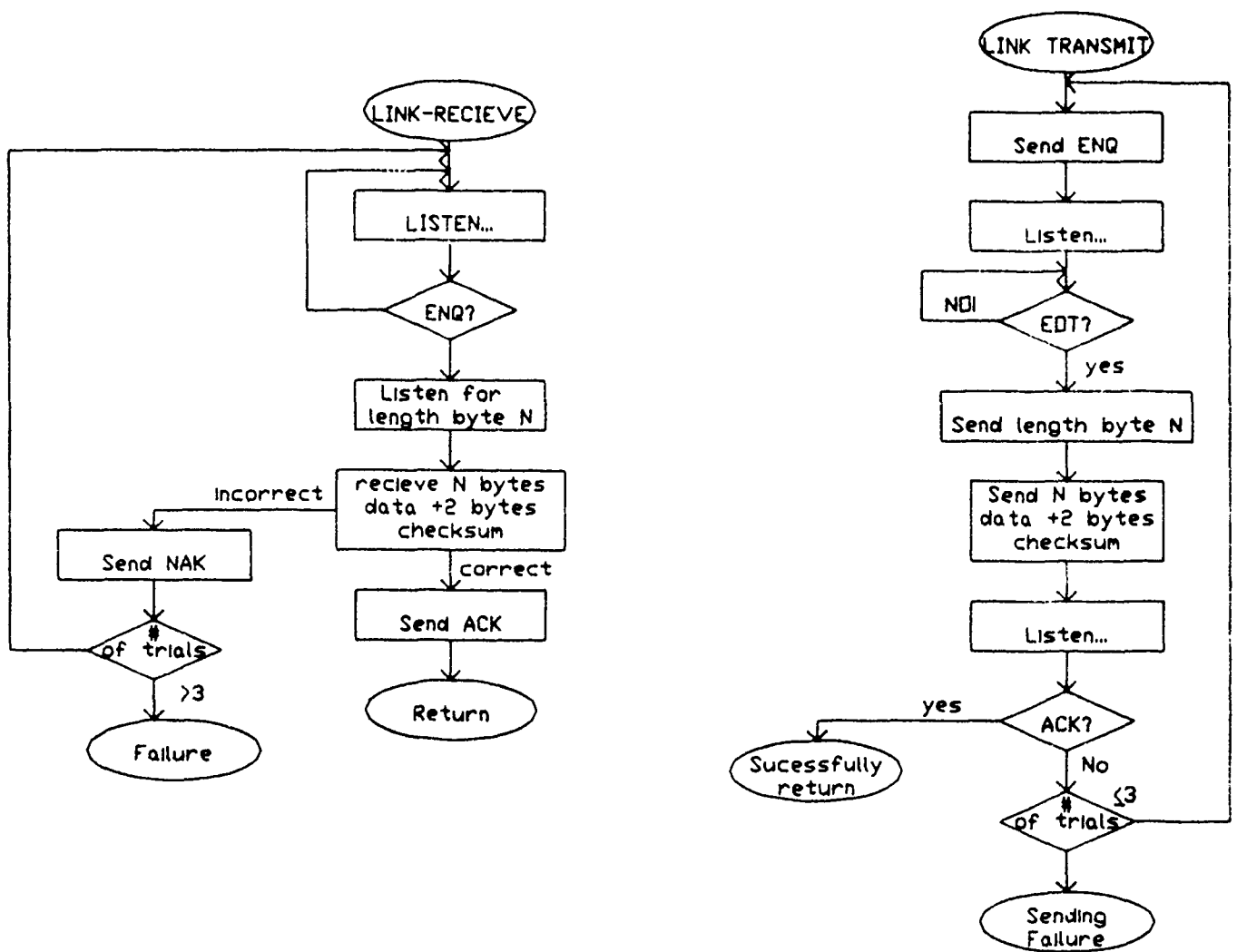


Fig. 2.4-5: Flowcharts for Data Link Protocol.

- (v) Receiving ("link-receive (N, buffer)" on Vectra, "RCVLINK" on HD6801): This procedure receives a block of characters and stores them in the "buffer" area. After receiving an ENQ character, the receiver replies an "EOT" character to indicate readiness for the length byte(N) and data from the sender. After the last character is received, the receiver compares the two check bytes against its own computation of the checksum. An improper checksum will let the receiver send a NAK(Not Acknowledged) to the sender. If the message is received correctly, the receiver will return an ACK to the sender.

2. Spectrum Measurement Modules:

These procedures (subroutines) are written in the C language to access the HP3585A remotely through the IEEE-488 (or HP-IB) bus by calling the "HP-IB Command Library" which is supported by Hewlett Packard. The Spectrum Measurement Modules are developed to collect reliable data measured from the HP3585A, which is used to provide accurate performance information for Tuning test. A brief description of these modules is given below:

(i) Spectrum Reading routine:

Calling Sequence:

Samples (amplitude, frequency, a-or-b, no-of-samples, linear, ref-level, db-dir, start-f, stop-f)

The input parameters are defined as follows:

amplitude:	the starting address of amplitude data array
frequency:	the starting address of frequency data array
a-or-b:	a flag indicating which trace (A or B) to be read on the HP3585A

no-of-samples:	an integer specifying how many data pairs(amplitude and frequency) to be sampled.
linear:	a flag which determines the data pairs are sampled in either a logarithmic or a linear scale with respect to the frequency axis.
ref-level:	reference level on the HP3585A
db-div:	dB per division on the HP3585A
start-f:	start frequency on the HP3585A
stop-f:	stop frequency on the HP3585A

This subroutine reads "no-of-samples" pairs of amplitude and frequency data from the HP3585A spectrum analyzer, where "no-of-samples" ranges from 1 to 1001. These data pairs are returned in the "frequency" and "amplitude" arrays to the calling program.

(ii) Spectrum Concatenate Routine:

Calling Sequence:

Concat (amplitude, frequency, a-or-b, samples-per-decade, ref-level,db-div, start-f, stop-f)

Most parameter definitions are the same as previous "samples" procedure except the "samples-per-decade." When calling "samples" routine by setting "linear" flag to zero, we can sample the displaying trace on the HP3585A logarithmically. However, if the spectrum spans several decades in frequency, the quantizing errors may be considerably large since the HP3585A is not log scaled in frequency axis. Therefore, the "concat" routine will sample all decades in the frequency span and then "concatenate" these decades together. The parameter "samples-per-decade" specifies the number of data pairs to be sampled for each decade. The number of decades of frequency span is determined by computing the log difference between the start frequency and the stop frequency. Then, for each decade, the routine will automatically set up the spectrum analyzer and prompt the operator pressing any key to read the data pairs if a trustful data on the HP3585A is available. Therefore, "concat" is also a routine which needs interactive responses.

(iii) Spectrum Saving Routine

Calling Sequence:

Savetrace (tracename, amplitude, frequency, length)

The parameter "tracename" is an 8-character string specifying the saving file name. The "length" is an integer specifying the size of data arrays. This routine will save the data arrays "amplitude" and "frequency" to a specified disk file with compact binary form.

(iv) Spectrum Loading Routine

Calling Sequence:

load trace(tracename, amplitude, frequency, length)

The "loadtrace" routine loads the data arrays from the specified disk file and return the arrays to the calling program.

(v) Spectrum Initialization Routine:

Calling Sequence:

Spec-init()

The "Spec-init()" is a subroutine which initializes the IEEE-488 bus and enables the HP3585A for remote mode.

(vi) Getting Parameters Routine

Calling Sequence:

get-parm(ref-level, db-div, start-f, stop-f)

All the parameters have been described in spectrum sampling routine "Samples." These parameters are of great importance for Spectrum Measurement Modules and Graphical Output Modules since they uniquely determine the ranges of amplitude and frequency axes. The "get-parm" routine reads these four parameters from the 3585A and return them to the calling program.

3. Graphic output Modules:

Two different output devices are of interest for graphical output; an HP Plotter and the CRT Screen. These procedures provide graphical output for analysis and evaluation of tuning algorithms. The HP Plotter can be any model of plotter which accept HPGL (HP

Graphic Language) instructions. The plotting algorithms developed for both devices are essentially the same except for some primitive functions such as line-drawing and labeling. The plotting routines are written in three languages: FORTRAN, C, and 8086 Assembly. This multi-language feature provides a more flexible programming environment which is adaptable to various programming languages.

(i) Dot Plotting Routine

Calling Sequence:

pixel (x,y,on-off)

This primitive graphic routine is coded in Assembly language. The routine turns the specified pixel position (x,y) on or off, depending on the value of on-off flag. This routine is used by the line-drawing routine to generate a straight line on the CRT screen.

(ii) Screen Mode Routine

Calling Sequence:

screen (mode)

This routine initializes the CRT screen mode as the following:

Mode	Description
0	80 × 25 TEXT MODE
1	200 × 320 Color/Graphics, 40 × 25 TEXT MODE
2	200 × 640 HR GRAPHICS, 80 × 25 TEXT MODE

Where mode 2 is set before performing any other plotting functions. This routine is also written in Assembly.

(iii) Cursor Positioning Routine

Calling Sequence:

Set-Cursor (row, column)

This procedure sets the cursor position to the specified (row, column) position on the CRT screen. The "Set-Cursor" is called by the GGLABL routine used for CRT labeling.

(iv) Line Drawing Routines

Calling Sequence:

GGVEC(x1,y1,x2,y2)— for CRT Screen

HPVEC(x1,y1,x2,y2)—for HP Plotter

The "HPVEC" routine is simply one single line of HPGL (HP Graphics Language) instructions which point from (x1, y1) to (x2, y2). The "GGVEC," however, is using more complicated algorithm to draw a line between two points since the CRT screen is a raster-scanning graphic device. The GGVEC and HPVEC routines have been called extensively by the Grid-Plotting and Trace-Plotting routines.

(v) Labeling Routines:

Calling Sequence:

HPLABL(P-string, x, y, direction)—for HP Plotter

GGLABL(P-string, x, y, direction)—for CRT Screen

The "HPLABL" labels a character string (addressed by "P-String") starting from the point (x, y) in the direction of "direction" on an HP Plotter. The direction may be either left to right (default), right to left, bottom to up, or up to bottom. The "GGLABL" does exactly the same thing except that the output device is the CRT screen. These routines are called by the Grid-Plotting routines to label the axis, scales, titles, etc.

(vi) Grid-Plotting Routines:

Calling sequence:

CALL GGGRID(X1,Y1,X2,Y2,XMIN,YMIN,XMAX,YMAX,NGX,NGY,
1NSX,NSY,LOGX,LOGY)—for CRT Screen

CALL HPGRID(X1,Y1,X2,Y2,XMIN,YMIN,XMAX,YMAX,NGX,NGY,
1NSX,NSY,LOGX,LOGY)—for HP Plotter

GGGRID draws a plotting grid on the page along with scale values for both X and Y axes, where the 'X' axis is the horizontal axis, and the 'Y' axis is the vertical axis. The function of HPGRID is to plot the grid on those plotters accepting HPGL commands. The calling sequence and input parameters are exactly the same as the GGGRID routine. Both HPGRID and GGGRID routines were written in FORTRAN.

Input parameters:

X1	is the X page address of left hand bottom corner of the grid (between 0 and 199) (Integer)
Y1	is the Y page address of left hand bottom corner of the grid (between 0 and 639) (Integer)
X2	is the X page address of the upper right hand corner of the grid (between 0 and 199) (Integer)
Y2	is the Y page address of the upper right hand corner of the grid (between 0 and 639) (Integer)
XMIN	is the minimum value of X (Real)
YMIN	is the minimum value of Y (Real)
XMAX	is the maximum value of X (Real)

YMAX	is the maximum value of Y (Real)
NGX	is the number of X grid lines (see linear grids or log grids for a discussion of how NGX is used). (Integer)
NGY	is the number of Y grid lines (see linear grids or log grids for a discussion of how NGY is used). (Integer)
NSX	is the number of X scaling (tic mark) values (see linear grids or log grids for a discussion of how NSX is used). (Integer)
NSY	is the number of Y scaling (tic mark) values (see linear grids or log grids for a discussion of how NSY is used). (Integer)
LOGX	= 0 if X is to be plotted on a linear scale otherwise X is to be plotted on a log scale. (See log grids for a discussion of how LOGX is used.) (Integer)
LOGY	= 0 if Y is to be plotted on a linear scale otherwise Y is to be plotted on a log scale. (See log grids for a discussion of how LOGY is used.) (Integer)
	NGX, NGY, NSX, NSY, LOGX, and LOGY usage for linear and log grids

The following paragraphs discuss the usage of the number of grid lines, number of scaling values, and linear-log parameters for linear and log axis. Substitute "X" or "Y" for "?" wherever "?" appears; for example LOG? stands for LOGX or LOGY. The direction, left-right-up-down, used in the case of the X axis is always given first; for example, left (bottom) means left in the case of the X axis or bottom in the case of the Y axis.

Linear Grids (LOG?=0)

NG?	The axis is divided into NG? minus one equal sized sections and NG? lines are drawn bounding those sections.
NG?	equal to one draws only the axis, left (bottom); NG? equal to two draws the axis and margin, right (top); NG? equal to three draws a the axis, the margin, and a line a the center; etc.
NS?	The axis is divided into NS? minus one equal sized sections and NS? tic marks with scale values are drawn marking the boundries of those sections. If NS? is less than one, no tic marks are drawn. When tic marks with scale values are drawn on the outside of the grid area.

Log Grids (LOG?.NE.0)

NG? ≤ 0 no decade or sub-decade lines, decade or sub-decade tic marks, or axis are drawn.
 > 0 decade and sub-decade lines and/or tic marks are controlled by LOG? value; axis is controlled by NG?.
 $= 1$ axis, left (bottom), is drawn.
 ≥ 2 axis and margin, right (top), are drawn.

LOG? < 0 draw any tic marks on the bottom (left) side of the grid only.
 > 0 draw any tic marks on the bottom (left) side of the grid and the top (right) side of the grid.
 If tic marks are drawn they are drawn inside the grid area.

IABS(LOG?)

$= 1$ don't draw any lines or tic marks.
 $= 2$ draw tic marks at decades only.
 $= 3$ draw tic marks at decades and sub-decades.
 $= 4$ draw lines at decades only.
 $= 5$ draw lines at decades and tic marks at sub-decades.
 $= 6$ draw lines at decades and sub-decades.

NS? ≤ 0 don't draw any scale tic marks or values.
 > 0 draw scale tic marks with printed powers of ten at each decade on the outside of the grid area.

(vii) Trace-plotting routines:

 Calling Sequence:

spec-plot(trace, freq, length, title,
 xp1,yp1,xp2,yp2,
 ref-level,db-div,start-f,stop-linear-x, spectrum-only)-for crt screen.
 spec-hp-plot(trace,freq, length, title,
 xp1,yp1,xp2,yp2,
 ref-level,db-div,start-f,

stop-f, linear-x, spectrum-only, pen-number)-for HP Plotter

Input parameter description:

trace[] : array containing the data to be plotted.

length : length of data in array trace[].

title : the name of the trace.

xpl, ypl : coordinate of the left lower point.

xp2, yp2 : coordinate of the right upper point.

ref-level : reference level.

db-div : db per division.

start-f : start frequency.

stop-f : stop frequency.

linear-x : a flag indicates the linear scaling is activated along x-axis. If linear-x = 0 then the x axis is log scaled. The value of linear-x also indicates the number of grids (or tic marks) to be drawn. (see the GGRID FORTRAN source for detail)

spectrum-only:

equals 0 if both gridings and spectral informations are desired

equals 1 for drawing only spectral data

pen-number: pen-number is an integer from 1 to 8 which specifies the pen of the hp plotter to be used to draw the trace.

The routines plot the measured data (in forms of Amplitude and frequency arrays) on HP plotter or CRT. Similar to Grid-plotting, many flexible features are provided, and the same algorithm is applied for both devices.

(III.) Tests of Tuning Host:

It is very important that the tuning host should be verified to function as expected. As a result, tests of the software/hardware described above are required.

For the Data Link Modules, Transmitting and Receiving tests have been conducted between two identical Vectra PC's. The results showed that up to 255 bytes of data can be successfully transmitted and received in one block using the SECS-1 protocol. In fact, the protocol we used here is only a subset of SECS-1 in the way that it doesn't support "timeout" checking. The data link between the Vectra PC and DCASP Controller (HD6801), has not yet been verified. The maximum "block size" for the Vectra- HD6801 link can be no more than 128 bytes since the HD6801 supports limited on-chip Read-Write Memory.

In order to test the spectrum measuring as well as Graphic Output procedures, a C program named "SPEC" has been written. This menu-driven program provides typical functions such as reading a trace, loading the trace, saving the trace, and plotting the trace on either CRT or Plotter. The reading routine, which actually just calls the "concatenate" procedure mentioned previously, shows a really nice feature that significantly increases the resolution and improves the quantization error due to logarithmic sampling. [Figure 2.4-6]

More tests have been planned to be conducted and more options may be added to the program "SPEC" to test both spectrum and graphic routine. The data link procedures on the HD6801 side can be verified by sending some CSP control parameters from the Vectra PC. After the tuning algorithms are well developed, an "automatic" tuning host can be implemented by using these modules.

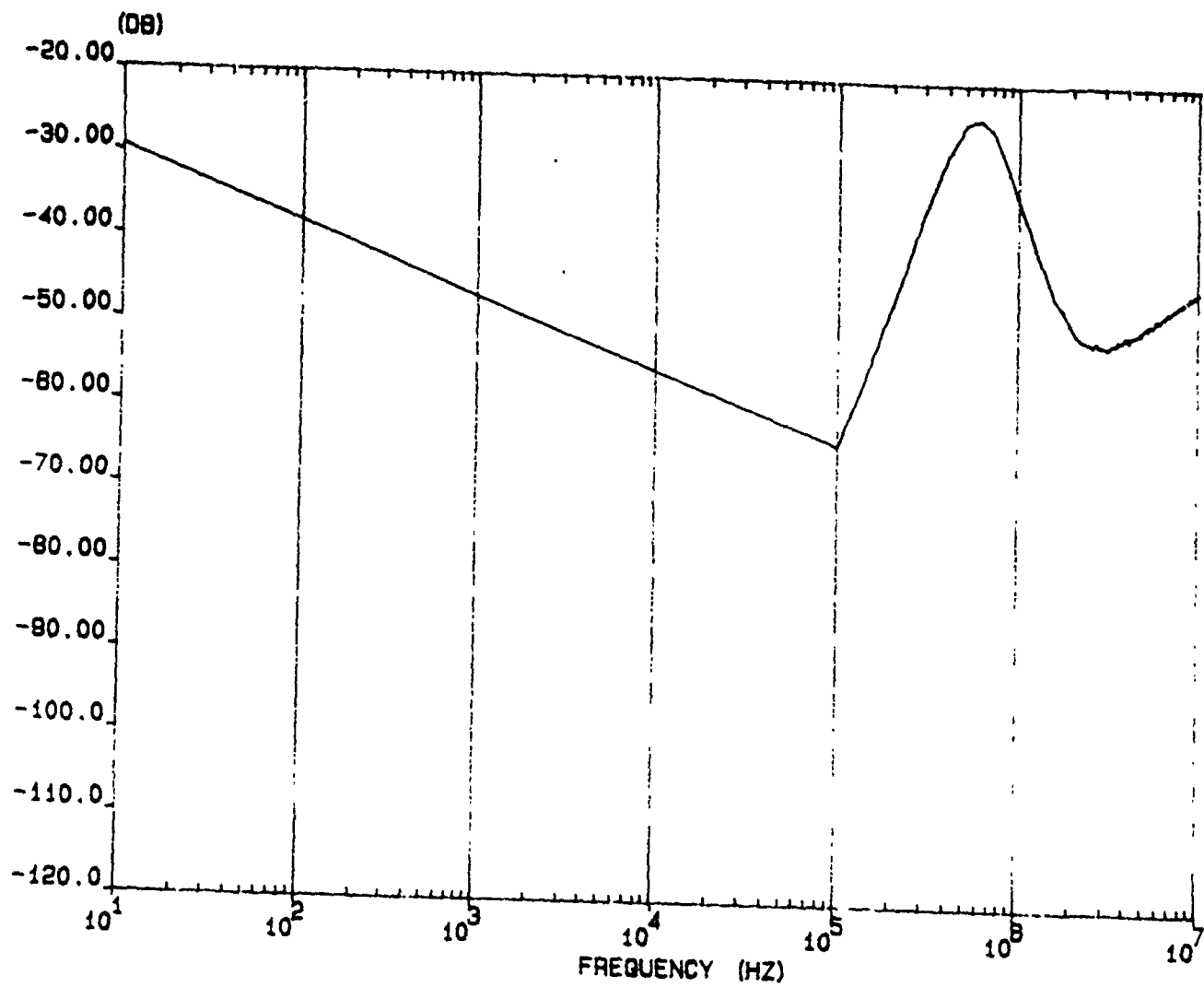


Fig. 2.4-6a: Log Sampling without "Concatenation".

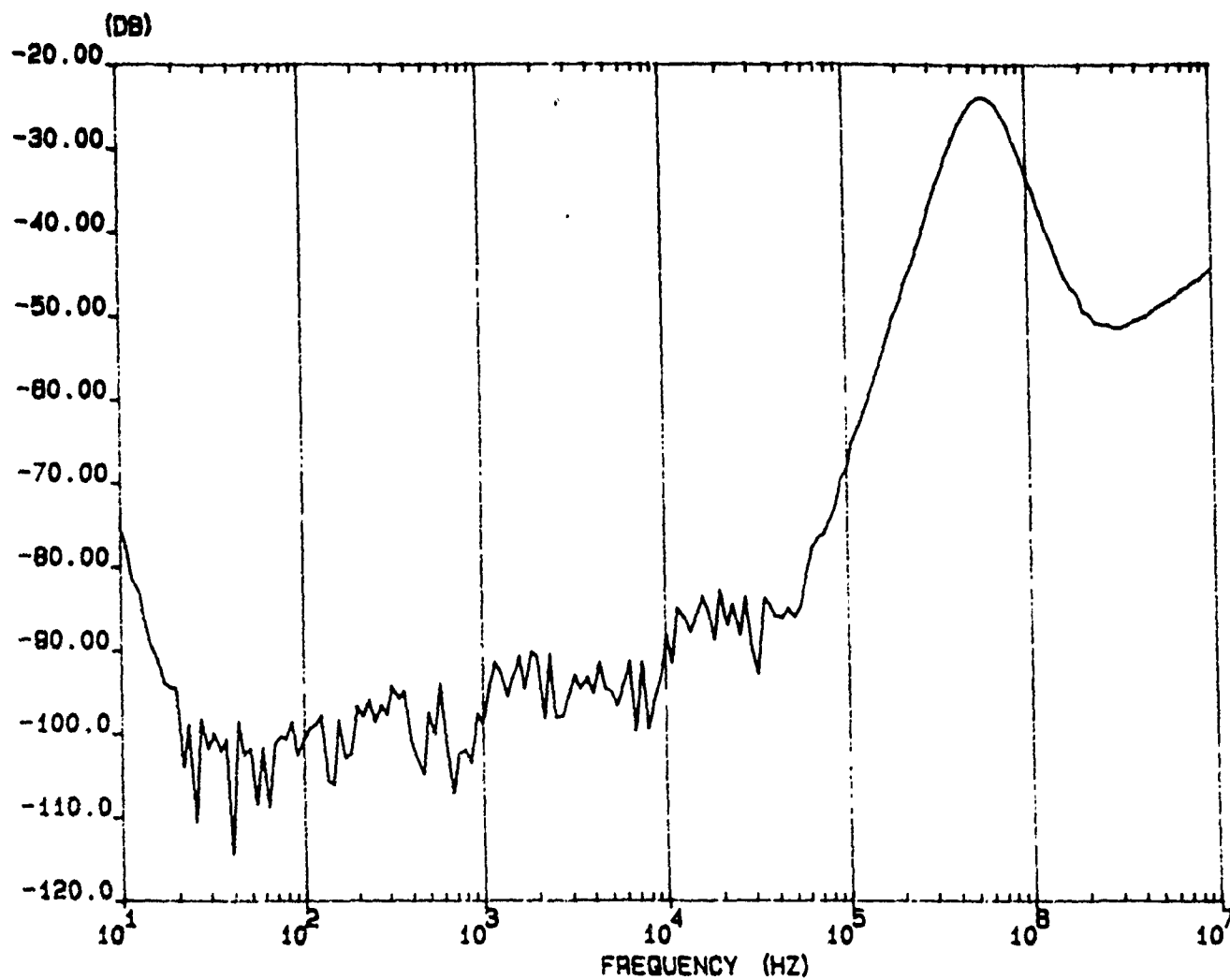


Fig. 2.4-6b: Log Sampling with "Concatenation".

2.5 CSP Control and Memory Map

The Controlled Signal Processor (CSP) in DCASP-2 is totally programmable and reconfigurable. A 21 bit system bus is used for configuring the CSP. This system bus is decomposed into a 12 bit predecode address bus ($A_0 - A_{11}$), an 8 bit data bus (D_0, \dots, D_7) and a 1 bit clock line. The CSP is comprised of 3 biquads, any or all of which can be used simultaneously in the creation of system transfer functions of up to 6th order.

A block diagram of the DCASP-2 architecture which includes the CSP and the performance detector and which shows the address and data bus structure is shown in Fig. 2.5-1. A description of the major blocks in this diagram follows.

1. Level Shifters. The external digital signals are assumed to have standard TTL logic levels of 0-5 volts. The internal digital circuits use CMOS logic levels of ± 5 volts. The level shifters are simply a pair of CMOS inverters sized to provide the logic level shift and necessary drive for the internal busses. The level shifter also provides complementary outputs, as required by the Address Predecode circuitry.
2. Address Predecode. The decoding of a 6 bit address on the address bus at each addressable element is very awkward. CMOS NAND gates with more than 4 inputs which could conceptually be used for this purpose are generally deemed impractical. The 6 bit address bus ($A_0 - A_5$) is predecoded into a 12 bit predecoded address bus ($P_0 - P_{11}$). It can be shown that this allows use of a 3 input NAND gate for final address decoding at each addressable element.
3. System Bus. The 21 line system bus is composed of the 8 data lines ($D_0 - D_7$), the 12 predecoded address lines ($P_0 - P_{11}$), and the system clock. The system bus handles all of the digital system control except for that of the Performance Detector which has several of its own control lines.
4. Analog Bus. The analog bus is composed of the analog reference voltages and analog input/output signals for both individual filter biquads and the overall chip. Portions of the analog bus are purely internal to the CSP and others are also external. The analog voltage references consist of V_{rf+} and V_{rf-} (which controls the range and resolution of attainable pole frequencies via the fine adjust of $gm_{1,2,3}$), V_{rq+} and V_{rq-} (which controls the range and resolution of attainable pole Q's via the fine adjustment of $gm_{4,5}$).
5. CSP (Controlled Signal Processor). The CSP is a digitally controlled analog signal processing block. The implemented CSP contains transconductance amplifiers with voltage controlled transconductances and a digitally controlled capacitor array. The topology of the CSP can also be modified by use of digitally controlled switches.
6. Latch. The latch shown is a 2 bit ADL (Address Decoder and Latch) as described

in Fig. 2.5-2. This ADL (hereafter termed "latch") controls the state of the Input Switch (S_1) and Response Switch (S_2). Similar latches will be employed at every addressable element internal to the CSP to perform the final address decode from the predecoded address bus and to store the required data bits from the data bus.

7. Performance Detector. The measurement system is based upon simultaneous voltage sampling of the input excitation and the output response of the CSP at multiple random time instances with a constant input frequency and amplitude. The resulting samples are converted by an external A/D to binary data for an external microprocessor to compute the gain and phase shift of the system. This combined with a digitally interfaced external frequency counter provides an automated means of characterizing the analog signal path.

The CSP itself is further decomposed in the block diagram of Fig. 2.1-1 which is repeated in Fig. 2.5-3. Each of the biquads which comprise the CSP are as shown in Fig. 2.1-2 which is repeated in Fig. 2.5-4. The OTA's and capacitor arrays of the biquads are shown in block diagram form in Figures 2.5-5 and 2.5-6.

A discussion of the memory map structure follows.

First the method of controlling each of the basic building block will be discussed. This will be followed by a discussion of the memory map for the system.

Consider initially the OTA depicted in Fig. 2.5-5. There are two 6-bit busses used to control the OTA. One is a coarse control and the other a fine control. These were discussed in Sec. 2.1 of this report. The data bus mapping for the coarse control is shown in Table 2.5-1 where the gain factor represents the current mirror gain discussed in Sec. 2.1. The fine control based upon using the logarithmic DAC of Sec. 2.1 controls the transconductance gain as described by the equation

$$g_m = A_m(mV_i + b) \quad (2.5 - 1)$$

where A_m is the mirror gain as given in Table 2.5-1, m and b are constants ($m = 61.8\mu S/V$ and $b = 257.9\mu S$) and V_i is the "tail" voltage which appears at the output of the D/A and is given by

$$V_i \cong V_{ref}^- + (V_{ref}^+ - V_{ref}^-) \frac{(1 - C^i)}{1 - C^{63}} \quad (2.5 - 2)$$

where $i = \sum_{i=0}^7 D_i 2^i$, $C = .01$ and D_i is the i^{th} bit on the data bus.

From Table 2.1-7 of Sec. 2.1, the data bus mapping to capacitor array values is as given in Table 2.5-2.

Data bus bits D_3 , D_4 and D_5 of the Biquad Latch of Fig. 2.5-4 set the biquad configuration and D_0 , D_1 and D_2 interconnect these biquads into the CSP structure. The

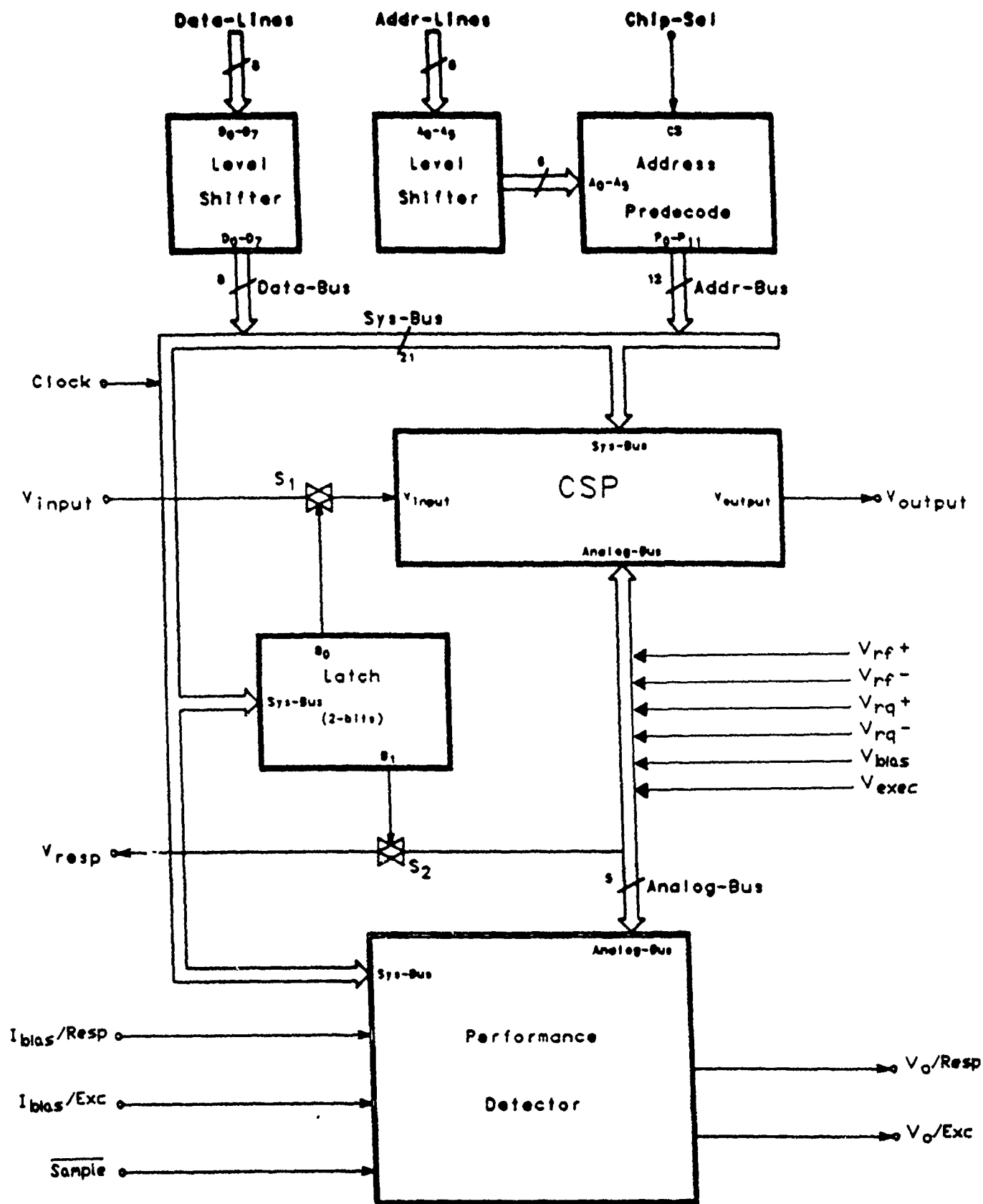
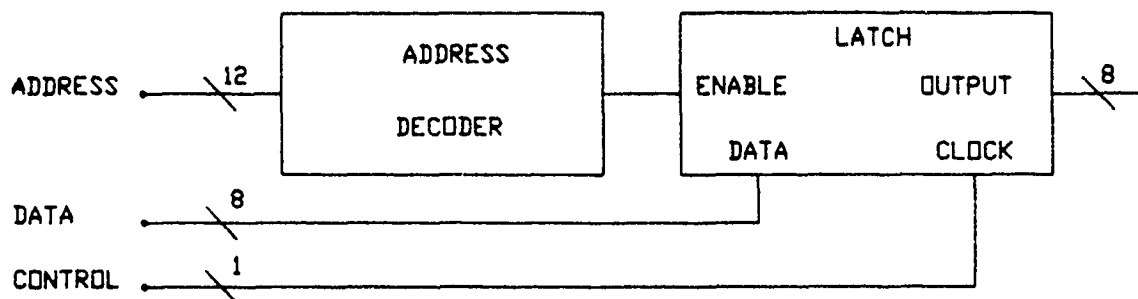
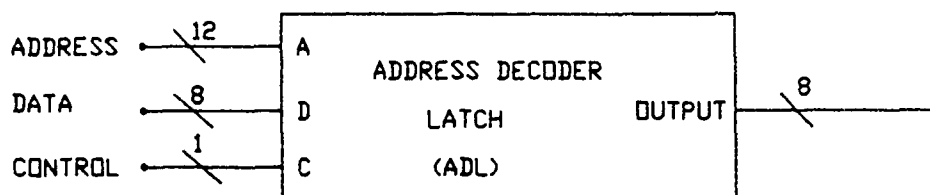


Fig. 2.5-1: Block Diagram of Initial DCASP Structure



(a)



(b)

Fig. 2.5-2 Address Decoder/Latch(ADL)
a) Block Diagram, b) Simplified Diagram

memory map for the setting of each of the biquadratic functions appears in Table 2.5-3. The memory map for the interconnection scheme for each biquad into the CSP structure appears in Table 2.5-4.

Finally, the memory map for the addressing scheme is shown in Table 2.5-5. Both the actual address and the predecode address which is used on the internal data bus is shown. Note that both the interconnection configuration and biquad function type are set with the biquad configuration latch. Separate addresses are also provided for the coarse and fine control of each biquad.

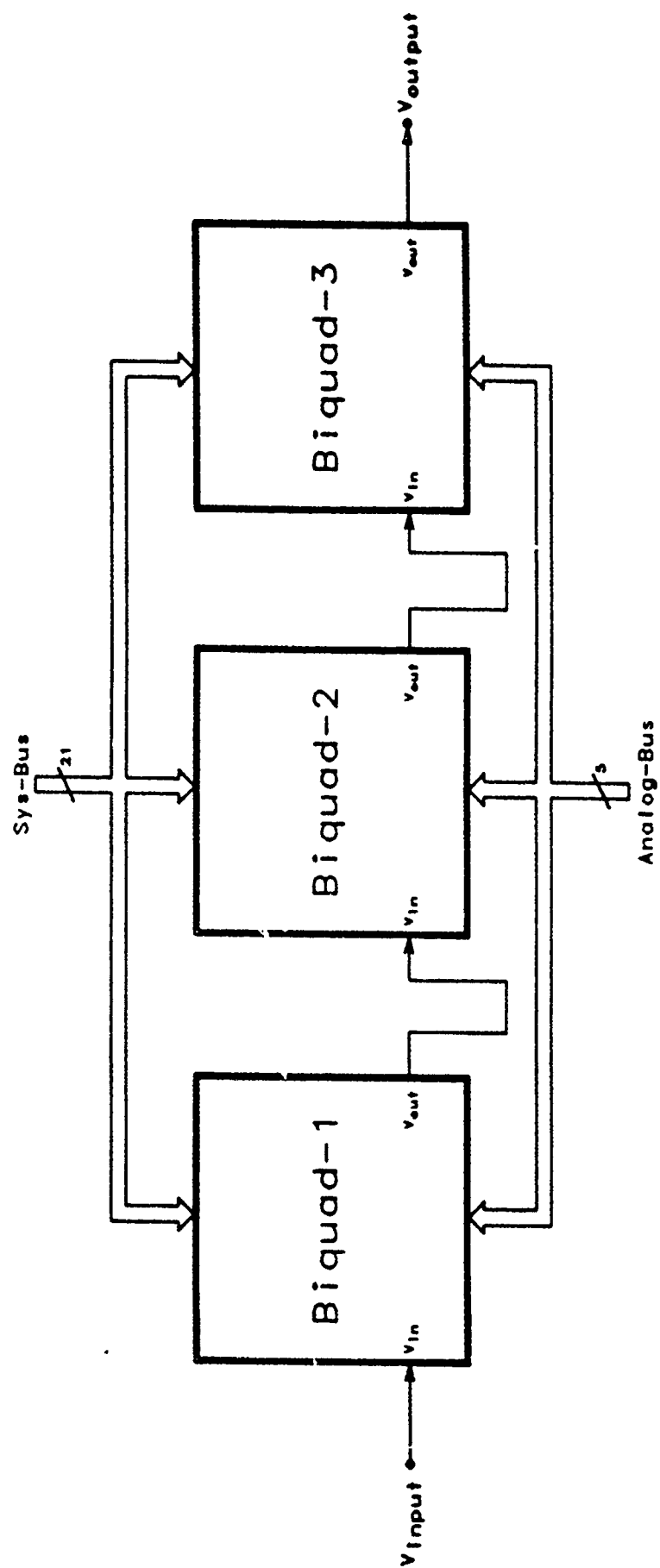


Fig. 2.5-3 Initial CSP Block Diagram

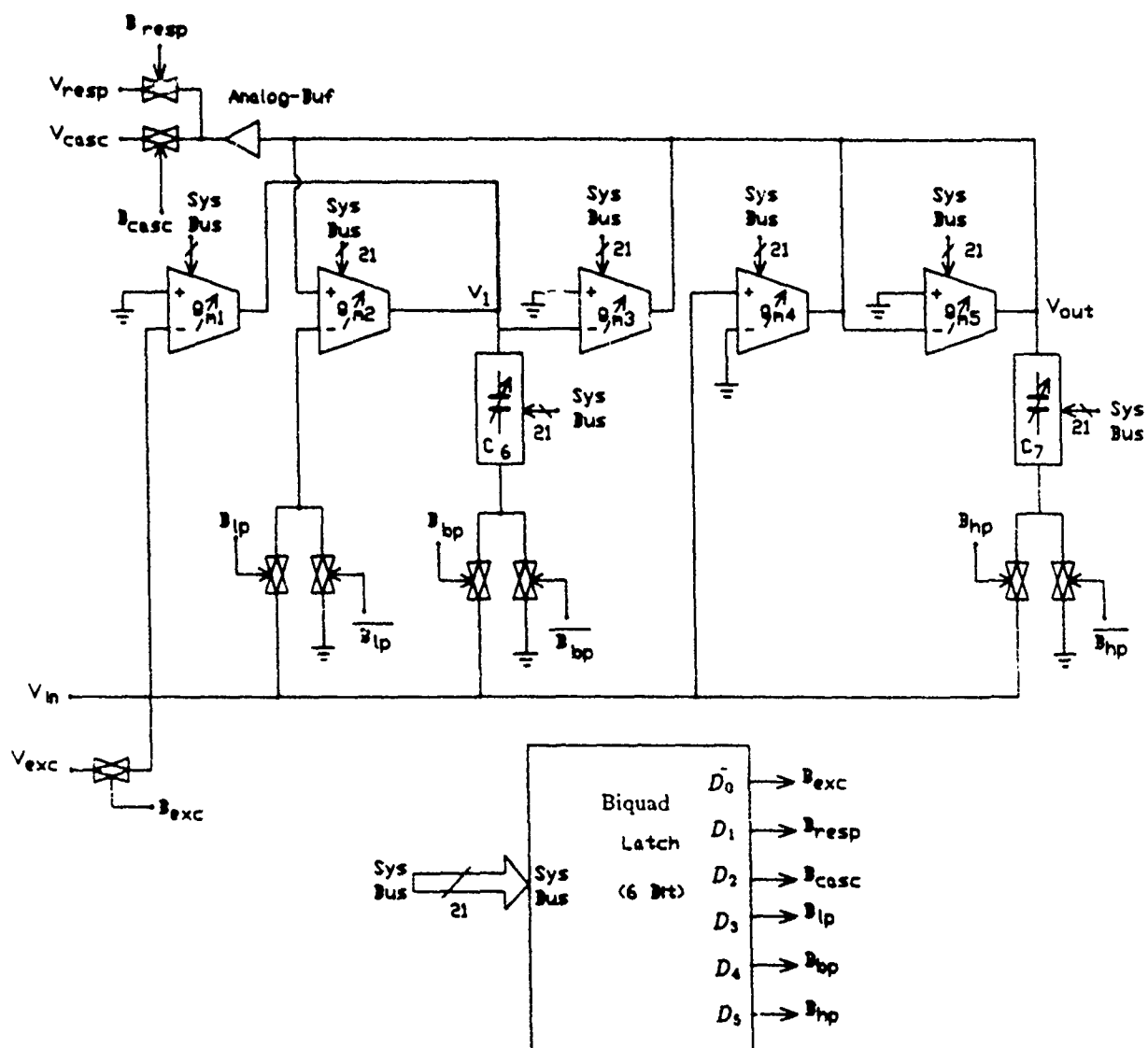


Fig. 2.5-4: Initial Biquad Block Diagram

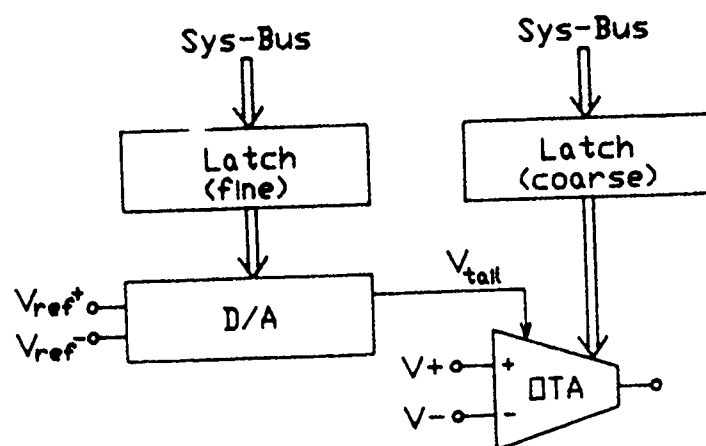


Fig. 2.5-5 CTA block diagram.

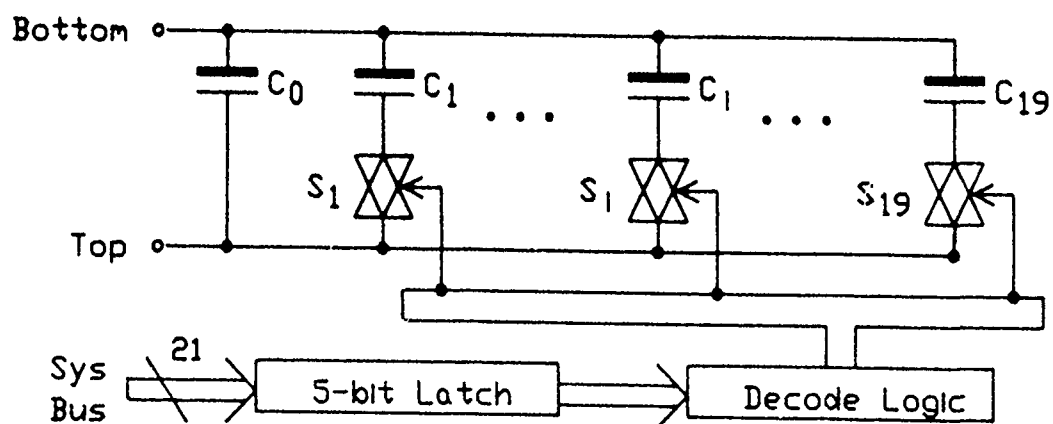


Fig. 2.5-6 Capacitor array block diagram.

D_0	D_1	D_2	D_3	D_5	N	DCASP-2 Cap. (pf)
0	0	0	0	0	0	0.48
0	0	0	0	0	1	0.26
0	1	0	0	0	2	0.30
1	1	0	0	0	3	0.35
0	0	1	0	0	4	0.40
1	0	1	0	0	5	0.46
0	1	1	0	0	6	0.52
1	1	1	0	0	7	0.60
0	0	0	1	0	8	0.68
1	0	0	1	0	9	0.78
0	1	0	1	0	10	0.88
1	1	0	1	0	11	1.00
0	0	1	1	0	12	1.14
1	0	1	1	0	13	1.30
0	1	1	1	0	14	1.47
1	1	1	1	0	15	1.67
0	0	0	0	1	16	1.89
1	0	0	0	1	17	2.15
0	1	0	0	1	18	2.43
1	1	0	0	1	19	2.75

Table 2.5-2 Memory Map for Capacitor Values

	D_5	D_4	D_3	Special Conditions
Highpass(HP)	1	0	0	$g_{m1} = g_{m4} = 0$
Bandpass (BP)	0	0 or 1	0	$g_{m1} = 0$
Lowpass(LP)	0	0	0 or 1	$g_{m4} = 0$
Allpass(AP)	1	1	1	$g_{m1} = g_{m4} = 0$ $g_{m3} = g_{m5}$
Lowpass Notch(LPN)	1	1	1	$g_{m3} = g_{m4}$ $g_{m1} > g_{m2}$
Highpass Notch (HPN)	1	1	0	$g_{m3} = g_{m4}$ $g_{m1} < g_{m2}$

Table 2.5-3 Memory Map for Function Control of Any Biquad

			Connection		
D_2	D_1	D_0	V_i	V_0	Cascade
X	X	1	Excitation Bus	Response Bus	Connect Output of Biquad to Input of Next Biquad
X	1	X			
1	X	X			

Table 2.5-4 Memory Map for CSP Interconnection of any Biquad.

LATCH	BIQUAD 1		BIQUAD 2		BIQUAD 3	
	Addr.	Precode Addr.	Addr.	Precode Addr.	Addr.	Precode Addr.
Biquad Config.	10 ₁₆	P ₀ , P ₄ , P ₉	20 ₁₆	P ₀ , P ₄ , P ₁₀	30 ₁₆	P ₀ , P ₄ , P ₁₁
g _{m1} Fine Course	12 ₁₆	P ₂ , P ₄ , P ₉	22 ₁₆	P ₂ , P ₄ , P ₁₀	32 ₁₆	P ₂ , P ₄ , P ₁₁
	13 ₁₆	P ₃ , P ₄ , P ₉	23 ₁₆	P ₃ , P ₄ , P ₁₀	33 ₁₆	P ₃ , P ₄ , P ₁₁
g _{m2} Fine Course	14 ₁₆	P ₀ , P ₅ , P ₉	24 ₁₆	P ₀ , P ₅ , P ₁₀	34 ₁₆	P ₀ , P ₅ , P ₁₁
	15 ₁₆	P ₁ , P ₆ , P ₉	25 ₁₆	P ₁ , P ₆ , P ₁₀	35 ₁₆	P ₁ , P ₆ , P ₁₁
g _{m3} Fine Course	16 ₁₆	P ₂ , P ₅ , P ₉	26 ₁₆	P ₂ , P ₅ , P ₁₀	36 ₁₆	P ₂ , P ₅ , P ₁₁
	17 ₁₆	P ₃ , P ₆ , P ₉	27 ₁₆	P ₃ , P ₆ , P ₁₀	37 ₁₆	P ₃ , P ₆ , P ₁₁
g _{m4} Fine Course	18 ₁₆	P ₀ , P ₆ , P ₉	28 ₁₆	P ₀ , P ₆ , P ₁₀	38 ₁₆	P ₀ , P ₆ , P ₁₁
	19 ₁₆	P ₁ , P ₆ , P ₉	29 ₁₆	P ₁ , P ₆ , P ₁₀	39 ₁₆	P ₁ , P ₆ , P ₁₁
g _{m6} Fine Course	1A ₁₆	P ₂ , P ₆ , P ₉	2A ₁₆	P ₂ , P ₆ , P ₁₀	3A ₁₆	P ₂ , P ₆ , P ₁₁
	1B ₁₆	P ₃ , P ₆ , P ₉	2B ₁₆	P ₃ , P ₆ , P ₁₀	3B ₁₆	P ₃ , P ₆ , P ₁₁
C ₆ C ₇	1C ₁₆	P ₀ , P ₇ , P ₉	2C ₁₆	P ₀ , P ₇ , P ₁₀	3C ₁₆	P ₀ , P ₇ , P ₁₁
	1E ₁₆	P ₂ , P ₇ , P ₉	2E ₁₆	P ₂ , P ₇ , P ₁₀	3E ₁₆	P ₂ , P ₇ , P ₁₁
Main Config. Control	01 ₁₆	P ₁ , P ₄ , P ₈				

Table 2.5-5 Memory Map for Latch Addressing

3.0 DOCUMENTATION

- Monthly progress reports (CDRL #A002) have been prepared and submitted to the project monitor which summarize the monthly activities of this task. These monthly progress reports cover each month beginning in January 1987 and ending in September 1987. Although financial support for this project did not start until early March, 1987, activity supported by alternate sources was ongoing through the months of January and February to avoid discontinuity associated with retraining new researchers to work on this project.
- A paper entitled "A Reconfigurable Biquadratic Building Block for Digitally Controlled Continuous-Time Signal Processing", by R. L. Geiger, E. Sánchez-Sinencio, D. Hiser, K. Peterson and A. Nedungadi which focuses on the original design of the CSP has been accepted for presentation at GOMAC-87.
- A paper entitled "Performance Characteristics of a CMOS Transconductance Element Using a Square-Law Compensated Differential Pair" by Ashok Nedungadi and Randall Geiger has been written. This paper focuses on OTA design and will be submitted for peer review in the near future.
- A paper entitled "Generation of Continuous-Time Two Integrator Loop OTA Filter Structures", by E. Sánchez-Sinencio, R. Geiger and Horacio Nevarez was presented at the IEEE International Symposium on Circuits and Systems, Philadelphia, May 1987.
- A paper entitled "Amplifier Design Considerations for High Frequency Monolithic Filters" by Kirk Peterson, Ashok Nedungadi and Randall Geiger which focuses on high frequency amplifier design was presented at the European Conference on Circuit theory and Design (ECCTD), Paris, Sept. 1987.
- A paper entitled "Monolithic Programmable State-Variable Biquadratic OTA-Capacitor (TAC) Filters" by E. Sánchez-Sinencio, S. C. Qin, R. L. Geiger and K. Peterson which focuses on OTA-based filter design was presented at the European Conference on Circuit Theory and Design (ECCTD), Paris, Sept. 1987.
- A paper entitled "A Linear Monolithic Active Attenuator with Multiple Output Taps" by S. C. Qin and R. L. Geiger which focuses on increasing signal swing in OTA structures was presented at the Midwest Symposium on Circuits and Systems, Syracuse, New York, August 1987.
- Several integrated test structures have been designed, fabricated and tested. A brief summary of these structures appears in Table 3.0-1.

Copies of these papers are attached in Appendix A.

Table 3.0-1

Silicon Test Structures Fabricated for this Project

ID No.	Major Purpose	Brief Description
DCASP Implementations:		
1	DCASP-1	6 th -order general purpose filter block
10	DCASP-2	6 th -order general purpose filter block
DCASP Component Test Vehicles:		
4		Analog switch test cell
6		Programmable capacitor array test cell
7		DCASP-1 digital support logic test cell
OTA Development:		
3		OTA with 2 selectable output stages
8		Modified OtA with 2 selectable output stages
11		OTA with 6 selectable output stages
DAC Development:		
5		6-bit 64 element linear resistor string DAC
9		6-bit binary tree linear DAC
12		6-bit binary tree logarithmic DAC
Performance Detectors and S/H's:		
2		Performance Detector based upon 2/H-1
13		Performance Detector based upon S/H-2
14		Single S/H-3 test cell
17		Performance Detector based upon S, μ -1 with modified OP Amp
18		Single S/H-3 test cell with modified Op Amp
Performance Detector Subcomponent Test Vehicles:		
15		High-Frequency S/H Op Amp
16		Performance Detector - Subcomponent Linearities
19		High-Frequency S/H Op Amp with Added Zero

4.0 Status of Accomplishments

Two generations of the CSP have been designed, fabricated and tested. The most advanced version, DCASP-2, was designed to have over three decades of center frequency adjustment and over three decades of bandwidth adjustment. The frequency adjustment range went from approximately 2KHz to 2MHz. Resolution in center frequency was to within 0.5% of the nominal center frequency over the entire range and bandwidth resolution was to within 1%. This circuit was also totally electronically reconfigurable. The basic functionality, reconfigurability, and the wide adjustment range and fine resolution were experimentally verified.

A second accomplishment was the realization of a high performance operational transconductance amplifier. Although not specifically a stated goal, this structure is actually a major subcomponent in the CSP and should find applications well beyond this project. This OTA has a wide linear input range and a gain (g_m) which can be digitally adjusted over more than two decades. Resolution to 1% of any value of g_m over this entire range is attained. The performance of this operational transconductance amplifier was experimentally verified.

A third accomplishment relates to the tuning problem. A method of measuring the system transfer characteristics at fixed frequencies was introduced. A method of accurately approximating system characterization parameters based upon these measurements was presented. This was based upon fitting spline functions to the measured data points and then numerically determining the system parameters from the spline functions. A tuning algorithm based upon these spline function fits which should be practical for a useful class of system functions was proposed.

A fourth accomplishment was in the design of a monolithic performance detector. A performance detector based upon a high speed sample and hold followed by a slower precision A/D converter was designed. The key individual building blocks which comprise this performance detector have been fabricated and tested for basic functionality.

A fifth accomplishment was in the generation of a set of test structures which constitute portions of the CSP and performance detector blocks. These test structures were fabricated and tested. They are useful for helping characterize the present CSP and performance detector as well as in the refinement of these structures in the next generation of circuits.

Details about the designs and tests of the circuits mentioned in this section appear in Sections 1 and 5 of this report.

A sixth accomplishment was in the development of a tuning host. This tuning host uses a commercial pc-based system and serves as a test vehicle for characterizing the performance of the blocks internal to the DCASP as well as a vehicle for experimentally

evaluating the performance of tuning algorithms.

5.0 TESTS

A total of 20 different test circuits have been fabricated and are reported in this section. The first 19 are integrated circuit designs and the last is the tuning host which was constructed on a conventional proto board with a standard microprocessor and "glue logic" parts. Most of these structures are test circuits which serve as sub-components in the CSP and/or performance detector. The most important structures are the DCASP-2 block in Sec. 5.10, the high resolution OTA of Sec. 5.11 and the performance detector block of Sec. 5.15. Most tests have focused on basic functionality and the results have been briefly summarized to keep the length of this section manageable. More detailed dynamic measurements of the test cells discussed in Sections 5.10, 5.11 and 5.13 are ongoing and will be reported in the near future. A discussion of the test results for the tuning host appears in Sec. 2.4 of this report. A listing of the test vehicles follows.

DCASP Implementations:

- Sec. 5.1 DCASP-1 6th-order general purpose filter block
- Sec. 5.10 DCASP-2 6th-order general purpose filter block

DCASP Component Test Vehicles:

- Sec. 5.4 Analog switch test cell
- Sec. 5.6 Programmable capacitor array test cell
- Sec. 5.7 DCASP-1 digital support logic test cell

OTA Development:

- Sec. 5.3 OTA with 2 selectable output stages
- Sec. 5.8 Modified OTA with 2 selectable output stages
- Sec. 5.11 OTA with 6 selectable output stages

DAC Development

- Sec. 5.5 6-bit 64 element linear resistor string DAC
- Sec. 5.9 6-bit binary tree linear DAC
- Sec. 5.12 6-bit binary tree logarithmic DAC

Performance Detectors and S/H's:

- Sec. 5.2 Performance Detector based upon S/H-1
- Sec. 5.13 Performance Detector based upon S/H-2
- Sec. 5.14 Single S/H-3 test cell
- Sec. 5.17 Performance Detector based upon S/H-1 with modified Op Amp
- Sec. 5.18 Single S/H-3 test cell with modified Op Amp

Performance Detector Subcomponent Test Vehicles:

- Sec. 5.15 High-Frequency S/H Op Amp
- Sec. 5.16 Performance Detector - Subcomponent Linearities
- Sec. 5.19 High-Frequency S/H Op Amp with Added Zero

5.1 DCASP-1 6th-Order General Purpose Filter Block

Name:	DCASP-1
MOSIS ID:	22143
Fab. ID:	M6BYCA-1
Technology:	CBPE-MOSIS 3 μ CMOS double-poly p-well process
Fabricated:	December 1986-January 1987
Chip Size:	7900 μ \times 9200 μ (72.68mm ²)
Active Area:	5700 μ \times 7300 μ (41.61mm ²)
Number of Pads:	27
Packaging:	64 pin package
Status:	Tested

Purpose:

This test chip is used to verify the functionality and measure the performance of the DCASP implementation. Both the individual and the cascaded biquad structures are studied.

Description:

The DCASP-1 implementation consists of three cascaded biquad structures plus associated interconnections. The structure has been described in detail in [32] and in previous sections of this report. The layout of the test cell is shown in Fig. 5.1-1. A block diagram is given in Fig. 5.1-2. A diagram showing the pinouts on the IC is given in Fig. 5.1-3. Following is a description of each pin.

Pin 1: Bulk	Connection to n ⁺ Substrate
Pin 2-9: D0-D7	Data Lines
Pin 11-16: A0-A5	Address Lines
Pin 18: CS	Chip Select
Pin 20: Clk	Clock
Pin 32: V _{DD}	Positive Supply
Pin 34: V _{ref} ⁺	Upper Reference Voltage
Pin 36: V _{ref} ⁻	Lower Reference Voltage
Pin 38: V _{bias}	DC Input Voltage used to Bias the Currents in the Cascoded Input Stages of the OTA's

Pin 40: Resp	Test output; response line of analog bus
Pin 42: Exc	Test input; excitation line of analog bus
Pin 58: Gnd	Common node
Pin 60: Output	Analog signal output
Pin 62: Input	Analog signal input
Pin 64: V_{SS}	Negative supply

Test Plan:

Testing may be classified as functional testing or performance testing. Functional testing of the DCASP-1 chip includes verification of the following:

- 1) configurability of the individual biquads as HP, BP, LP, AP, LPN, or HPN filters;
- 2) tunability of pole and zero frequencies and bandwidths via adjustment of the capacitance of the capacitor arrays and the g_m of the OTAs;
- 3) configurability of 4th or 6th order structure by cascading individual biquads.

Performance testing of the DCASP-1 chip includes determination of the following:

- 1) frequency and bandwidth adjustment range;
- 2) frequency and bandwidth resolution;
- 3) dynamic range;
- 4) distortion;
- 5) noise level;
- 6) nonidealities of model;
- 7) power dissipation.

The DCASP-1 chip is tested in the digital CSP controller board (see Sec. 2.4).

Experimental Results:

Fig. 5.1-4 shows the frequency response of one biquad of DCASP-1 in the HP, BP, LP, and LPN configurations for the same settings of the g_m 's and C's of the biquad. These curves verify that the biquad can be configured as a HP, BP, LP, or LPN filter.

That the pole frequency can be adjusted using the capacitor arrays is verified by Fig. 5.1-5. This figure shows four of the responses generated by varying C_6 and C_7 over their entire range, while keeping $C_6 = C_7$. It was also verified experimentally that the pole frequency can be adjusted by the fine adjustment of g_m . The coarse g_m adjustment was found to be inoperable; this led to the discovery of a design error in the output mirror of the OTA.

That the pole bandwidth can be adjusted using the capacitor array and the fine g_m adjustment was also verified experimentally. The coarse bandwidth adjustment via the coarse g_m adjustment could not be verified; again, this was due to the design error in the output mirror of the OTA.

It was also verified that a 4th or 6th order structure can be obtained by cascading the individual biquads. Fig. 5.1-6 shows frequency response curves for the three biquads individually (#1, #2, #3), for biquads #1, and #2 in cascade (4th), and for biquads #1, #2, and #3 in cascade (6th).

The performance testing of DCASP-1 was hampered by the lack of the coarse g_m adjustment noted above. Still, several of these tests were performed; results are given in Table 5.1-1 for a single biquad.

The range of pole frequencies obtained by $C_6 = C_7$ adjustment is seen from Fig. 5.1-5 to be from 300 kHz to 1.2 MHz. The range of pole bandwidths is the same. It is anticipated that these ranges will be extended after modifications to the OTA are made to allow a coarse g_m adjustment.

The resolutions in the pole frequency and in the pole bandwidth were not determined.

Extensive testing beyond that reported here was not done because of the design error which inhibited the coarse g_m adjustment. More extensive measurements have been made on the second-generation DCASP structure in which the design errors have been corrected. The latter structure is discussed in Sec. 5.10 of this report.

Table 5.1-1: Summary of measured filter performance for the biquad of DCASP-1.

	Lowpass ¹	Bandpass ²
Passband Noise Density ($\eta V/\sqrt{Hz}$)	270	250
3 dB Bandwidth (kHz)	760	580
Total Inband Noise (mV_{rms})	0.20	0.20
1% Distortion Level V_{rms})	1.0	1.2
Dynamic Range (dB)	73	76

¹Lowpass configuration: $B_{BP} = B_{LP} = B_{HP} = 0$
 $C6, C7, g_{m1}, g_{m2}, g_{m3}$ set at maximum values
 g_{m5} set at minimum non-zero values
 g_{m4} set at zero

²Bandpass configuration: $B_{BP} = B_{LP} = B_{HP} = 0$
 $C6, C7, g_{m2}, g_{m3}$ set at maximum values
 g_{m4}, g_{m5} set at minimum non-zero values
 g_{m1} set at zero

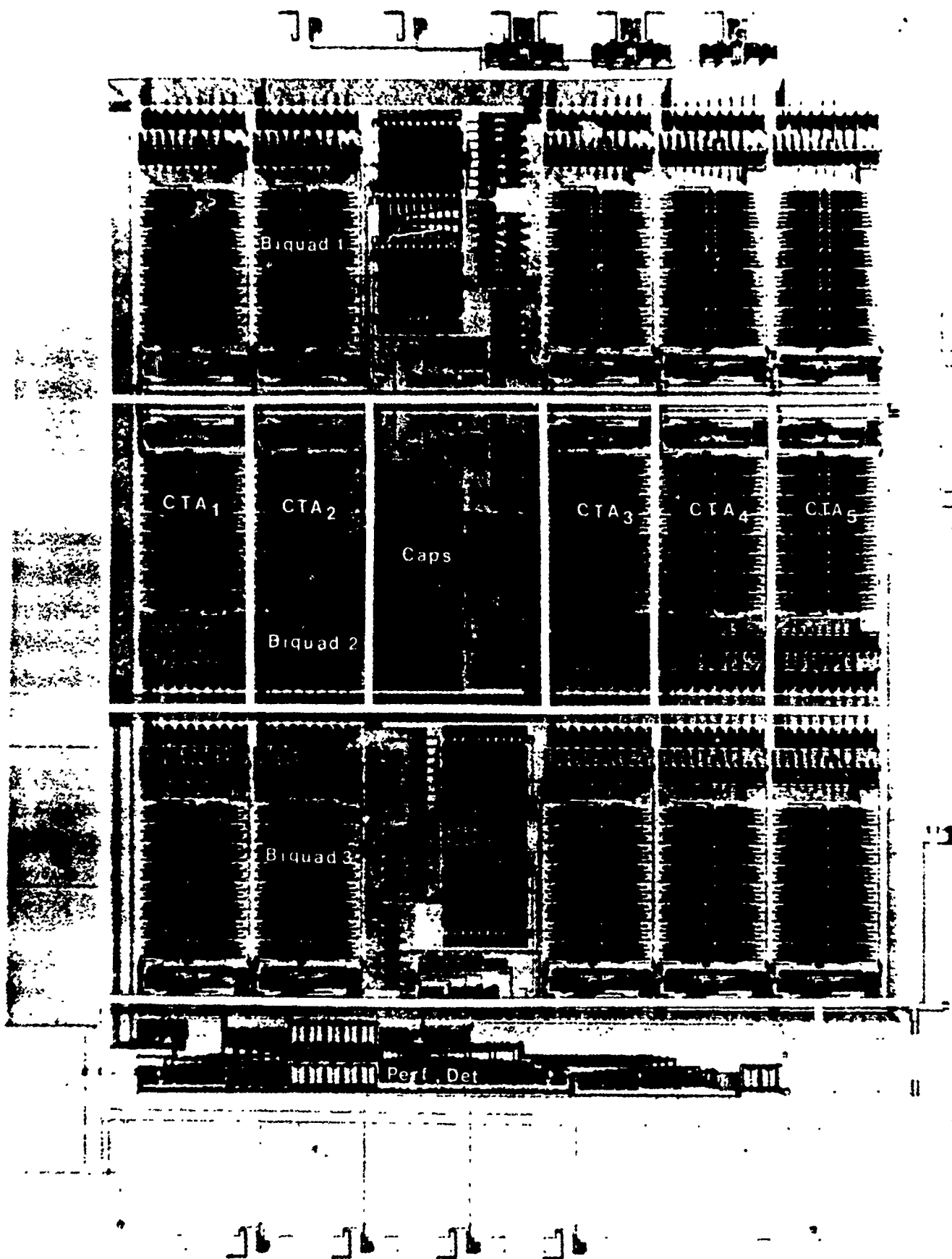


Fig. 5.1-1: Layout of DCASP-1.

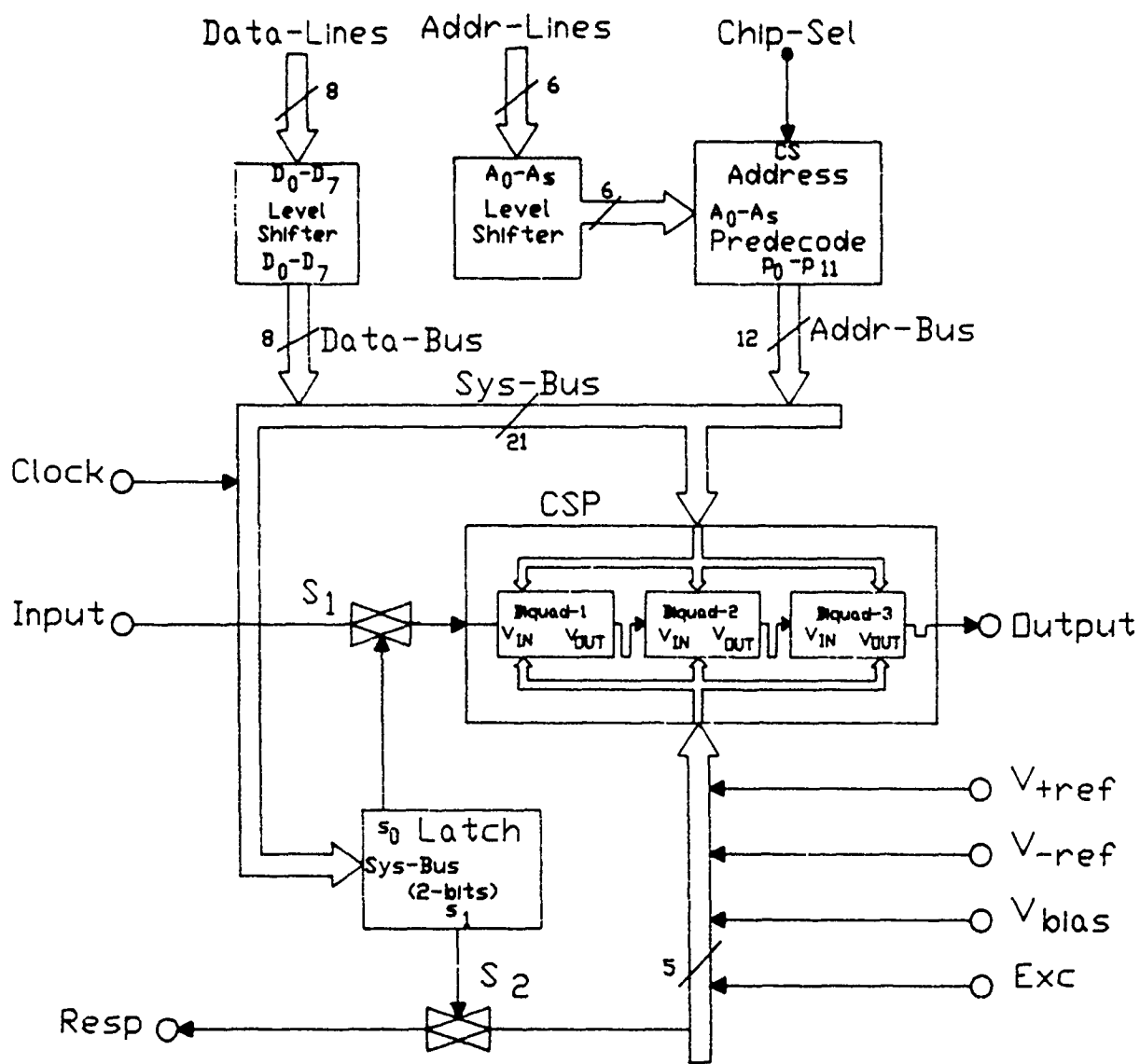


Fig. 5.1-2: Block diagram of DCASP-1.

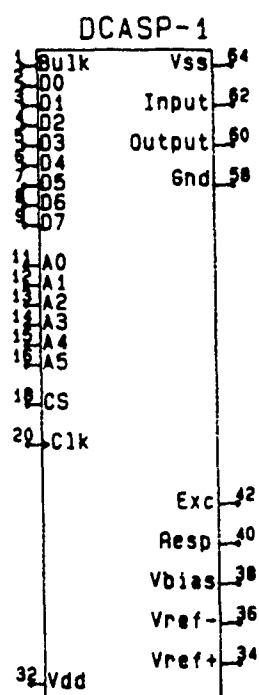


Fig. 5.1-3: Pinouts for DCASP-1 test cell.

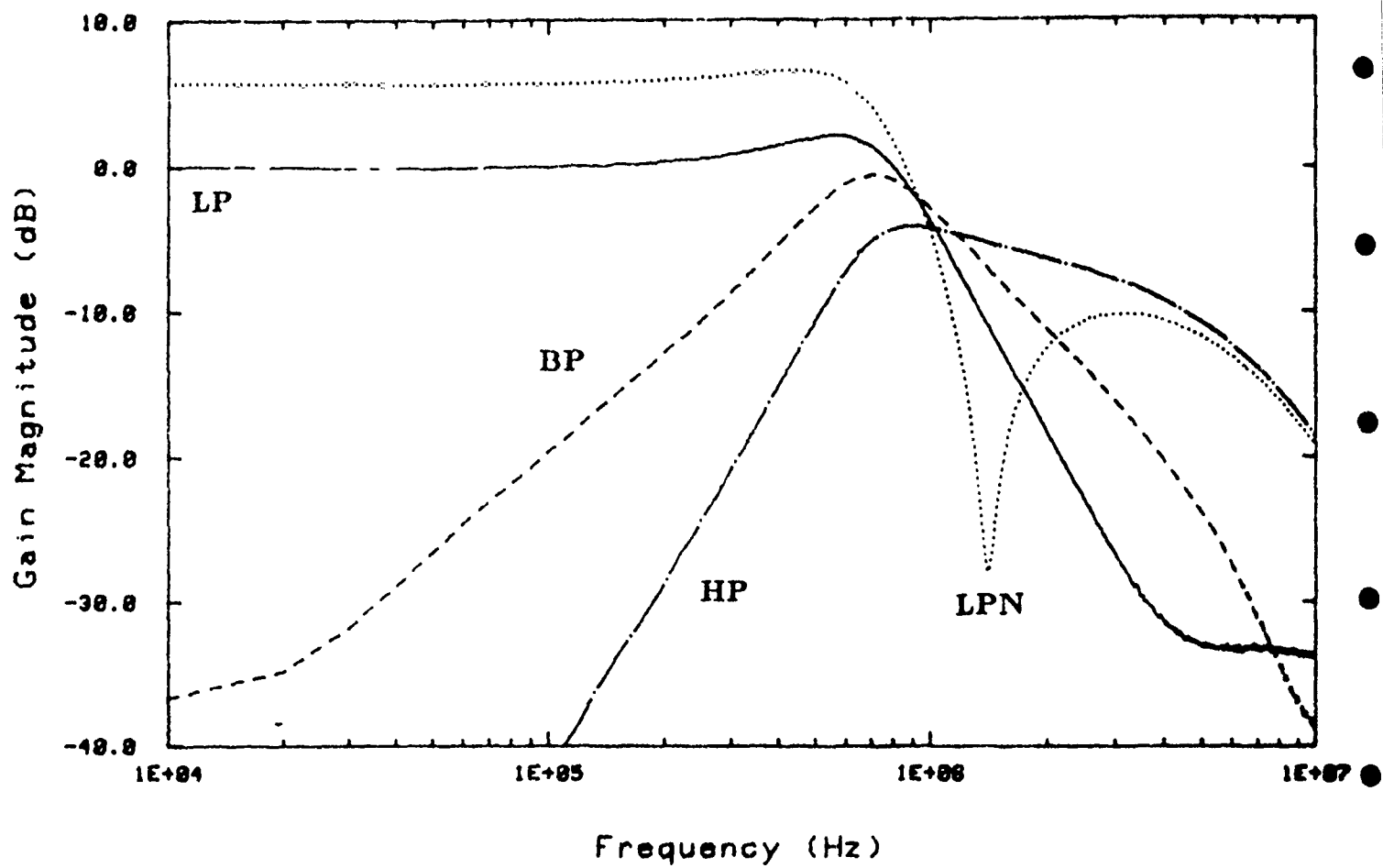


Fig. 5.1-4: Various filter transfer functions realized by Biquad 1 of DCASP-1.

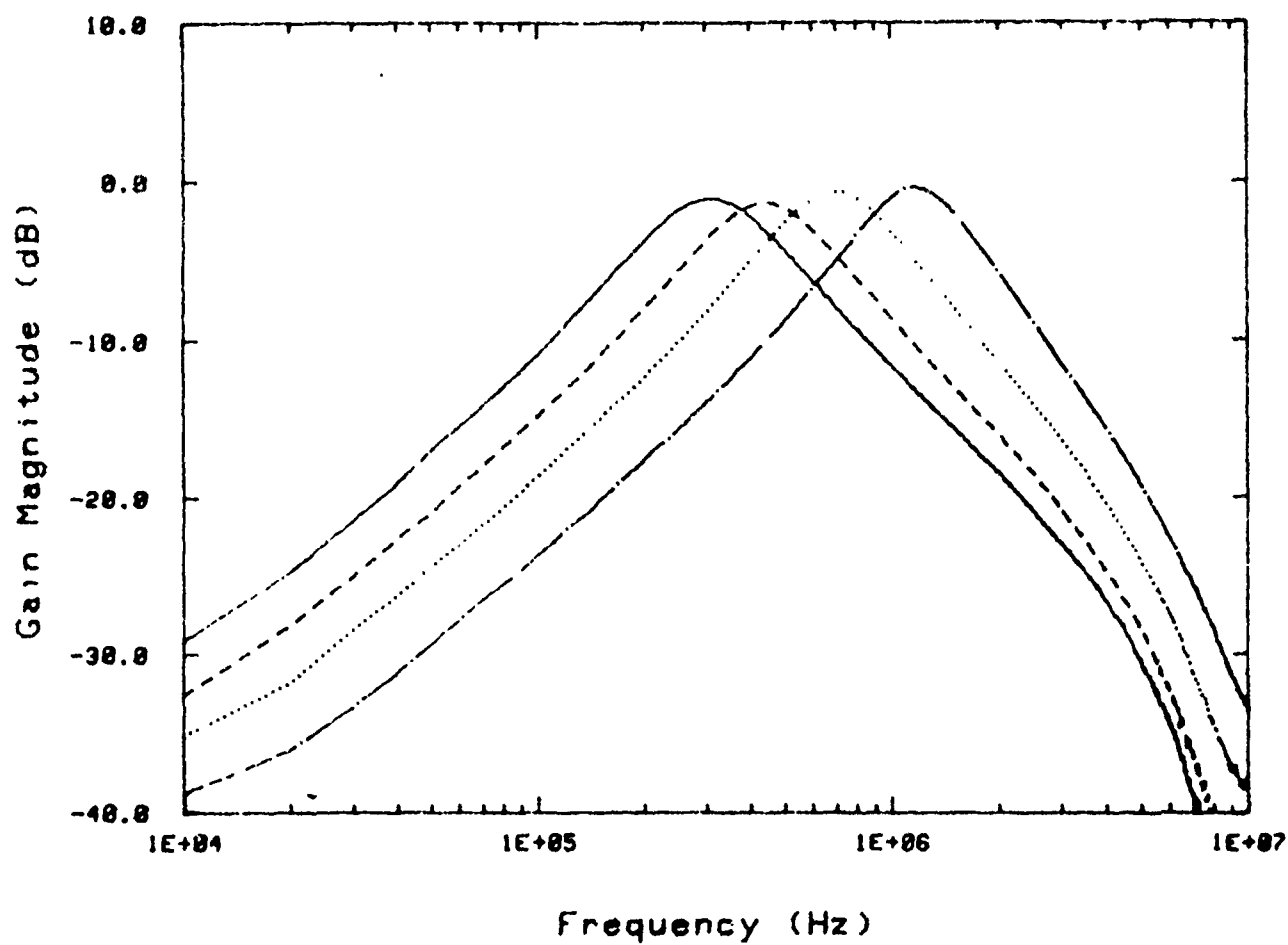


Fig. 5.1-5: Bandpass filter transfer functions obtained by adjusting capacitor arrays C6 and C7 of Biquad #1 of DCASP-1.

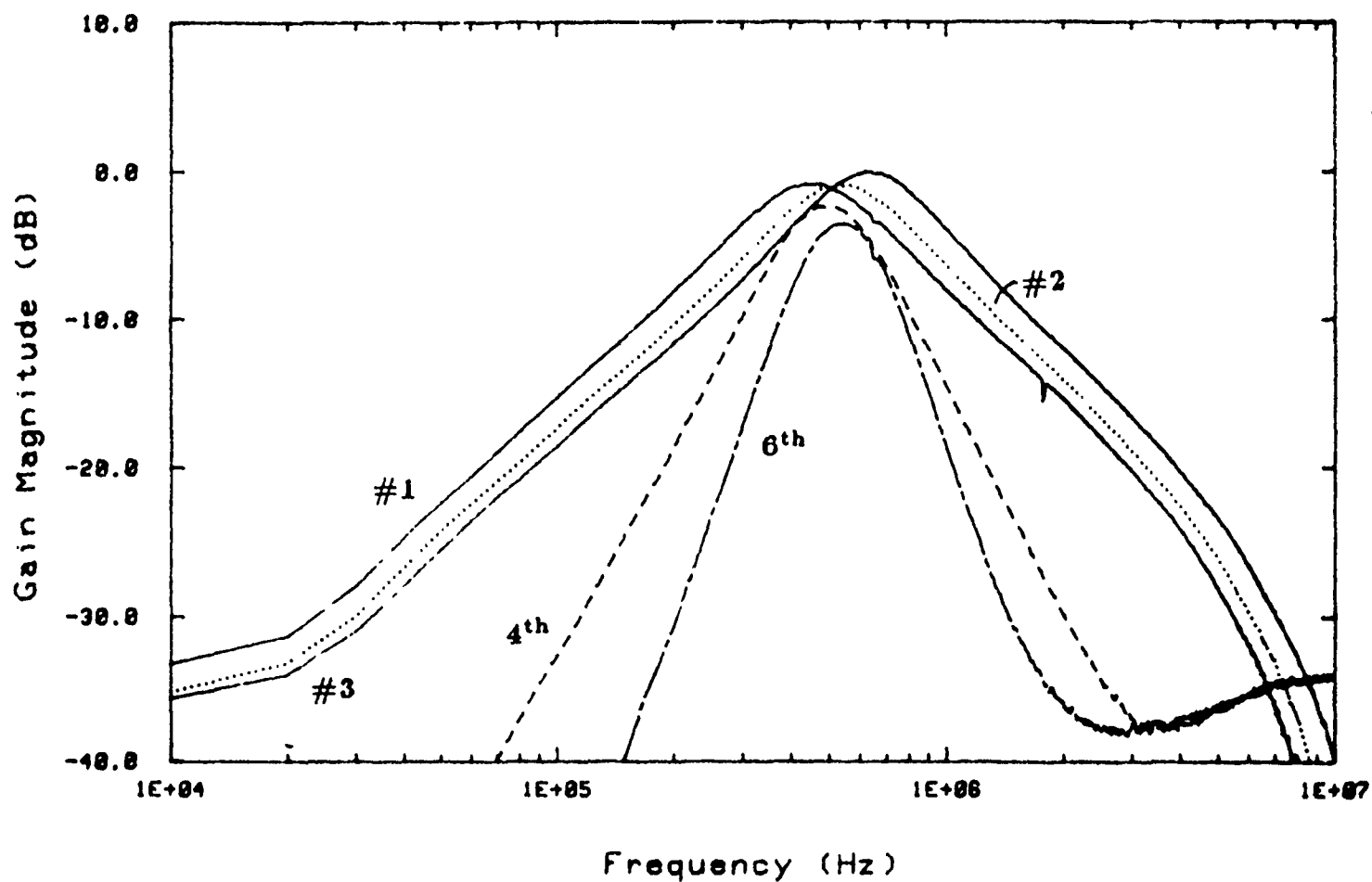


Fig. 5.1-6: Higher order bandpass filters obtained by cascading individual biquads.

5.2 Performance Detector based upon S/H-1

Name:	S/H-1
MOSIS ID:	22143
Fab. ID:	M6BYCA-1
Technology:	CBPE — MOSIS $3\mu\text{m}$ CMOS double-poly p-well process
Fabricated:	December 1986 - January 1987
Chip Size:	$7900\mu\text{m} \times 9200\mu\text{m}$ (72.68mm^2)
Active Area:	$5135\mu\text{m} \times 500\mu\text{m}$ (2.57mm^2)
Number of Pads:	32
Packaging:	64 pin package
Status:	Tested.

Purpose:

This Performance Detector, as originally discussed in the '86 Technical Report [32] for this project, was intended to be the heart of the 1st generation S/H based performance measurement system and provide an interim solution at low frequencies ($< 200\text{kHz}$), until the 2nd generation high-frequency S/H design could be developed. This particular Performance Detector has several purposes:

- (1) Provide DCASP-1 with an on-chip performance detector.
- (2) Provide for the characterization of the analog portion of the S/H-1 design and determine its inherent limitations.
- (3) Verify the operation of the complex digital logic that "optimally" interfaces to a single multiplexed A/D.

This test vehicle will be briefly described in the following section, along with its associated test results. Because of a design error in the digital control logic, the analog portion of the Performance Detector was left in-operative. The S/H-1 architecture was superseded by that of S/H-2 so the circuit was not re-fabricated after the digital control logic error was detected.

Description:

This test structure contains two arrays of five S/H-1 cells, capable of sampling the excitation and response signals simultaneously, at five different instants. Each of these samples can then be converted to a digital signal via a multiplexed external A/D. Also included in this subsystem was the interface and multiplexer logic necessary to interface the S/H array to the shared A/D. This complete system was developed and included as part of the DCASP-1 chip, with pin-outs shown in Fig. 5.2-1 and die photograph in Fig. 5.2-2

A block diagram of the performance detector exclusive of the A/D converter is shown in Fig. 5.2-3. This is comprised of a sample and hold array, sampling control logic and A/D

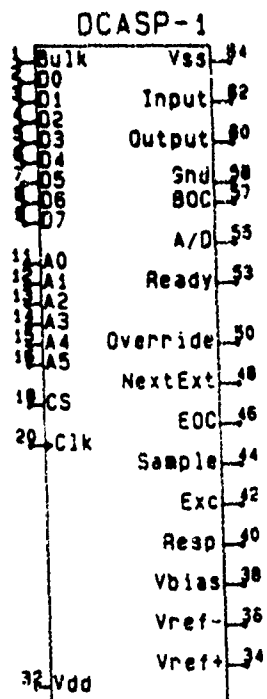


Fig. 5.2-1. Pin-outs for the S/H-1 test vehicle.

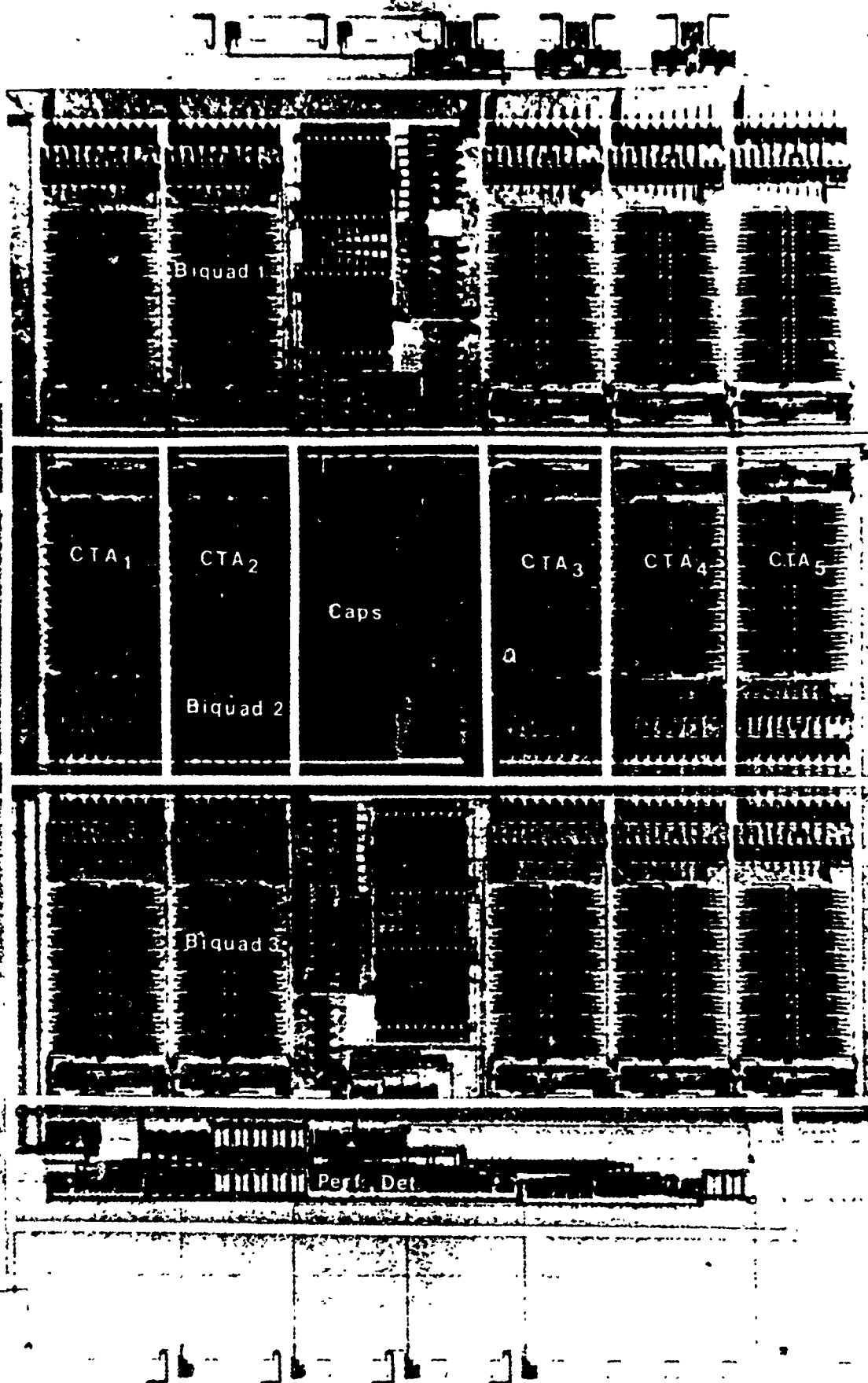


Fig. 5.2-2. Die photograph of DCASP-1 with an array of 5×2 S/H-1 cells with complex control logic and A/D interface, as shown at the bottom of the photograph and labeled "Perf. Det.".

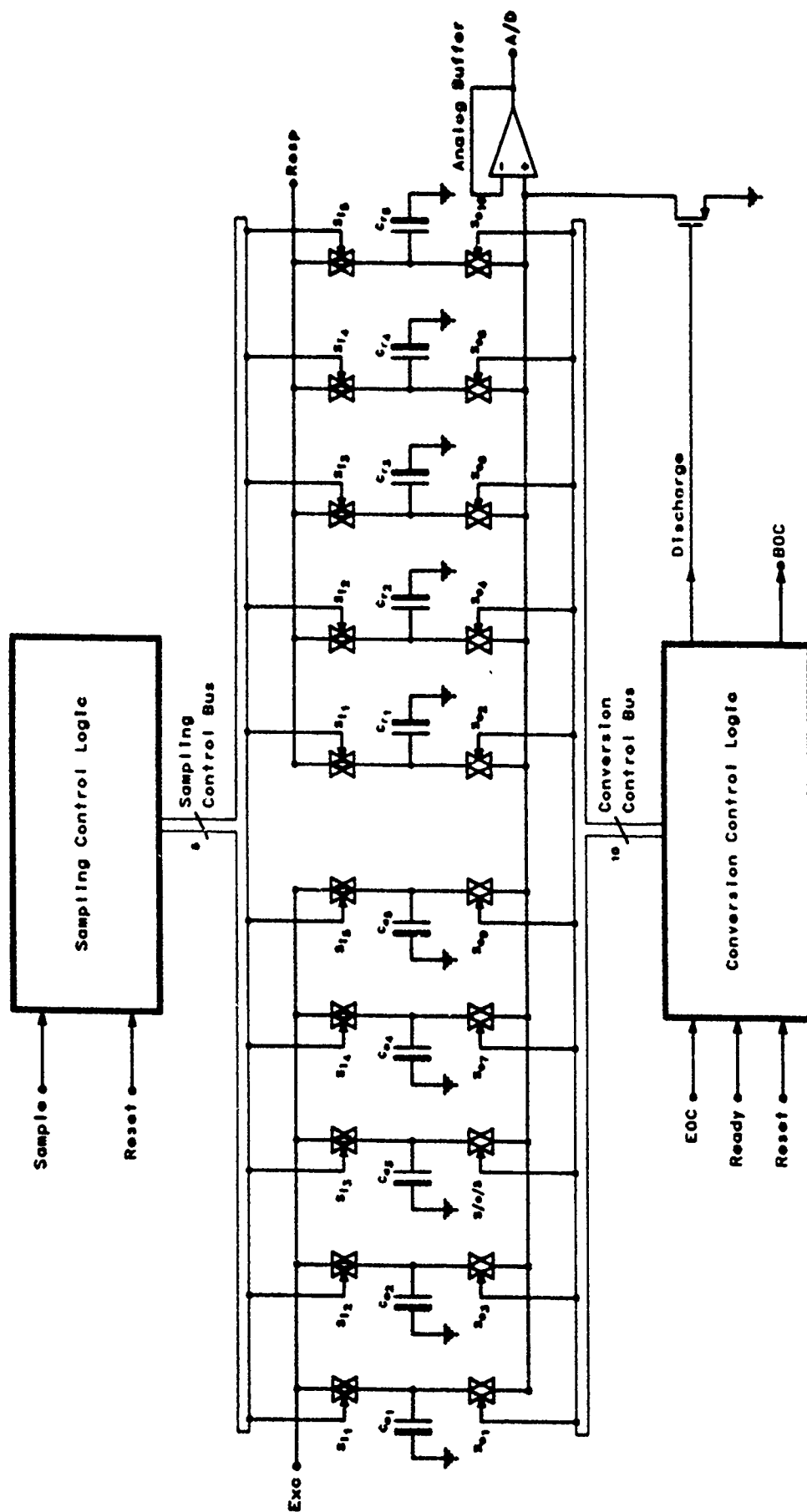


Fig. 5.2-3. Block diagram of the integrated portion of the S/H-1 based Performance Detector.

conversion control logic. The performance detector shown here was designed to interface to a single microprocessor controlled A/D converter.

Once the performance detector is reset by logically toggling the *Reset* line via physically addressing the location 02₁₆ on the DCASP address bus (A_0 through A_5); five consecutive samples of both *Exc* and *Resp* signals can be simultaneously taken on the falling edge of *Sample*. These analog voltage samples are stored on holding capacitors, $C_{e,1} - C_{e,5}$ and $C_{r,1} - C_{r,5}$. Following sampling, these samples are sequentially buffered and supplied via the A/D signal to a single external multiplexed A/D converter, where it is converted to a digital word.

To better understand the operation of this array, a single analog S/H cell is shown in Fig. 5.2-4. Shown here is a "sampling" analog switch, constructed from the floating-well complimentary switch architecture and a "conversion" analog switch, constructed from a regular complimentary switch. Both of these analog switches are described in detail in section 2.2.2.3a.

The sampling control logic consists of a dynamic shift register that is used to automatically index each sequential sample by physically controlling the opening and closing of the analog switches associated with the S/H-1 array.

The conversion control logic is much more complex and can be broken down into the following parts:

- (1) Analog Control Logic — When an analog sample and held voltage is ready for conversion, this logic throws the appropriate analog switch ($S_{o,1} - S_{o,10}$) to buffer this analog signal to the external A/D. Prior to patching this analog signal through to the unity gain buffer, any excess charge on the input of the buffer is discharged when the analog control logic pulses the *Discharge* signal, thus eliminating any reminiscence of previous samples.
- (2) Sampled Queue Manager Logic — This logic monitors which of the 5 "samples" have been taken by the "sampling control logic" and which of these 10 voltage samples have been converted to digital words. From this information it can be decided if a voltage sample is ready for conversion and which voltage sample is next. This optimizes the interaction between the sampling mechanism and the conversion process, by queueing up each consecutive sample to be converted at a later time when the A/D is available. Thus this easily facilitates both high-speed and low-speed sampling rates, where high-speed/low-speed sampling rates are defined as sampling the excitation and response signals much faster/slower than the conversion speed of the A/D. In the event this logic does not perform as expected the signal *Override* bypasses this logic and substitutes the externally provided signal *NextExt* for the dynamic shift register control line. This allows for the samples to be manually one-by-one gated to the outside world.
- (3) A/D Interface Logic — This logic monitors the internal control lines supplied by

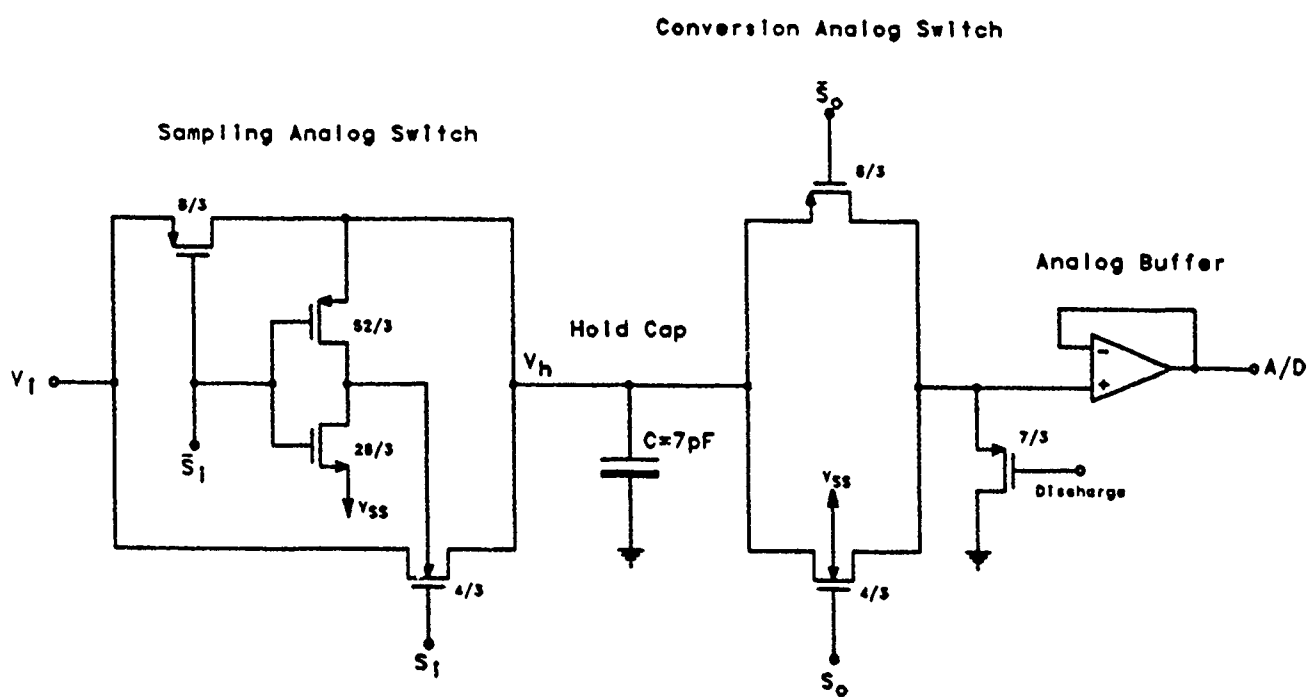


Fig. 5.2-4. Single S/H-1 cell circuit schematic.

the Sampled Queue Manager, and the external signals *Ready* and *EOC* (end-of-conversion), and decides when to trigger the conversion process by pulsing the *BOC* (beginning-of-conversion) signal with a 250 η sec. pulse. The *EOC* signal is supplied by the A/D, indicating when the A/D has completed the conversion of the last sample. The *Ready* signal is supplied by the microprocessor, indicating when it has stored the previous digital word and is now ready and waiting.

The remainder of the pins contained in Fig. 5.2-1 not yet discussed here, are used by the DCASP-1 CSP and discussed in detail in Section 5.1.

Experimental Results:

Due to a design error in the sampling control logic, there was not sufficient dead time between the "sampling" (the transition from track-mode to hold-mode) of the i^{th} S/H cell and the $i^{\text{th}} + 1^{\text{st}}$ S/H cell switching into track-mode. This overlap or race condition resulted in a large variation in each sequential sample of the analog array of S/H's. This variation can be attributed to charge sharing between the adjacent S/H cells right at the instance the input signal is sampled.

The conversion control logic seems to be operational based upon observations, though it is difficult to be conclusive with the aforementioned sampling problems persisting.

The A/D interface logic was functional, but the pulse width of the one-shots used in the timing of this logic was 50% smaller than designed. This can be attributed to process variation, though it is recommended that the integrating capacitors of this structure be decreased and the channel length of the "slow" inverter be increased to compensate for the change in capacitor size. This should drastically reduce the overall size of all of the one-shots.

Lastly, it is recommended that in future generations of the S/H based Performance Detectors, redirected the complex digital interface logic used here should be removed with sampling and conversion control to the external test circuitry. This will allow the analog portion of these designs to be more exactly characterized by obtaining direct control of the analog switch control lines.

5.3 OTA with 2 selectable output stages

Name: OTA 2-Bit-1
MOSIS ID: 22119
Fab. ID: M6BYAA-4
Technology: CBPE—MOSIS 3μ CMOS double-poly p-well process
Fabricated: December 1986-January 1987
Chip Size: $2300\mu \times 3400\mu$ ($7.82mm^2$)
Active Area: $216\mu \times 784\mu$ ($.169mm^2$)
Number of Pads: 9
Packaging: 28 pin package
Status: Tested

Purpose:

This test chip is used to characterize the 2-output stage OTA used in the controlled transconductance amplifier (CTA) of DCASP-1. The g_m vs V_{tail} curve for the OTA is studied in order to determine the attainable g_m range. Also, since in the CTA the control voltage V_{tail} is the output of the DAC, the g_m vs V_{tail} curve yields the voltage range over which the DAC must operate in order to obtain the desired g_m adjustment range.

Description

A circuit schematic is given in Fig 5.3-1 and the device sizes are listed in Table 5.3-1. A diagram showing the pinouts on the IC is given in Fig 5.3-2. Following is a description of each pin.

Pin 1: Bulk	Connection to the n+ substrate of the chip.
Pin 8: V_b	DC input voltage used to bias the currents in the cascoded input stages of the OTA.
Pin 9: I_{out}	OTA output current.
Pin 10: B_0	The digital control for the smaller of the two OTA output stages. The stage is enabled for $B_0 = 1$.
Pin 11: B_1	The digital control for the larger of the two OTA output stages. The stage is enabled for $B_1 = 1$.
Pin 12: V_{DD}	The positive supply for the OTA circuit.
Pin 13: V_{in}^+	The positive input terminal of the OTA.
Pin 14: V_{SS}	The negative supply for the OTA circuit.

Pin 15: V_{in}	The negative input terminal of the OTA.
Pin 16: V_{tail}	The control voltage used to adjust the g_m of the OTA by adjusting the tail current in the cascoded structures of the OTA input stage.

Test Plan

The circuit shown in Fig 5.3-3 is used to test this OTA. The experimental value of g_m is computed from the equation

$$g_m = \frac{I_{out}}{V_{in}} = \frac{V_{out}}{R_{out}V_{in}} .$$

This is repeated for several values of the control voltage V_{tail} . From the resulting data, a plot of g_m versus V_{tail} may be constructed.

Experimental Results

An experimental plot of g_m versus V_{tail} was obtained for the case of $B_1B_0 = 10$; i.e., for the case where only the larger of the two output stages is enabled. This curve is shown in Fig 5.3-4. Segments of the curve may be approximated by straight lines; in particular, for $-3.8 < V_{tail} < -3.4$, the curve may be approximated as

$$g_m = 61.8V_{tail} + 257.9 ,$$

where V_{tail} is in volts and g_m is in μS . SPICE analysis of the OTA yields the relation

$$g_m = 40.5V_{tail} + 174.25 .$$

Discrepancies between this and the experimentally determined relationship are somewhat larger than would be anticipated from typical process variations. These differences should, however, not have a major affect in what is to follow.

Attempts to measure the g_m of the OTA for the case where only the smaller output stage is enabled led to the discovery of a circuit design error. Upon this discovery, full testing of the circuit was discontinued.

The error is in the method of disabling the output stages of the OTA. The OTA contains two differently-sized current mirror output stages which provide a coarse adjustment of g_m . The larger gain factor is provided by the stage consisting of M26, M27, M32 and M33 in Fig. 5.3-1. This stage is disabled by turning off the transmission gate formed by M38 and M39. With the transmission gate off, the current I_{O_2} does not contribute to the overall output current I_O . However, with the load removed in this way, the gain of the stage is greatly increased.

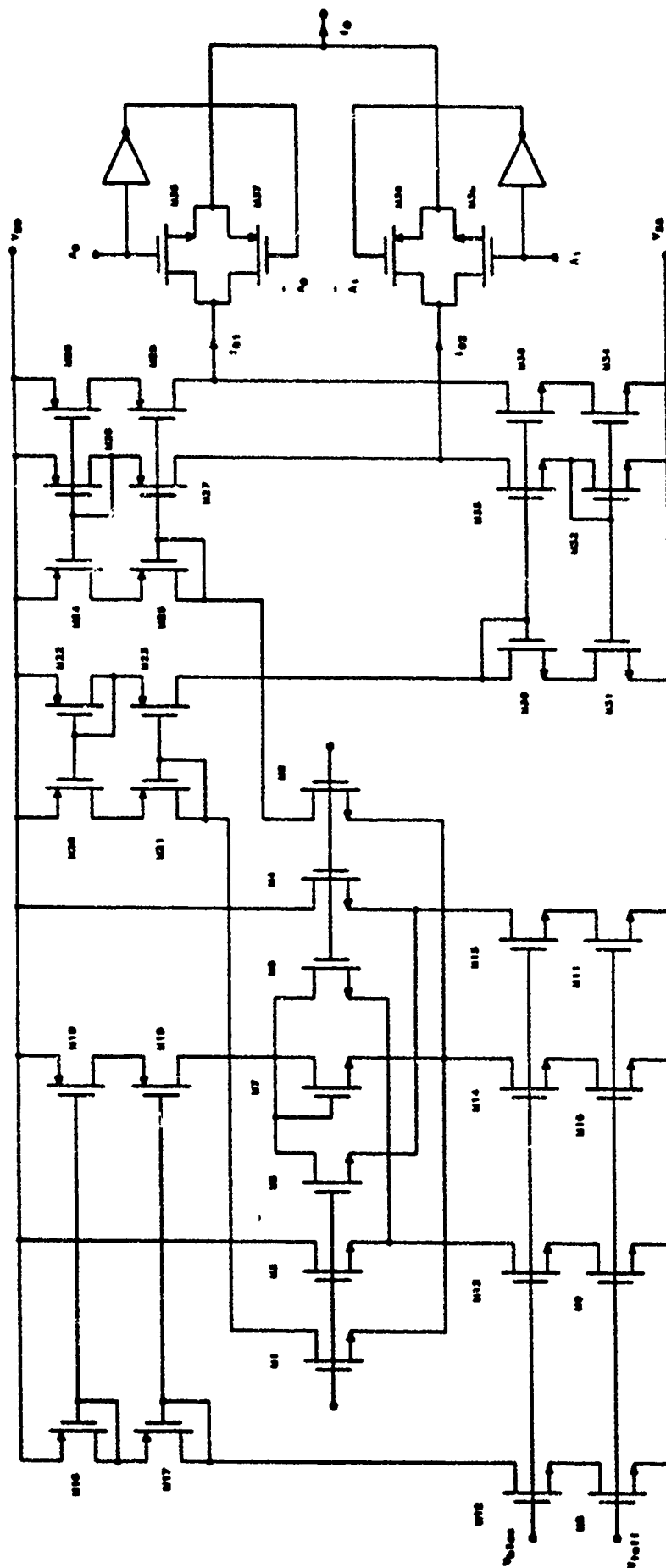


Fig. 5.3-1: Circuit schematic of 2-output stage OTA used in DCASP-1.

Table 5.3-1: Device sizing for OTA structure of Figure 5.3-1.

Device	SIZE (microns)	
	W	L
M1-M2	8	5
M3-M4	16	5
M5-M6	8	5
M7	7	5
M8, M12	40	3
M9-M11, M13-M15	80	3
M16-M17	60	3
M18-M21	120	3
M22-M23	60	3
M24-M25	120	3
M26-M27, M32-M33	60	3
M28-M29, M34-M35	6	3
M30-M31	60	3
M36, M38	15	3
M37, M39	32	3

OTA-2Bit

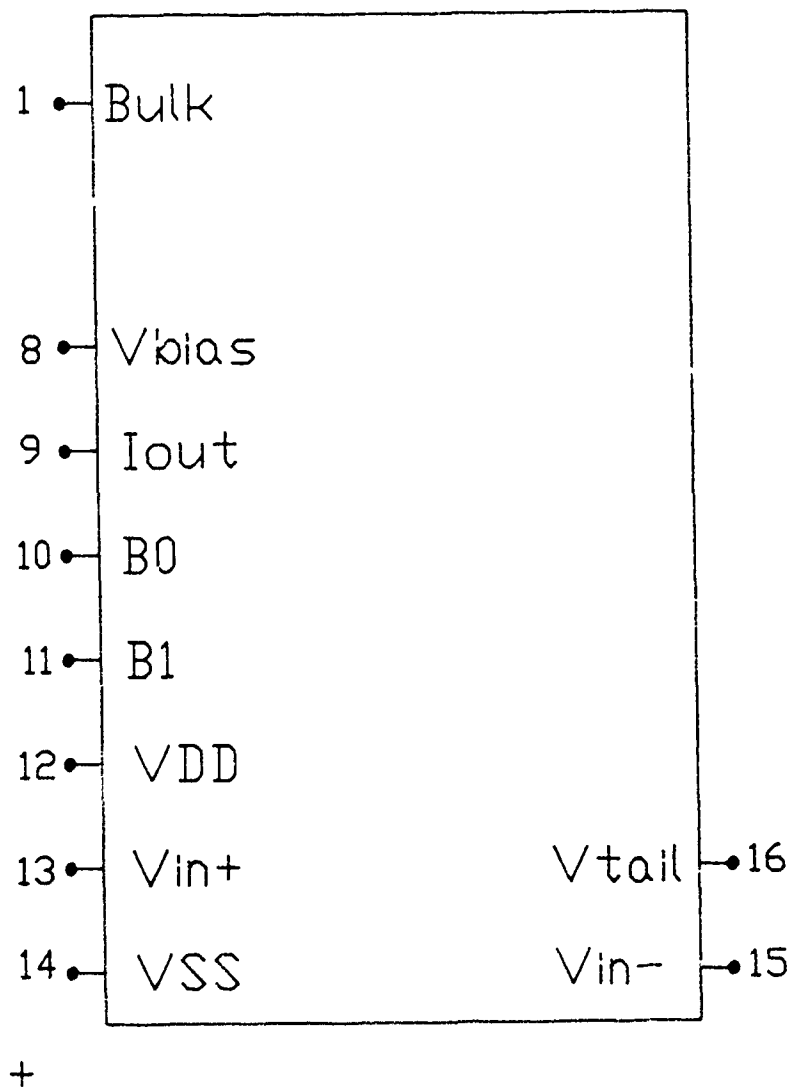


Fig. 5.3-2: Pinouts for 2-output stage OTA test device.

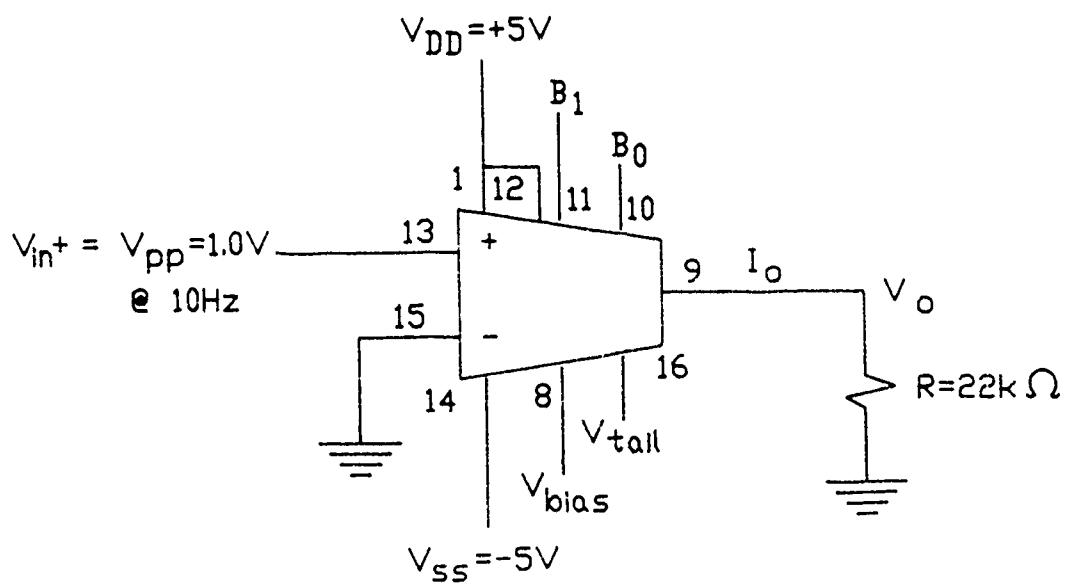


Fig. 5.3-3: Test circuit used to measure g_m as a function of V_{tail} .

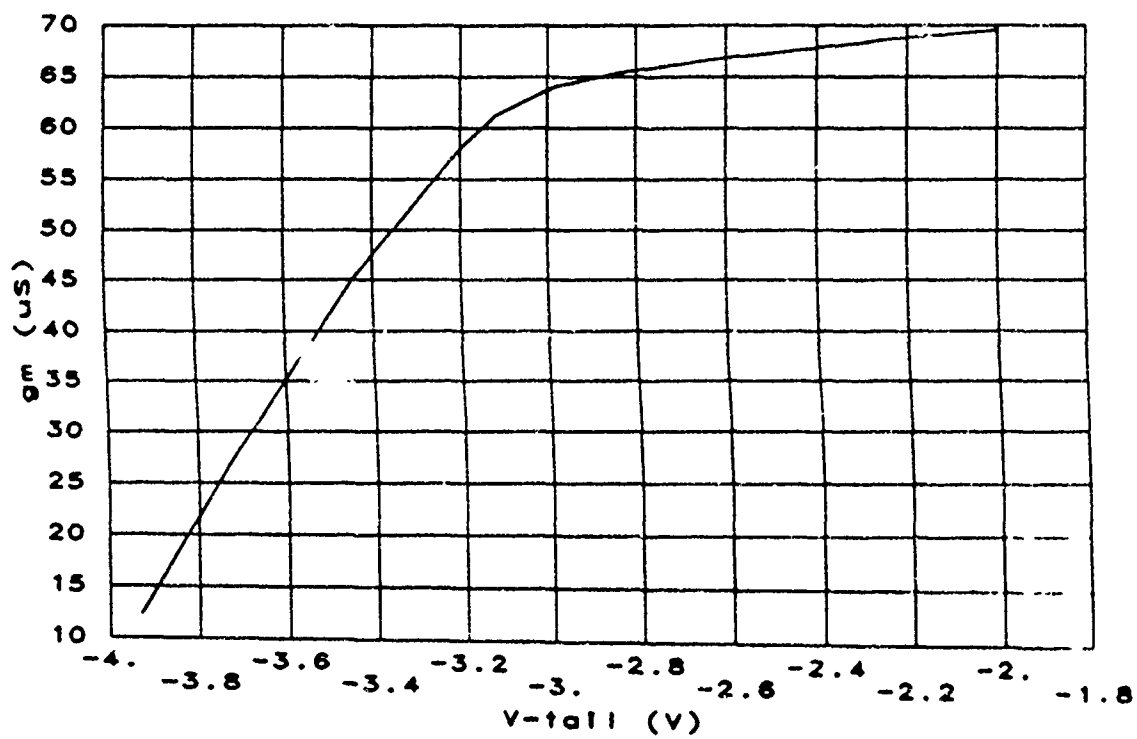


Fig. 5.3-4: Experimental g_m vs. V_{tail} for OTA of DCASP-1 - $V_{bias} = -1.5V$.

The result is that, for all but very small amplitude input signals, the gate voltages of $M26$ and $M32$, and hence of $M28$ and $M34$, become too close to the supply voltages V_{DD} and V_{SS} , respectively. Thus, for the case where only the smaller stage (consisting of $M28$, $M29$, $M34$, and $M35$) is enabled, the output is distorted, and the coarse g_m adjustment is essentially useless.

A new circuit was subsequently designed which does allow a coarse g_m adjustment without the problems outlined above. This circuit is discussed in Sec. 5.11.

5.4 Analog switch test cell

Name:	Analog Test
MOSIS ID:	22119
Fab. ID:	M6BYAA-4
Technology:	CBPE — MOSIS $3\mu m$ CMOS double-poly p-well process
Fabricated:	December 1986 - January 1987
Chip Size:	$2300\mu m \times 3400\mu m$ ($7.82mm^2$)
Number of Pads:	20
Packaging:	28 pin package
Status:	Tested

Purpose:

This test chip was designed to verify the proper operation of the three different type of analog switches used in DCASP-1 (MOSIS ID: 22143), and provides a means of extracting the specific process parameters for this processing run (M6BY), via a series of test devices. If DCASP-1 performs as expected, then this test structure will only be used as a functional test vehicle.

Description:

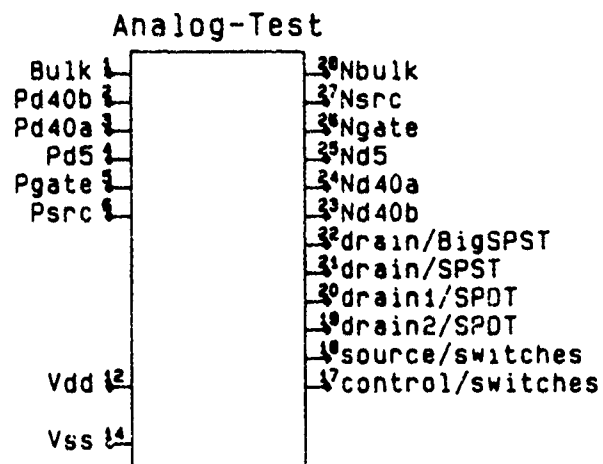
This test chip as shown in Fig. 5.4-1 contains three different analog switches, (i.e., a regular SPST, a large SPST and regular SPDT switch), 3 different sizes of p-channel MOSFET's and 3 different sizes of n-channel MOSFET's. The pins on the p-channel, n-channel and analog switch tests cells, shown in Fig. 5.4-2 have been multiplexed to reduce the number of pads required, without sacrificing the ability to test each device separately. The sizes of the MOSFET test devices were chosen to characterize both short-channel effects and matching from device to device.

A detailed circuit schematic for each of the analog switches are shown in Fig. 5.4-3, with devices sizes contained in Table 5.4-1. The SPDT analog switches are used to configure the Biquad via the B_{lp} , B_{bp} and B_{hp} bits stored in the Biquad control latch, shown in Fig. 1025-3 (e.g., the bottom-plate of each of the Programmable Capacitor Arrays is connected to the Biquad input signal or to ground, via one of these SPDT switches). The large SPST switches (B_{lgSPST}) are used in connection with each of the three remaining bits of the Biquad control latch, and are used to control where the input and output of each Biquad come from and goes to. The remaining analog switches are the regular SPST switch ($SPST$).

Test Plan:

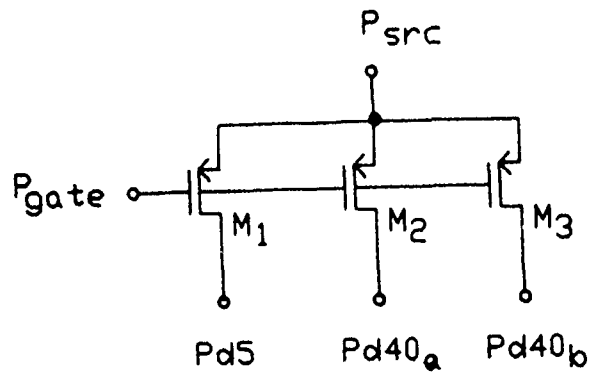
Functional Test:

Each of the analog switches will be configured as follows:

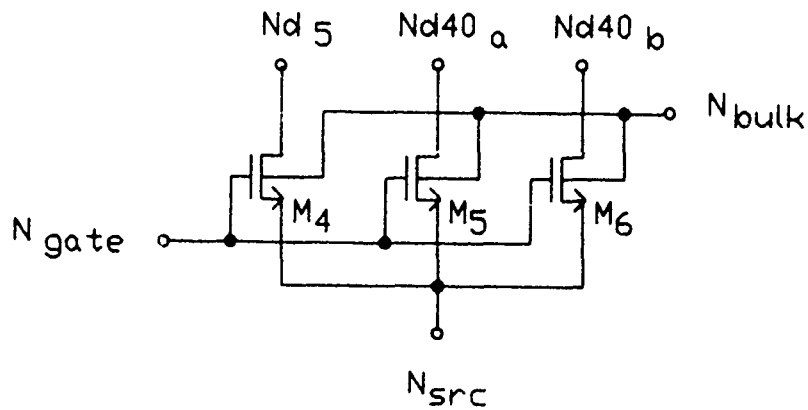


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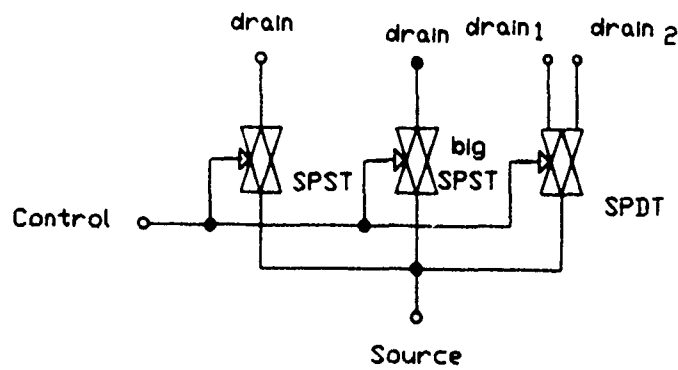
Fig. 5.4-1. Pin-outs for Analog test cell.



a) Circuit schematic of p-channel test devices.

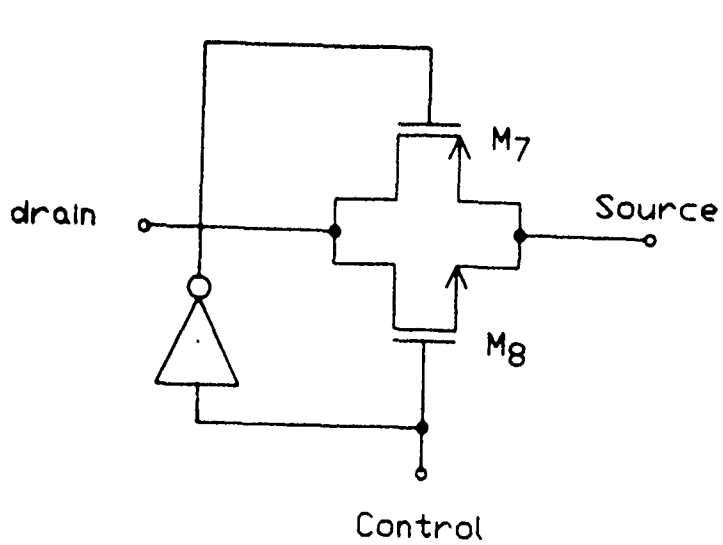


b) Circuit schematic of n-channel test devices.

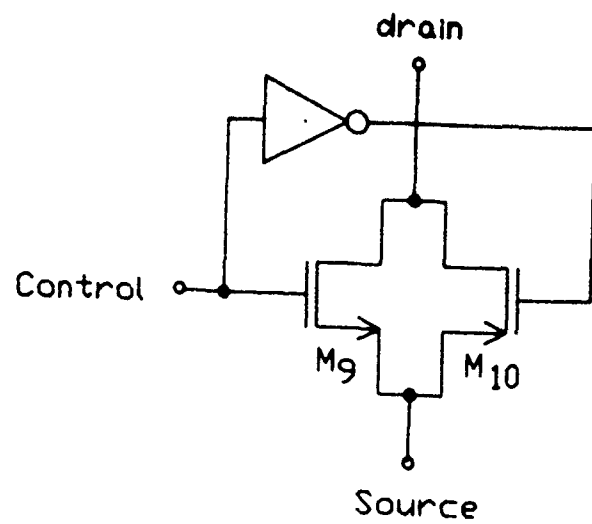


c) Circuit schematic of analog switches.

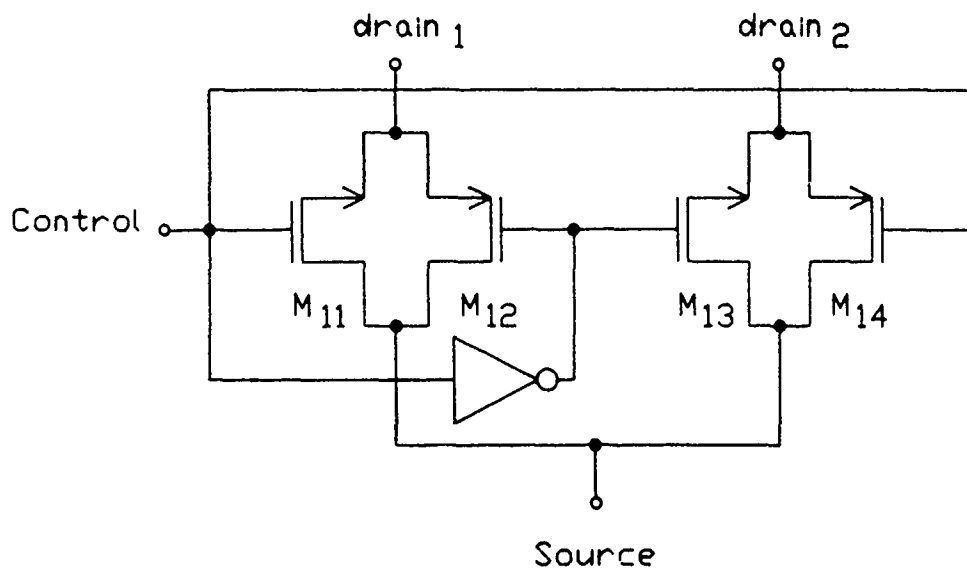
Fig. 5.4-1: Analog Switch Test Cell



(a) SPST



(b) BigSPST



(c) SPDT

Fig. 5.4-3. Circuit schematics of individual analog switches.

Table 5.4-1. Device sizes for Analog test cell.

Device	Size	
	<i>W</i>	<i>L</i>
M_1, M_4	$5\mu m$	$5\mu m$
M_2, M_3, M_5, M_6	$40\mu m$	$40\mu m$
M_7, M_{12}, M_{14}	$32\mu m$	$3\mu m$
M_8, M_{11}, M_{13}	$15\mu m$	$3\mu m$
M_9	$90\mu m$	$3\mu m$
M_{10}	$40\mu m$	$3\mu m$

- (1) connect the common source node of the analog switches to a low-frequency sinusoidal excitation; and
- (2) monitor each of the drains and source nodes on an oscilloscope.

Thus by switching each of the analog switches "on" and "off" via the common control signal, the sinusoidal input should appear and disappear on each of the drains. Once it has been confirmed that each of the devices are controlled properly, the input signal amplitude should be increased until the outputs (drains) begin to noticeably distort because of dynamic range restrictions.

Experimental Results:

A functional test was performed on each of the analog switches, as detailed in the test plan. The results of this test are listed below.

- (1) With a low frequency sinusoidal signal on the source input node of each of the analog switches, the drain output node was isolated when the devices was turned "off" and tracked the input signal when turned "on".
- (2) No noticeable distortion was observed when the input sinusoidal was increased to $\pm 2V$ signal levels.

This implies that the analog switches are indeed functional at low frequencies with typical signal swings.

5.5 6-Bit Linear DAC With Decode Logic

MOSIS ID: 22119
Fab. ID: M6BYAA-4
Technology: CBPE-MOSIS 3μ CMOS Double-Poly p-Well
Fabricated: December 1986-January 1987
Chip Size: $2300\mu \times 3400\mu$
Active Area: $850\mu \times 1600\mu$
Number of Pads: 17
Packaging: 28 Pin Package
Status: Tested

Purpose:

This test chip is used to characterize the monotonicity as well as the linearity of the Digital-to-Analog Converter (DAC) which has been used in DCASP-1 to provide the OTA control voltages.

Description:

There are two linear DAC circuits fabricated in this test chip, Large DAC and Small DAC. These are shown on the die photograph of Fig. 5.5-1. Each circuit has a resistive string with taps and pass transistors at uniformly spaced intervals. The pass transistor, once selected, will pass its tapped voltage to the control voltage line. The two ends of the resistor string are driven by two voltages, V_{ref-} and V_{ref+} . The first DAC circuit, also termed "large DAC", has three standard 2- to 4-bit decoders to pre-decode the input data. A 3-line decoder is then required at each tap to complete the data decoding. In Figs. 5.5-2 and 5.5-3, the block diagram and circuit schematic are shown respectively. The "Small DAC", as its name implies, saves considerable space by using the switching transistor tree instead of decoders (refer to Sec. 5.9 for details).

Test Plans:

The pin designations of the DAC test chip appear in Fig. 5.5-4. The biasing voltages and triggering signals are connected as follow:

$$V_{DD} = \text{Bulk} = +5V \quad (5.5 - 1)$$

$$V_{SS} = P - \text{Well} = -5V \quad (5.5 - 2)$$

$$A_i = +5V \text{ (enabling)} \quad (5.5 - 3)$$

$$\overline{CLK} = \pm 5V, 1000Hz \quad (5.5 - 4)$$

$$V_{ref1+} = V_{ref2+} = 0V \quad (5.5 - 5)$$

$$V_{ref1-} = V_{ref2-} = -5V \quad (5.5 - 6)$$

Sixty-four DC voltages have been measured from each of V_{out1} and V_{out2} pins by changing the 6-bit data word (D0-D5) to all possible combinations. The instrument used for DC measurements is the HP 3456A digital voltmeter which has been extensively used throughout this experiment.

Experimental Results:

The small DAC fabricated in this test chip is found not functional since the p-well was not connected during fabrication. The 64 DC voltages measured on the V_{out2} pin are listed in Table 5.5-1. The DAC is used for determining the OTA control voltages in biquad. Although the linearity is less important than monotonicity, it has been found, in Fig. 5.5-5, that the DAC circuit behaves rather linear characteristically. This 6-bit DAC seems to be capable of having finer resolution since the maximum LSB error is as low as 10.8% (Refer to Section 5.9 for the definition of LSB error and $\frac{R_N}{R_{total}}$).

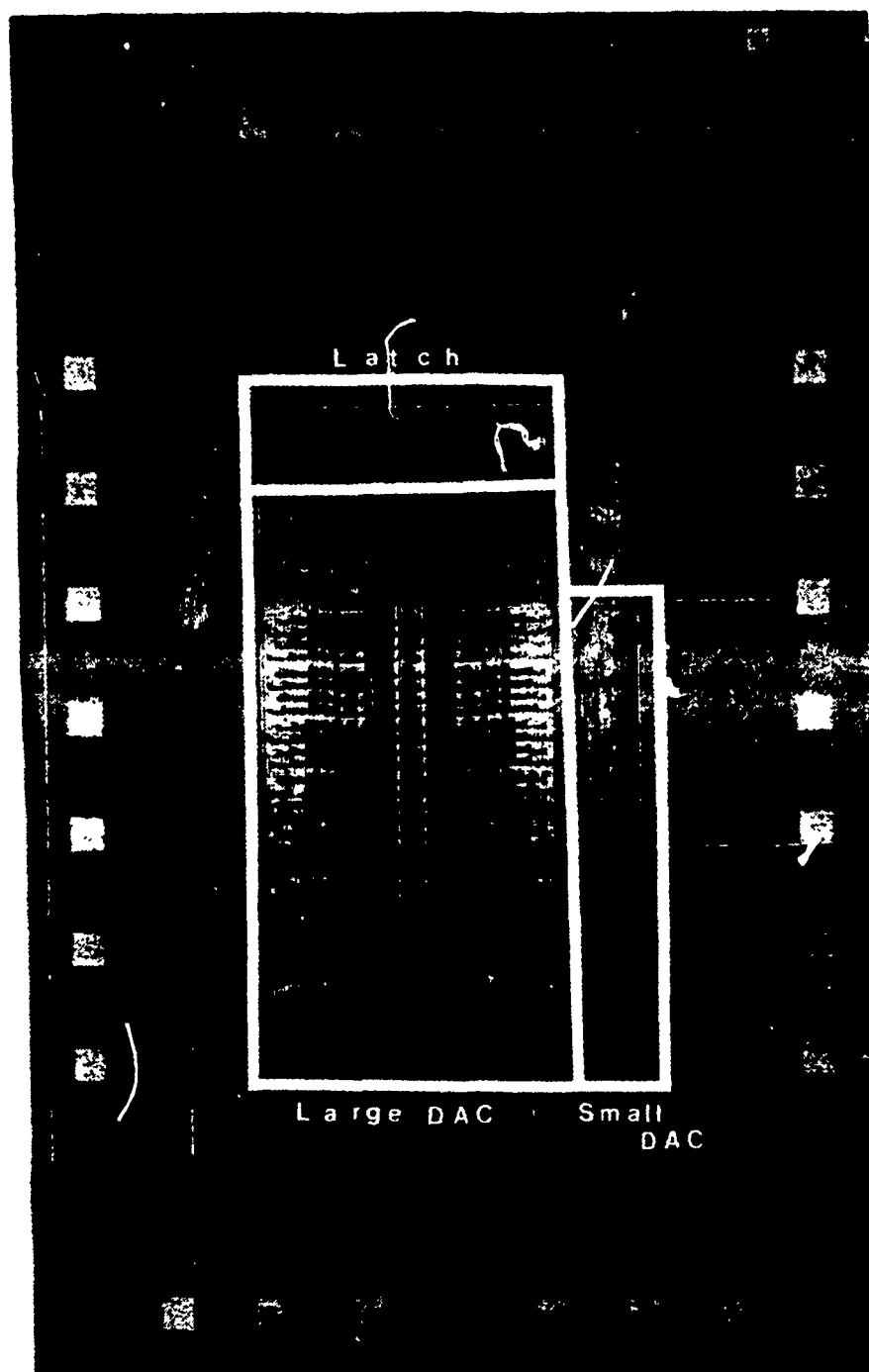


Fig. 5.5-1. The Die Photo of the Large DAC Test Chip

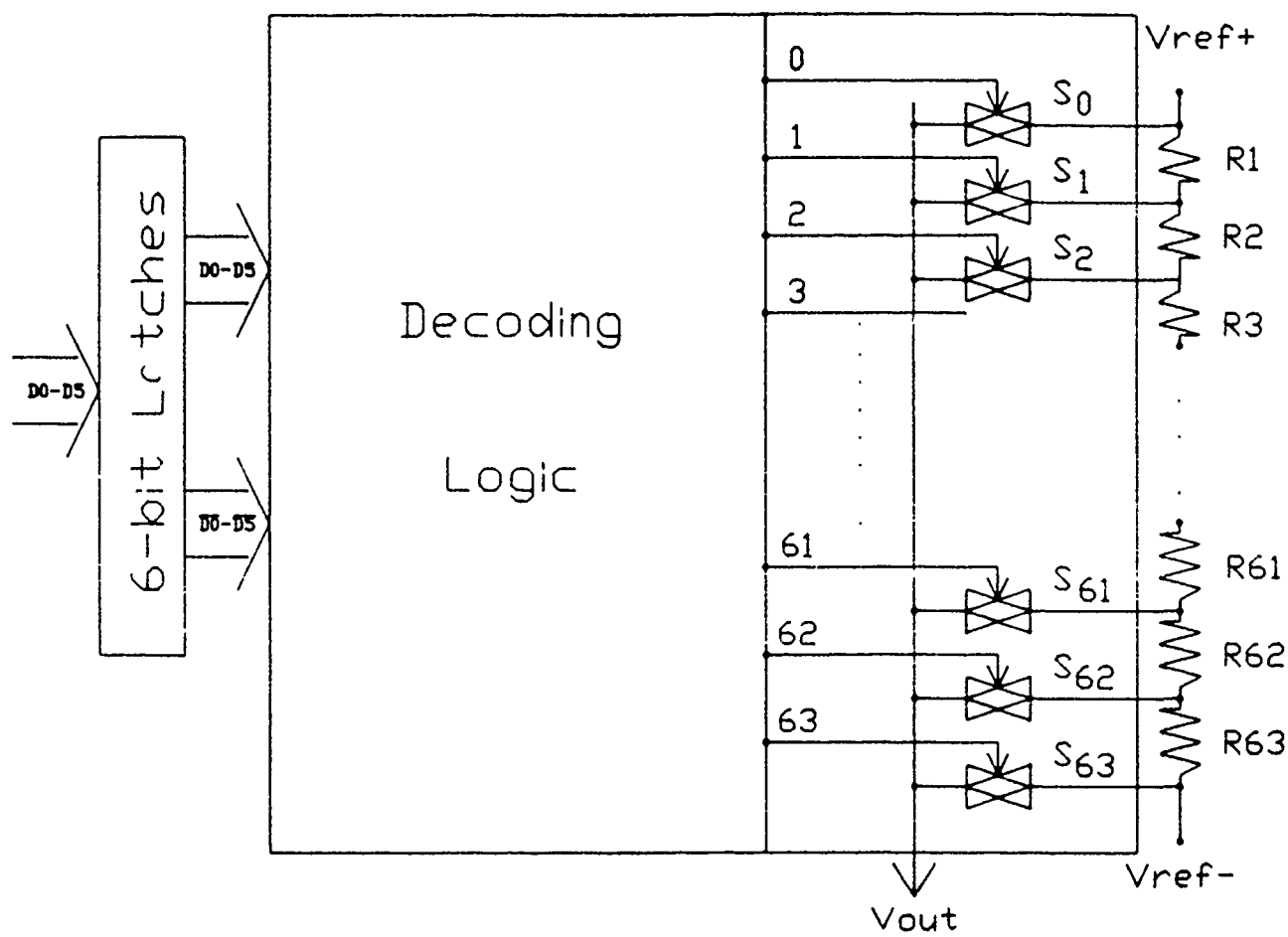


Fig. 5.5--2. Block Diagram of the Large DAC

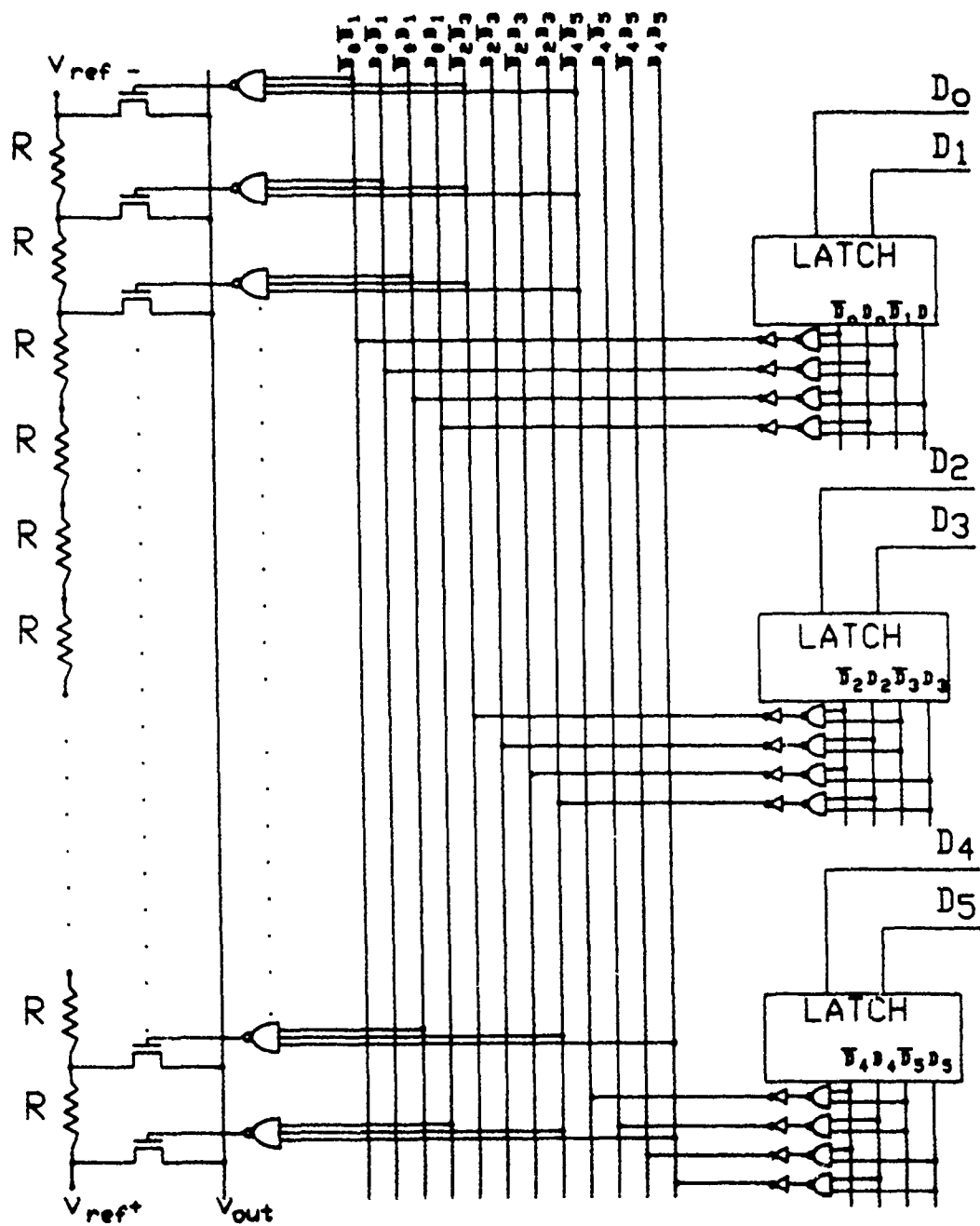


Fig. 5.5-3. Large DAC Decoding Circuit Schematic Diagram

1	Bulk	Pwell2	28
2	Vref2+	Vref2-	26
5	D5	Vout	24
6	D4	VDD	23
7	D3	Vref1-	22
8	D2	Vout1	21
9	D1	Vref1+	20
10	D0	Vss	19
11	CLK		
12	Ai		

Pin Assignments
of Large DAC

Fig. 5.5-4. Pin Assignments of Large DAC

Table 5.5-1 The DC Output Voltages and the Linearity Characteristics with Different Digital Settings.

Digital Setting	Output	LSB Error (%)	$\frac{R_N}{R_{total}}$ (%)	$\frac{R_N}{R_{N-1}}$
0	-4.962500	0.000000	0.749998	-
1	-4.885800	1.948212	1.534004	2.035344
2	-4.808700	3.385597	1.541996	1.005210
3	-4.731500	4.694971	1.543990	1.001299
4	-4.654000	5.620310	1.550007	1.003891
5	-4.576700	6.802282	1.545992	0.997410
6	-4.499000	7.472208	1.554003	1.005182
7	-4.421400	8.270146	1.552000	0.998711
8	-4.343500	8.684659	1.557999	1.003865
9	-4.265900	9.482596	1.552000	0.996150
10	-4.187900	9.769098	1.560001	1.005155
11	-4.110000	10.183612	1.557999	0.998716
12	-4.032100	10.598125	1.557999	1.000000
13	-3.952700	9.094601	1.588006	1.019260
14	-3.874300	8.869971	1.567998	0.987400
15	-3.796600	9.540202	1.553998	0.991071
16	-3.718500	9.698692	1.562004	1.005152
17	-3.640900	10.496630	1.552000	0.993595
18	-3.562800	10.655425	1.561999	1.006443
19	-3.484600	10.686514	1.563997	1.001279
20	-3.406400	10.717298	1.564002	1.000003
21	-3.328200	10.748385	1.563997	0.999997
22	-3.249600	10.267734	1.572003	1.005119
23	-3.171800	10.809953	1.556001	0.989820
24	-3.903300	10.457617	1.569996	1.008994
25	-3.015100	10.48840	1.564002	0.996182
26	-2.933600	6.300599	1.630001	1.042199
27	-2.858300	10.038836	1.506000	0.923926
28	-2.778500	8.024486	1.595998	1.059760
29	-2.699900	7.543834	1.572003	0.984966
30	-2.621600	7.446911	1.566000	0.996181
31	-2.543900	8.117142	1.553998	0.992336
32	-2.465500	7.892512	1.567998	1.009009

Table 5.5-1: The DC Output Voltages and the Linearity Characteristics with Different Digital Settings

Digital Setting	Output	LSB Error (%)	$\frac{R_N}{R_{total}}$ (%)	$\frac{R_N}{R_N-1}$
33	-2.387500	8.179014	1.560001	0.994900
34	-2.309100	7.954080	1.568003	1.005129
35	-2.231000	8.112875	1.561999	0.996171
36	-2.152500	7.760234	1.570001	1.005123
37	-2.074200	7.663311	1.566000	0.997452
38	-1.996000	7.694399	1.563997	0.998721
39	-1.918000	7.980901	1.560001	0.997445
40	-1.839700	7.883978	1.566000	1.003845
41	-1.761800	8.298491	1.557999	0.994891
42	-1.683600	8.329275	1.564002	1.003853
43	-1.604200	6.826208	1.587999	1.015343
44	-1.525100	5.706565	1.582000	0.996223
45	-1.446800	5.609643	1.566000	0.989886
46	-1.368500	5.512720	1.566000	1.000000
47	-1.290600	5.927080	1.558001	0.994892
48	-1.212000	5.446733	1.571999	1.008984
49	-1.134000	5.733234	1.560001	0.992368
50	-1.055870	5.853778	1.562598	1.001664
51	-0.977280	5.386003	1.571801	1.005890
52	-0.898350	4.483599	1.578600	1.004326
53	-0.820000	4.322670	1.567000	0.992652
54	-0.741480	3.944427	1.570400	1.002170
55	-0.663380	4.103147	1.561999	0.994651
56	-0.584590	3.379730	1.575800	1.008835
57	-0.506330	3.333859	1.565200	0.993273
58	-0.427140	2.099082	1.583800	1.011884
59	-0.348160	1.132787	1.579600	0.997348
60	-0.269640	0.754543	1.570400	0.994176
61	-0.191270	0.568051	1.567400	0.998090
62	-0.112790	0.240964	1.569600	1.001403
63	-0.034380	0.003348	1.568200	0.999108
			0.006876	

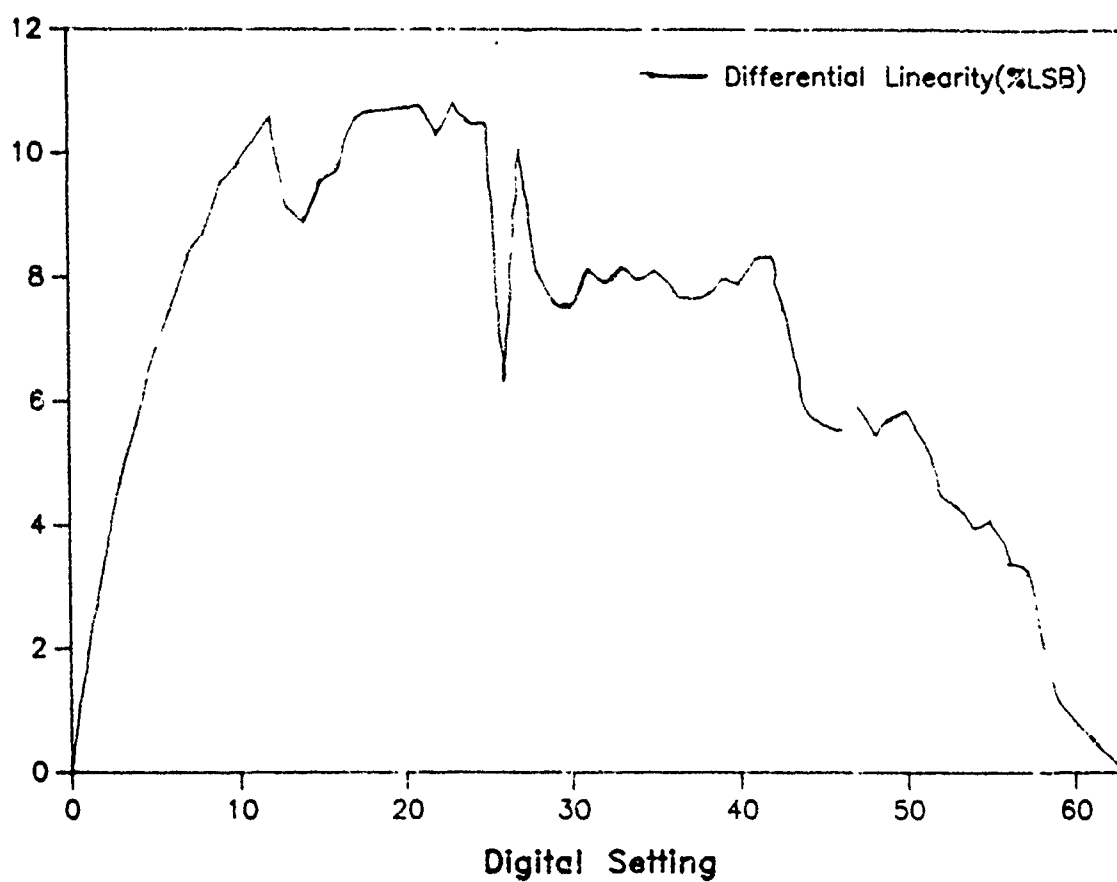


Fig. 5.5-5. DAC Performance Analysis of the Large DAC used in DCASP-1

5.6 Programmable Capacitor Array Test Cell

Name:	Cap Array-1
MOSIS ID:	22123
FAB. ID:	M6BYAA-2
Technology:	CBPE-MOSIS 3μ CMOS Double-Poly p-Well Process
Fabricated:	December 1986 - January 1987
Chip Size:	$2300\mu \times 3400\mu$
Active Area:	$1400\mu \times 2000\mu (2.8mm^2)$
Number of Pads:	14
Packaging:	28 Pin Package
Status:	Tested

Purpose:

This test device is used to confirm the functionality of the programmable capacitor array and associated digital logic circuitry of DCASP-1. The actual capacitance values are also measured. This test device is also used to confirm the functionality of the analog switches and the buffer of the biquad of DCASP-1.

Description:

A block diagram of the test cell is given in Fig. 5.6-1. A block diagram of the capacitor array given in Sec. 2.1.4 is repeated as Fig. 5.6-2. The die photograph of the test cell is given in Fig. 5.6-3.

A diagram showing the pinouts on the IC is given in Fig. 5.6-4. Following is a description of each pin.

Pin 1: Bulk Connection to the n^+ substrate of the chip.

Pin 2: \overline{CLK} Clock input to digital latches.

Pins 3-8: PX , $P5$
 $P4$, $P3$, $P2$, $P0$ Predecode address lines of system bus.

Pins 9-14: $D5 - D0$ Data lines of system bus.

Pin 15: V_{DD} Positive supply.

Pin 16: $C7_{51}$ Connection to bottom plate of $C7$ capacitor array via switch
 B_{HP}

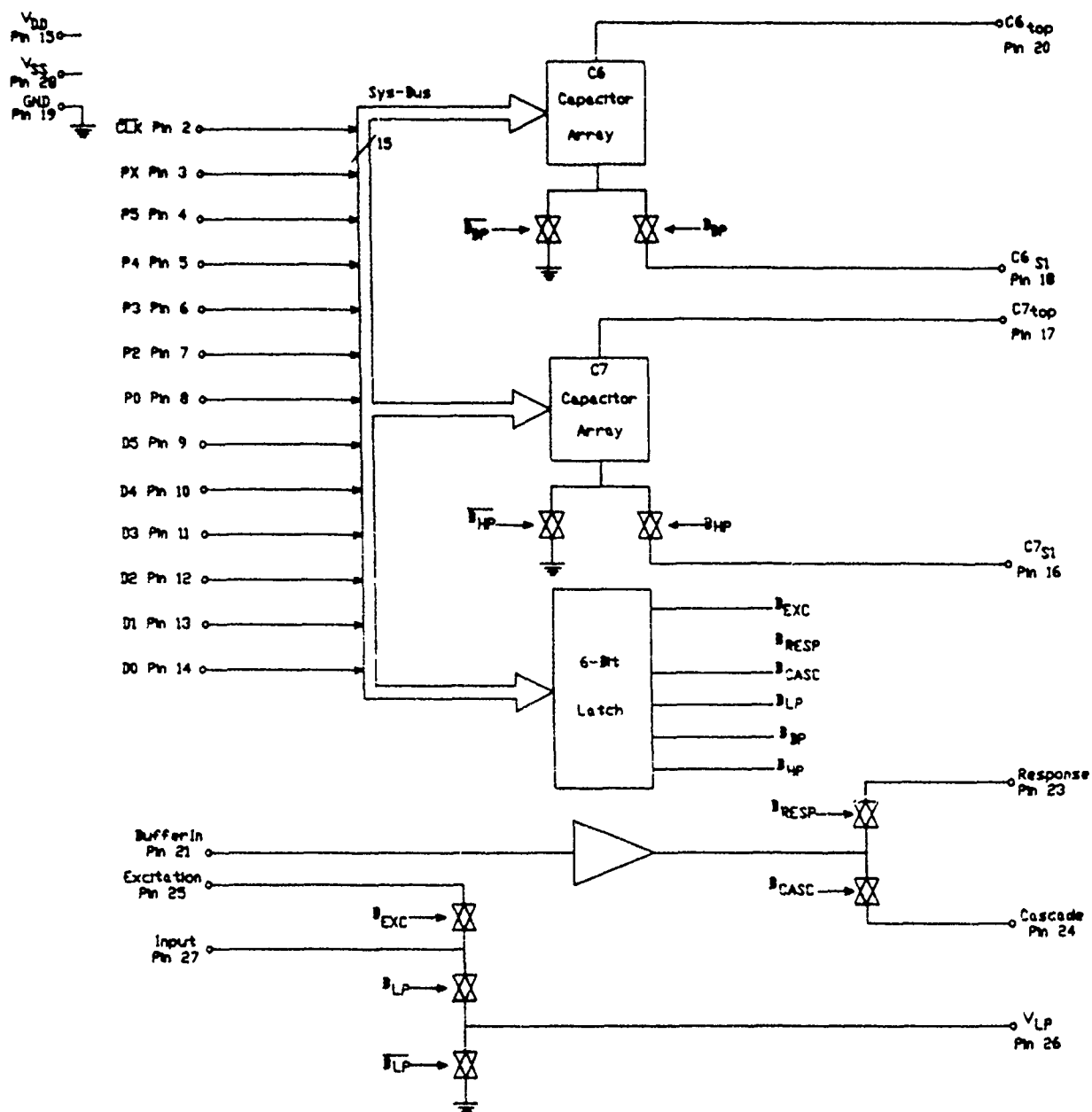


Fig 5.6-1: Block diagram of programmable capacitor array test cell.

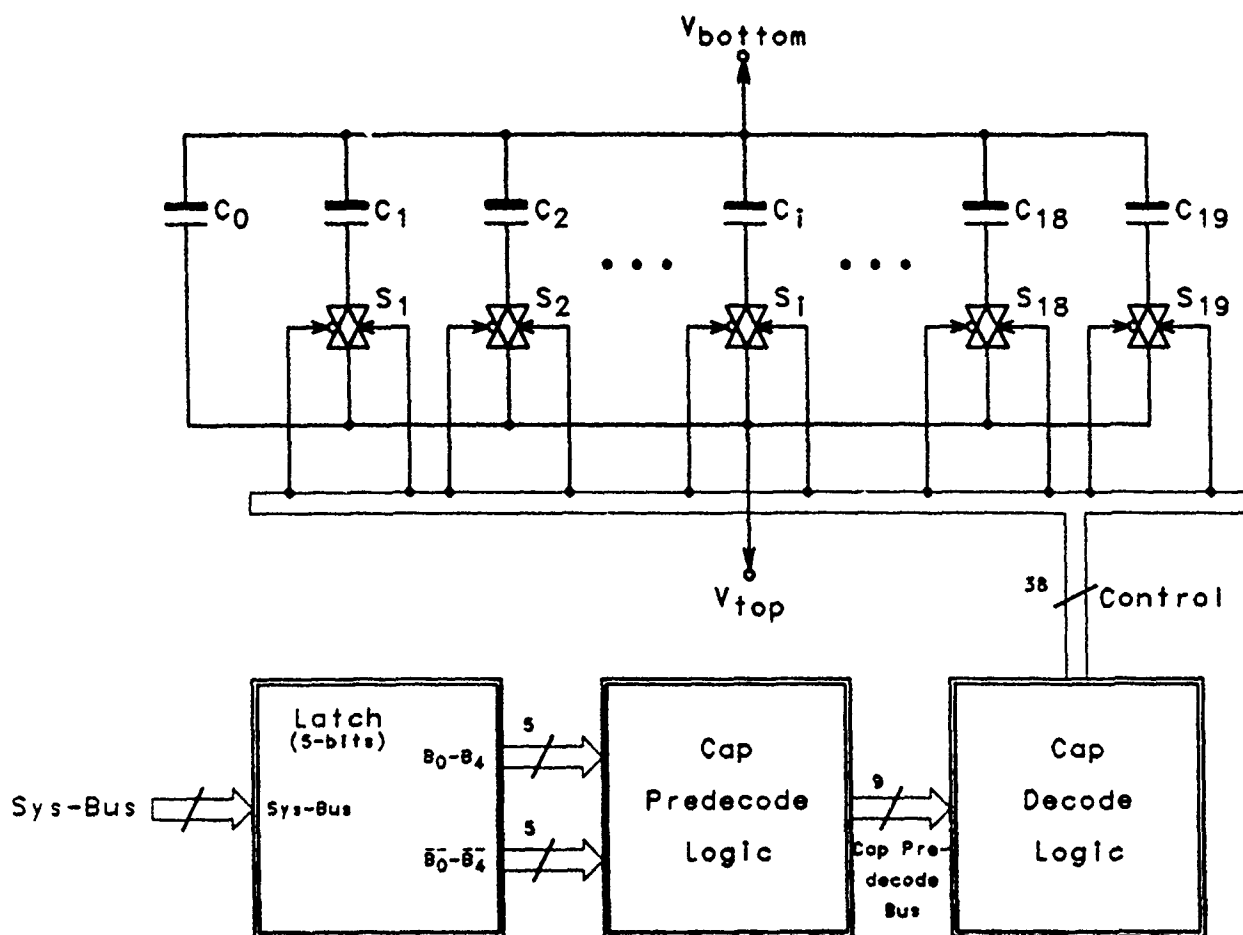


Fig. 5.6-2: Programmable capacitor array block diagram.

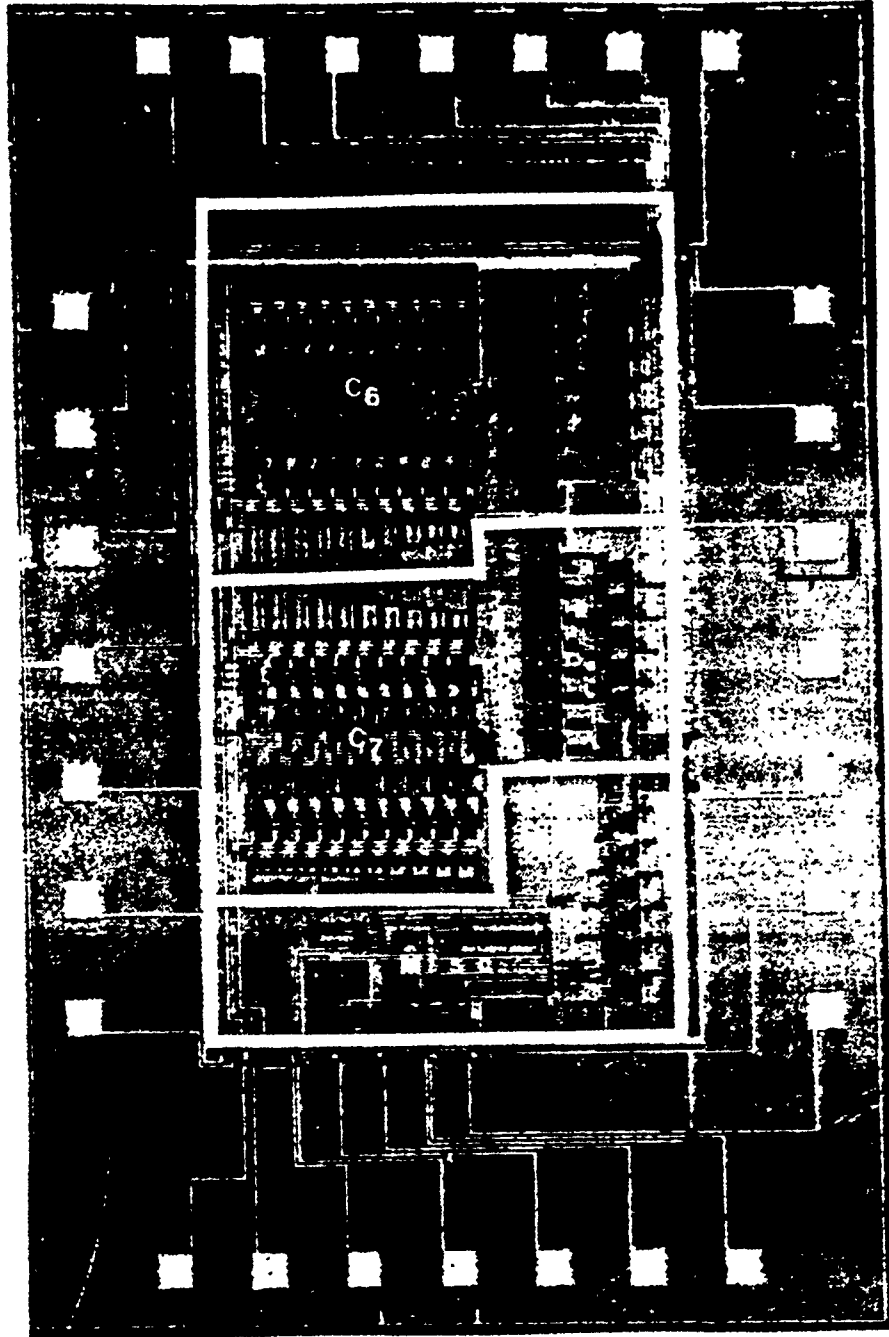


Fig. 5.6-3: Layout of programmable capacitor array test cell.

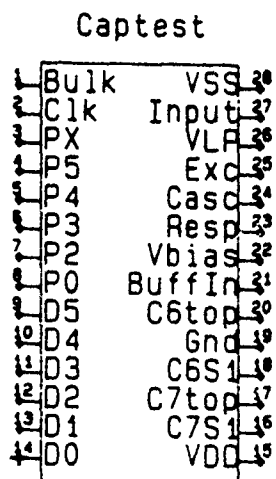


Fig. 5.6-4: Pinouts for programmable capacitor array test cell.

Pin 17: $C7_{top}$	Connection to top plate of $C7$ capacitor array.
Pin 18: $C6_{s1}$	Connection to bottom plate of $C6$ capacitor array via switch B_{BP}
Pin 19: Gnd	Common node.
Pin 20: $C6_{top}$	Connection to top plate of $C6$ capacitor array.
Pin 21: BuffIn	Input to CMOS analog buffer.
Pin 22: V_{bias}	DC bias voltage for CMOS analog buffer.
Pin 23: Resp	Output of CMOS analog buffer via switch B_{RESP} .
Pin 24: Cascade	Output of CMOS analog buffer via switch B_{CASC} .
Pin 25: Exc	Connection to switch B_{EXC} simulating connection from excitation line of analog bus of DCASP.
Pin 26: Input	Connection to switches B_{EXC} and B_{LP} simulating connection from input line of biquad.
Pin 27: V_{LP}	Connection to switches B_{LP} and \bar{B}_{LP} .
Pin 28: V_{SS}	Negative supply.

Table 5.6-1 gives the predecode address line settings necessary to address the capacitor arrays and the 6-bit latch. The capacitor sizes are set by loading the data lines $D0 - D5$ with the desired code 00 thru 13_{16} (see Tables 5.6-2, 3). For the 6-bit latch, the data lines correspond to the analog switch controls as follows:

$D0 - B_{EXC}$
 $D1 - B_{RESP}$
 $D2 - B_{CASC}$
 $D3 - B_{LP}$
 $D4 - B_{BP}$
 $D5 - B_{HP}$

Test Plan:

The Hewlett Packard LF Impedance Analyzer, Model 4192A (see Appendix C for specifications) is used. The capacitance for $C6$ is measured twice; once with each of the two associated analog switches (controlled by B_{bp} and \bar{B}_{bp}) closed.

For the case where $B_{BP} = 1$, the capacitance of $C7$ is measured between the top plate

of the capacitor and the input line V_{in} . This yields the approximate capacitance of the array; the measured value is listed as $C6_{top-bottom}$ in Table 5.6-2 of the following section.

For the case where $\overline{B_{BP}} = 1$, the capacitance is measured between the top plate of the capacitor and the common node of the circuit. In addition to the capacitance of the array, this measurement includes parasitic diffusion capacitances of the 19 analog switches enabling the array, the B_{BP} and $\overline{B_{BP}}$ switches, and the parasitic capacitance of the bonding pad. This measured value is listed as $C6_{top-ground}$ in Table 5.6-2.

The capacitance of $C7$ is measured for the case where $\overline{B_{HP}} = 1$; the measured values are listed as $C7_{top-ground}$ in Table 5.6-2.

Experimental Results:

The measured capacitances are listed in Table 5.6-2. The functionality of the capacitor array is verified by the fact that the incremental changes in capacitance ($\Delta C6_{top-bottom}$) increase monotonically as the digital state goes from $N = 0$ to $N = 19$.

Table 5.6-3 lists the capacitance values calculated from the actual capacitor dimensions data supplied by the IC manufacturer. These calculated values compare favorably with the measured values listed in the $C6_{top-bottom}$ column of Table 5.6-2; the greatest absolute difference is 0.396 pF for the case $N = 19$.

The $\Delta\%$ column of Table 5.6-2 shows that in all cases the incremental change in capacitance is slightly less than the design goal of 13% (see Section 2.1.4). The incremental changes obtained are satisfactory; the resulting overlap in the coarse frequency and bandwidth adjustment ranges will simply be slightly more than was intended. Also note that the range of capacitor values (2.441pF - 21.26pF) is slightly less than the design goal (2.34pF - 24.37pF). Such deviations are to be expected due to the IC process variations. The capacitor values (2.068pF-10.864pF) listed in Table 5.6-3 were obtained by calculation using the measured capacitance/area ratio ($.391fF/\mu m^2$) given by MOSIS for this particular IC fabrication run.

The $C6_{top-gnd}$ column of Table 5.6-2 reveals that this measured capacitance differs significantly from the $C6_{top-bottom}$ values. The measured differences range from 2.60pF to 2.97pF. This indicates that the parasitic capacitances from the top plate of the capacitor array to the common node of the circuit are significant. These parasitics are due to the diffusions at the analog switches of the capacitor array. See Section 2.1.4 for a further explanation of these parasitics.

Element	\overline{CLK}	Predecode Address Lines					
		PX	$P5$	$P4$	$P3$	$P2$	$P0$
C6	1	1	1	0	0	1	0
C7	1	1	1	0	1	0	0
6-bit Latch	1	1	0	1	0	0	1

Table 5.6–1: Addressing of capacitor arrays and 6-bit latch of programmable capacitor array test cell.

N	Digital Input (hex)	$C_{6_{top-bot}}$ (pF)	$\Delta C_{6_{top-bot}}^1$ (pF)	$\Delta\%^2$	$C_{6_{top-gnd}}$ (pF)	$C_{7_{top-gnd}}$ (pF)
0	00	2.441	—	—	5.072	3.155
1	01	2.706	.265	10.9	5.335	3.403
2	02	3.012	.306	11.3	5.982	4.056
3	03	3.360	.348	11.6	—	—
4	04	3.750	.390	11.6	—	—
5	05	4.182	.432	11.5	—	—
6	06	4.676	.494	11.8	—	—
7	07	5.234	.558	11.9	7.849	5.920
8	08	5.852	.618	11.8	—	—
9	09	6.558	.706	12.1	—	—
10	0A	7.345	.787	12.0	—	—
11	0B	8.235	.890	12.1	—	—
12	0C	9.251	1.016	12.3	—	—
13	0D	10.396	1.145	12.4	—	—
14	0E	11.709	1.313	12.6	—	—
15	0F	13.188	1.479	12.6	15.810	13.810
16	10	14.855	1.667	12.6	—	15.360
17	11	16.745	1.890	12.7	—	17.255
18	12	18.865	2.120	12.7	—	—
19	13	21.26	2.395	12.7	23.86	21.77

Table 5.6-2: Measured capacitances of programmable capacitor arrays C_6 and C_7 .

$$^1\Delta C_{6_{top-bot}_N} = C_{6_{top-bot}_N} - C_{6_{top-bot}_{N-1}}$$

$$^2\Delta\% = \frac{\Delta C_{6_{top-bot}_N}}{C_{6_{top-bot}_{N-1}}}$$

N	Hex	Capacitor Dimensions ($\mu m \times \mu m$)	Capacitor Area (μm^2)	Calculated Capacitance (pF)
0	00	115 \times 46	5.290	2.068
1	01	13 \times 53	5.979	2.338
2	02	15 \times 53	6.774	2.649
3	03	17 \times 53	7.675	3.001
4	04	19 \times 53	8.682	3.395
5	05	21 \times 53	9.795	3.820
6	06	24 \times 53	11.067	4.327
7	07	27 \times 53	12.498	4.887
8	08	30 \times 53	14.088	5.508
9	09	34 \times 53	15.890	6.213
10	0A	38 \times 53	17.904	7.001
11	0B	43 \times 53	20.183	7.892
12	0C	49 \times 53	22.780	8.907
13	0D	55 \times 53	25.695	10.047
14	0E	63 \times 53	29.034	11.352
15	0F	71 \times 53	32.797	12.824
16	10	80 \times 53	37.037	14.482
17	11	91 \times 53	41.860	16.367
18	12	102 \times 53	47.266	18.481
19	13	115 \times 53	53.361	20.864

Table 5.6-3: Calculated capacitance of programmable capacitor array.

$$\text{Capacitance/area} = .391 \text{ fF}/\mu m^2.$$

Note that some of the parasitics included in the measurements of $C_{6_{top-gnd}}$ will not appear in the actual DCASP operation. For example, in the actual DCASP circuit, the top plate of the capacitor array is not connected to a bonding pad; thus, in the actual DCASP circuit, there is no parasitic capacitance between a bonding pad and the common node. The protoboard and probes used in the test circuit also contribute a small parasitic capacitance.

The capacitance for several of the $C7$ array states was also measured for the case where $\overline{B_{HP}} = 1$; the measured values are listed in the $C_{7_{top-gnd}}$ column of Table 5.6-2. These values are approximately 2pF less than the corresponding $C_{6_{top-gnd}}$ values. This difference may be attributed to the proximity of the respective pinouts of the IC. The $C_{6_{top}}$ pin (pin 20) is adjacent to the ground pin (pin 19), and therefore the parasitic protoboard capacitance between these two pins will be higher than that between the $C_{7_{top}}$ pin (pin 17) and the ground pin.

In summary, the functionality of the capacitor array has been verified. The measured values of capacitance are approximately equal to the design values. The only possible problem is that of parasitic capacitances which contribute to the total capacitance when the bottom plate of the capacitor array is connected to ground.

5.7 DCASP-1 digital support logic test cell

Name:	Digital Test
MOSIS ID:	22118
Fab. ID:	M6BYAB-1
Technology:	CBPE — MOSIS $3\mu m$ CMOS double-poly p-well process
Fabricated:	December 1986 – January 1987
Chip Size:	$2300\mu m \times 3400\mu m$ ($7.82mm^2$)
Number of Pads:	25
Packaging:	28 pin package
Status:	Tested.

Purpose:

This test chip was designed to verify the digital logic used to control DCASP-1 (MOSIS ID: 22143). This chip contains most of the digital support logic that interfaces DCASP-1 with the external digital controller and stores the digital control words used to configure the filters in DCASP-1. This test vehicle will only be used to characterize each of the individual digital blocks, verify their functionality, and verify input trip-points and output signal levels. Speed of operation is not a consideration with this test structure.

Description:

This test chip with pin-outs shown in Fig. 5.7-1, contains the following digital support logic:

- (1) Address Predecode Logic (AP_{decode}) — This logic block, as shown in Fig. 5.7-2, takes 3 pair of externally provided address lines, and converts them (a) from the external TTL logic levels to the internal $\pm 5V$ logic levels; and (b) generates 3 quadruple predecode addresses for a total of 12 lines and commonly referred to as the predecode address bus. This bus is then supplied to each of the internal latches (ADL_{latch}). This functional block is described in Section 2.5. Contained here is just one such sub-block, with 2 input address lines (A_i and A_k) and four predecode addresses (P_a , P_b , P_c and P_d). This cell also requires the chip select line (CS) to be enabled, before the predecode address bus will be enabled, as shown in Table. 5.7-1.

Also included on this test chip is the fundamental address predecode cell, a three input AND gate AP_{nand3i} as shown in Fig. 5.7-3. The overall Address Predecoder contains twelve of these gates — one for each output predecoded address. The input to this cell is provided via the shared input pads, In_1 , In_2 and In_3 , with a single output pin Out . Each of these input/output signals are at $\pm 5V$ CMOS logic levels.

- (2) TTL interface drivers (TTL_{in}/TTL_{out}) — There are two functional logic blocks as shown in Fig. 5.7-4a and 5.7-4b that convert between the external TTL digital logic levels and the internal $\pm 5V$ CMOS logic levels.

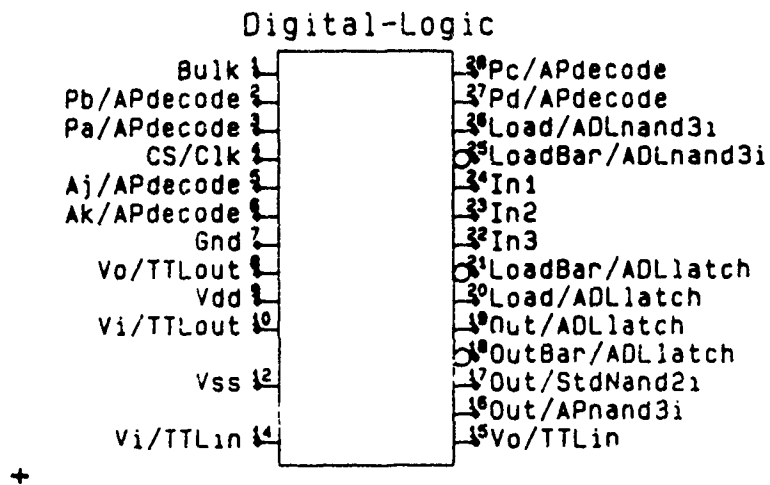


Fig. 5.7-1. Digital support logic test chip pin-outs.

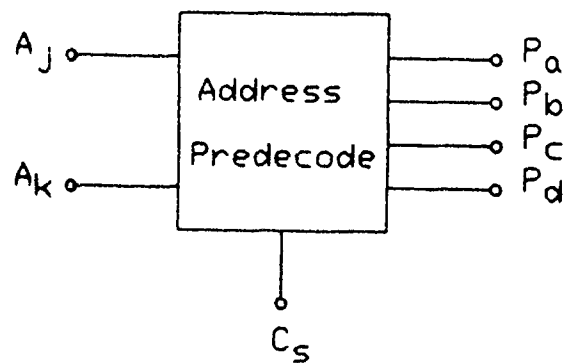


Fig. 5.7-2. Address predecode (AP_{decode}) block diagram.

Table 5.7-1. Address predecode logic description.

CS	A_k	A_j	P_a	P_b	P_c	P_d
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	X	X	0	0	0	0

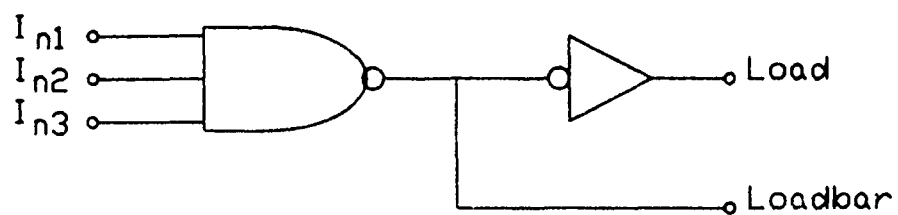
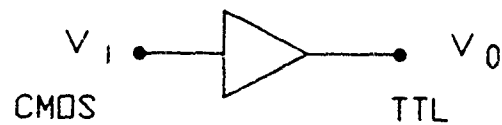
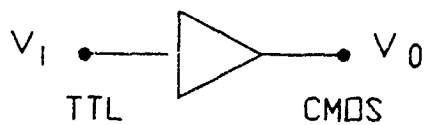


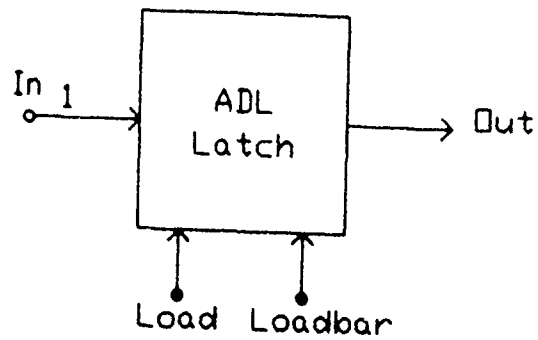
Fig. 5.7-3. Address predecode (AP_{nand3i}) circuit schematics.



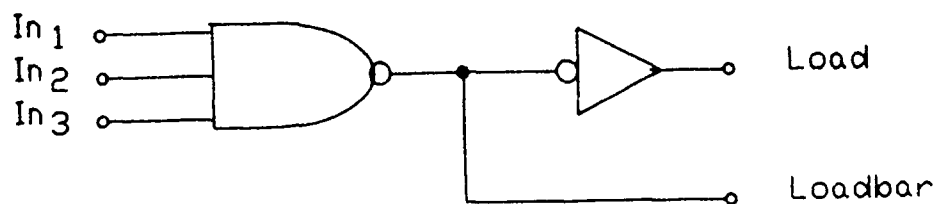
(a) *TTLin*

(b) *TTLout*

Fig. 5.7-4. TTL level shifters block diagrams.



(a) *ADLnand3i*



(b) *ADLlatch*

Fig. 5.7-5. Address Decode and Latch circuit schematics.

- (a) TTL input driver (*TTLin*) — This gate takes a 0-5V TTL input signal ($V_i/TTLin$) and converts it to the internal CMOS levels ($V_o/TTLin$).
- (b) TTL output driver (*TTLout*) — This gate takes a $\pm 5V$ CMOS input signal $V_i/TTLout$ and converts it to a TTL 0-5V logic levels, $V_o/TTLout$.
- (3) Address Decode and Latch (*ADLnand3i, ADLlatch*) — This logic block decodes the address as a function of three predecode address lines, and latches the data found on the data bus in the latch. This test vehicle contains the address decode logic (*ADLnand3i* with inputs I_{n1} , I_{n2} and I_{n3} , and outputs *Load* and *LoadBar*, as shown in Fig. 5.7-5a. Also contained on this chip is the latch (*ADLlatch*) as shown in Fig. 5.7-5b. This block is controlled by the complementary latch control inputs *Load* and *LoadBar*, normally provided by the *ADLnand3i* gate; input data line I_{n1} and latched complimentary output data lines *Out* and *OutBar*. Each of these input/output signals are at $\pm 5V$ CMOS logic levels.
- (4) Standard 2-input AND gate (*stdnand2i*) — This logic gate as shown in Fig. 5.7-6 is used in various portions of the DCASP-1 chip, typically as a predecode of the digital control words. This cell has two inputs I_{n1} and I_{n2} and a single output *Out*. Each of these input/output signals are at $\pm 5V$ CMOS logic levels.

Test Plan:

Functional Test:

Each of the digital gates will be verified based upon the following criterion:

- (1) Each of the gates agrees logically with the aforementioned description, (i.e., logic truth-table, state diagrams, etc.).
- (2) The input signals' trip-points meet specifications.
- (3) The output signals are at the expected signal levels.

If a particular support logic function does not perform as anticipated, then more detailed testing should be done to trace down any discrepancies.

Experimental Results:

A functional test was performed on each of the digital blocks, and each of them functioned as expected, and well within specifications. The following discuss the specific results reported for each of the functional cells.

(1) Address Predecode Logic (*APdecode*)

- (a) The predecode address lines (outputs) swings rail to rail ($\pm 5V$), as expected.

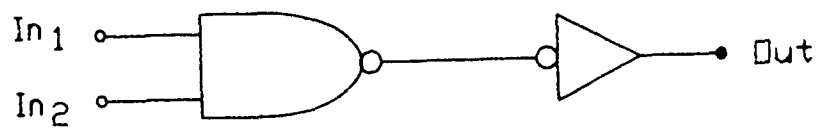


Fig. 5.7-6. Standard 2-input AND gate (*stdnand2i*) circuit schematic.

- (b) Clock frequencies in excess of $5 - 10\text{MHz}$ are no problem.
- (c) TTL inputs trip at a signal level of approximately $+2\text{V}$, as expected.
- (d) Rise times are much faster than fall times. At high clock rates, the output of the Address Predecode Logic and associated ADL decode logic must be stable before the data is latched on the falling edge of the clock signal. This restricts the clock frequencies to less than 50MHz or so.

(2) TTL interface drivers (TTL_{in}/TTL_{out})

- (a) The TTL input driver tripped at approximately 2.4V and output was $\pm 5\text{V}$, as anticipated.
- (b) The TTL output driver tripped at -0.2V and outputs were between 0 and 5V .
- (c) Both drivers could easily handle up to 5MHz .
- (d) The TTL input driver (TTL_{in}), had a rise time of $1 - 3\text{ns}$ and a fall time of $10 - 15\text{ns}$. This difference can be accounted for by the large parasitic diffusion capacitance associated with the output of the input inverter and the imbalance in drive capability between the pull-up transistor and the pull-down transistor of this stage. The experimental results shown here, agree with that predicted by SPICE and logic simulations.

(3) Address Decode and Latch ($ADL_{nand3i}, ADL_{latch}$)

At low-frequencies, the precharge nature of this design, shows the address trip level at approximately -3.5 to -3.8V ; but at 1MHz the trip level is up to -2V and no longer a problem. Thus it is concluded that as long as the clock frequency is not lowered by 3-4 order magnitudes below typical clock frequencies, there is no problem.

(4) Standard 2-input AND gate ($stdnand2i$)

Functioned as expected.

5.8 Modified OTA with 2 Selectable Output Stages

MOSIS ID: 22846
Fab. ID: M721AB-2
Technology: CBPE-MOSIS 3μ CMOS double-poly p-well process
Fabricated: March-April 1987
Chip Size: $2300\mu \times 3400\mu$ ($7.82mm^2$)
Active Area: $191\mu \times 784\mu$ ($.150mm^2$)
Number of Pads: 9
Packaging: 28 pin package
Status: Tested

Purpose:

This test chip is used to verify that the design modifications to the OTA of DCASP-1 do indeed result in an OTA with a functional coarse g_m adjustment capability. Recall from Section 5.3 that for the OTA of DCASP-1, the disabling of the larger output gain stage rendered the smaller output gain stage useless for practical input signal amplitude levels.

Description:

Fig. 5.8-1 shows the circuit schematic. Device sizing is presented in Table 5.8-1. Of special interest is the method of biasing the two output stages. In the OTA circuit of DCASP-1 (Fig. 5.3-1), problems arose because the current mirror output stages were biased by connecting the drain and gate of $M26$ and of $M32$. As seen in Fig. 5.8-1, those connections have been replaced by connections between the gate and drain of $M24$ and between the gate and drain of $M31$. In this way, the gate voltages for the transistors in the output stages are not affected by the current in these stages, as was the case in the OTA of DCASP-1.

Another modification is that the pass transistors used to disable the output stages in the OTA of DCASP-1 have been eliminated. In the modified circuit of Fig. 5.8-9, a stage is disabled by shunting signal current to the positive and negative supplies via transistors $M36$, $M39$ or $M37$, $M38$.

The layout of the test chip is shown in Fig. 5.8-2 (Note: The DAC and latch contained on this test chip are described in Sec. 5.). A diagram showing the pinouts on the IC is given in Fig. 5.8-3. Following is a description of each pin:

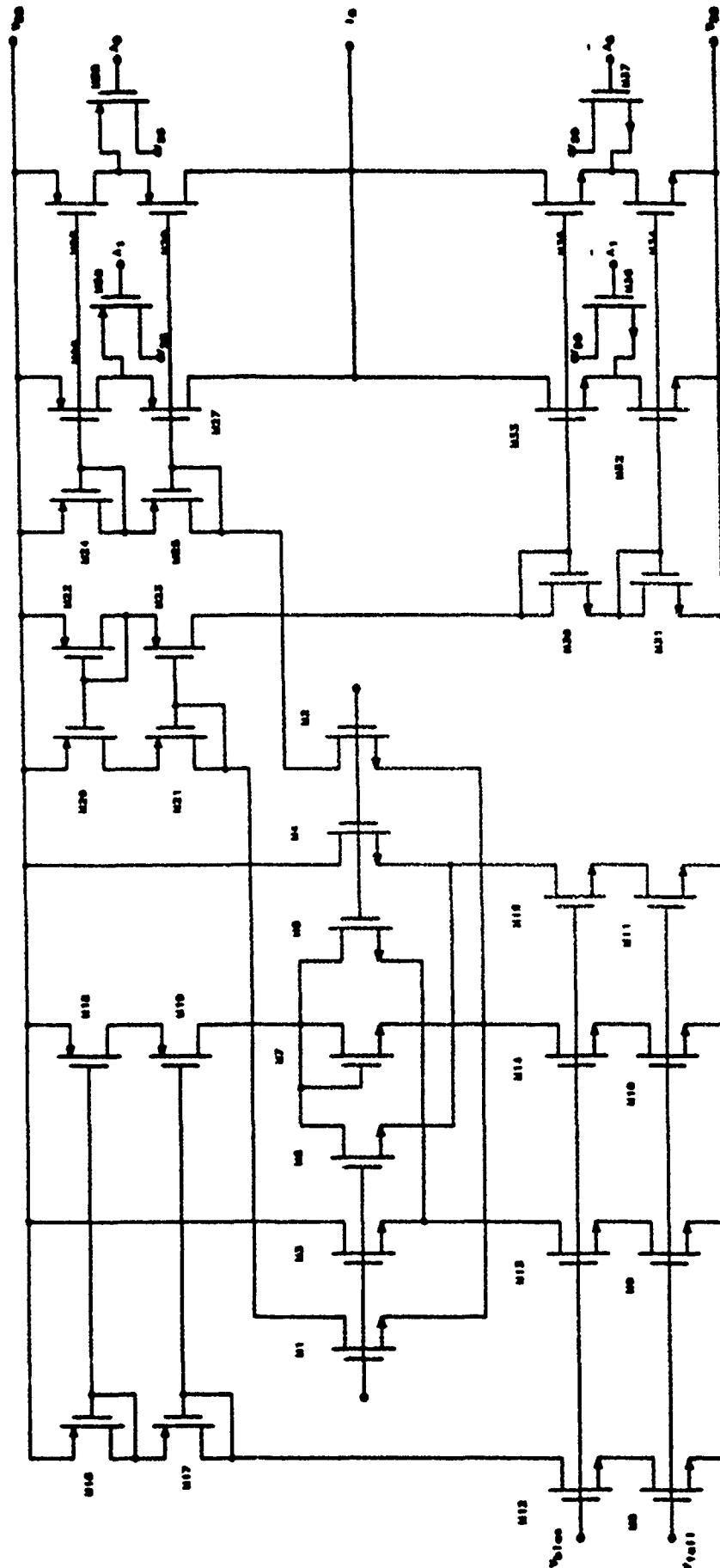


Fig. 5.8-1: Circuit schematic for modified 2-output stage OTA.

DEVICE	SIZE (microns)	
	W	L
M1-M2	8	5
M3-M4	16	5
M5-M6	8	5
M7	7	5
M8, M12	40	3
M9-M11, M13-M15	80	3
M16-M17	60	3
M18-M21	120	3
M22-M23	60	3
M24-M25	120	3
M26-M27, M32-M33	60	3
M28-M24, M34-M35	6	3
M30-M31	60	3
M36-M38	20	3
M37-M39	7	3

Table 5.8-1: Device Sizing for OTA Structure of Figure 5.8-1.

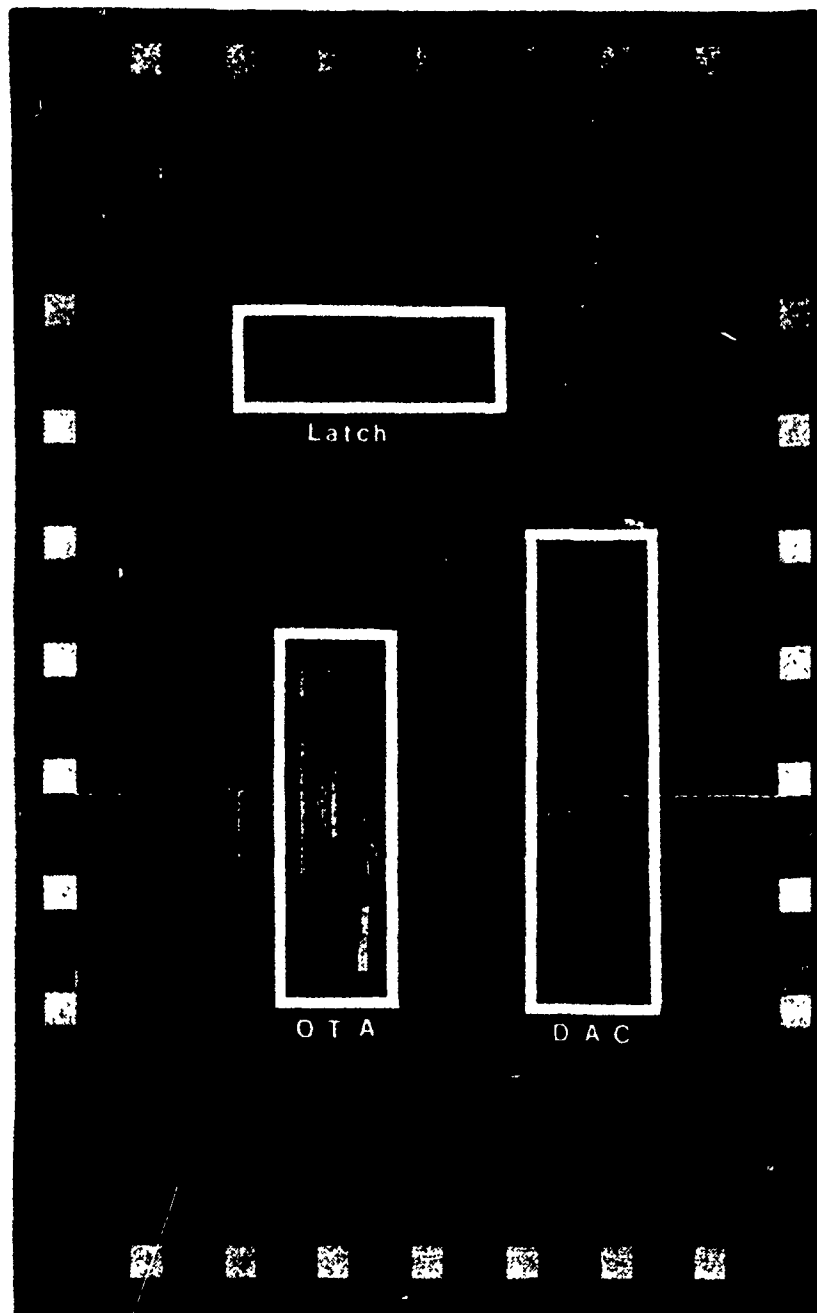
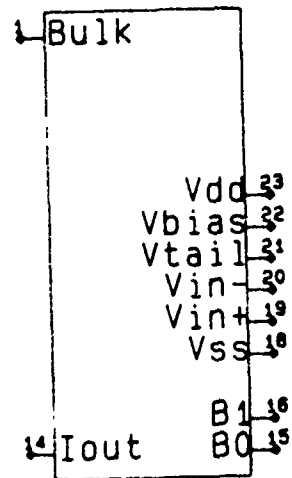


Fig. 5.8-2: Layout of modified 2-output stage of OTA test cell.

OTA-DAC-test



+

Fig. 5.8-3: Pinouts for modified 2-output stage OTA test cell.

Pin 1: Bulk	Connection to the n^+ substrate of the chip
Pin 14: I_{out}	OT' output current.
Pin 15: B_0	Digital control for the smaller of the two OTA output stages. The stage is enabled for $B_0 = 1$.
Pin 16: B_1	Digital control for the larger of the two OTA output stages. The stage is enabled for $B_1 = 1$.
Pin 18: V_{SS}	Negative supply for the OTA.
Pin 19: V_{in}^+	Positive input terminal of the OTA.
Pin 20: V_{in}^-	Negative input terminal of the OTA.
Pin 21: V_{tail}	DC input voltage used to adjust the g_m of the OTA by adjusting the tail current in the cascoded structures of the OTA input stage.
Pin 22: V_{bias}	DC input voltage used to bias the currents in the cascoded structure of the OTA input stage.
Pin 23: V_{DD}	Positive input terminal of the OTA.

Test Plan:

The circuit of Fig. 5.8-3 is used to determine whether output signal amplitudes greater than $3V_{p-p}$ can be obtained without excessive distortion. This is done for both the case where only the larger stage is enabled and the case where only the smaller stage is enabled in order to ensure that the problem discussed in Section 5-3 does not exist in the modified OTA.

This modified OTA is itself superseded by the 6-output stage OTA discussed in Section 5.11. For this reason, this modified 2-output stage OTA was not extensively tested. The modified 2-output stage OTA is not found in either of the two DCASP implementations.

Experimental Results

It was verified experimentally that for the circuit of Fig. 5.3-4 output signal amplitudes greater than $3V_{p-p}$ can be obtained with either of the two output stages enabled. This verified that the problem with the original OTA of DCASP-1 had indeed been eliminated.

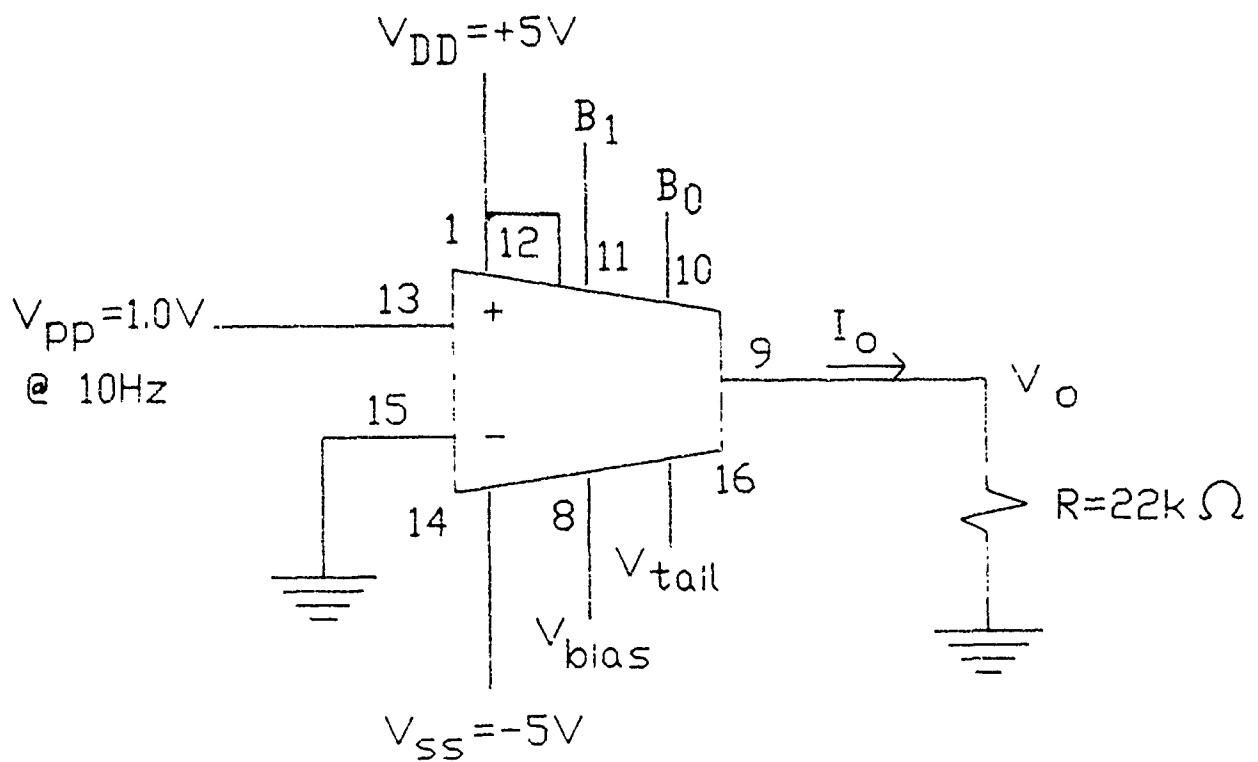


Fig. 5.8-4: Circuit used to test the modified 2-output stage OTA.

5.9 6-Bit Linear DAC with Switching Tree

MOSIS ID: 22846
Fab. ID: M72QAB-2
Technology: CBPE-MOSIS 3μ CMOS Double-Ply p-Well
Fabricated: March-April 1987
Chip Size: $2300\mu \times 3400\mu (7.82mm^2)$
Active Area: $200\mu \times 1150\mu$
Number of Pads: 14
Packaging: 28 Pin Package
Status: Tested

Purpose:

This test chip (Small DAC) is used to characterize both the monotonicity and linearity of the Digital-to-Analog Converter (DAC) circuit using a switching transistor tree. The chip is the second fabrication of the "small linear DAC". The first small DAC, described in Sec. 5.5, was not functional due to the fabrication error.

Description:

As shown in Fig. 5.9-1, two independent blocks have been fabricated in the Small DAC, an OTA and a small DAC. In this section, however, only the small DAC circuits are described and tested. The small DAC structure is based on a resistive polysilicon string with taps and pass transistors at uniformly spaced intervals. The operation principles are thus similar to the "Large DAC", except that the small DAC uses a pyramidal switching array to decode the data instead of using the standard decoders. (See Fig. 5.9-2 and Fig. 5.9-3 for the block diagram and circuit schematic.)

Test Plans:

The pin designations of the small DAC are shown in Fig. DAC2-1. The biasing voltages and triggering signals are connected as follows:

$$V_{DD} = \text{Bulk} = +5V \quad (5.9-1)$$

$$V_{SS} = (\text{p-well}) = -5V \quad (5.9-2)$$

$$A_i = +5V \text{ (Enabling)} \quad (5.9-3)$$

$$\overline{CLK} = \pm 5V, 1000Hz \quad (5.9-4)$$

$$V_{ref+1} = 0V \quad (5.9 - 5)$$

$$V_{ref-} = -5V \quad (5.9 - 6)$$

64 DC voltages have been measured from V_{out} pin by changing the 6-bit data word (D0-D5) to all possible combinations. The instrument used for DC measurements is the HP 3456A Digital Voltmeter which has been extensively used throughout this experiment.

Experimental Results:

The 64 DC voltages measured on the V_{out} pin are listed in Table 5.9-1. The LSB error and $\frac{R_n}{R_{total}}$ both characterize the linearity of the DAC and can be defined as follows:

$$LSB_{error}[n] \triangleq \left| \frac{V_{out}[n] - \left[n \cdot \left(\frac{V_{out}[63] - V_{out}[0]}{63} \right) + V_{out}[0] \right]}{\left(\frac{V_{out}[63] - V_{out}[0]}{63} \right)} \right| \times 100\% \quad n = 0, \dots, 63 \quad (5.9 - 7)$$

and

$$\frac{R_n}{R_{total}} \triangleq \frac{V_{out}[n] - V_{out}[n-1]}{V_{ref+} - V_{ref-}} \times 100\% \quad n = 0, 1, \dots, 64 \quad (5.9 - 8)$$

where $V_{out}[-1] = V_{ref-}$ and $V_{out}[64] = V_{ref+}$ and R_o and R_{64} are the parasitic resistors at two biasing end. Fig. 5.9-1 shows that the small DAC performs somewhat better than the large DAC in Section 5.5 in the sense that the maximum LSB error is as low as 6.3%. This fact also implies that the 6-bit small DAC may be improved with much higher resolutions. However, at digital setting zero, a very significant offset voltage was measured. This output voltage of zero setting is expected to be much closer to V_{ref-} .

Table 5.9-1 The DC Output Voltages and the Linearity Characteristics with Different Digital Settings

Digital	Output	LSB_{error}	$\frac{R_N}{R_{total}}$	$\frac{R_N}{R_{N-1}}$
0	-4.476500	0.000000	10.469999	
1	-4.406100	0.175119	1.408005	0.13148
2	-4.335500	0.066937	1.412001	1.002838
3	-4.265200	0.384722	1.405993	0.995745
4	-4.194600	0.276540	1.412001	1.004273
5	-4.124000	0.168358	1.412001	1.000000
6	-4.053600	0.343477	1.408005	0.997170
7	-3.983000	0.235634	1.411996	1.002835
8	-3.912600	0.411091	1.408000	0.997170
9	-3.842100	0.444560	1.410003	1.001422
10	-3.771900	0.903656	1.403999	0.995742
11	-3.701000	0.370185	1.417999	1.009971
12	-3.630300	0.120352	1.413999	0.997179
13	-3.559800	0.153821	1.410003	0.997174
14	-3.489200	0.045977	1.411996	1.001414
15	-3.418600	0.062205	1.412001	1.000003
16	-3.348200	0.113253	1.408000	0.997167
17	-3.277400	0.278568	1.416001	1.005683
18	-3.206900	0.245099	1.410003	0.995764
19	-3.136300	0.352943	1.411996	1.001414
20	-3.065700	0.461125	1.412001	1.000003
21	-2.995400	0.144017	1.406002	0.995752
22	-2.924500	0.677487	1.417999	1.008533
23	-2.854100	0.502031	1.408000	0.992948
24	-2.783500	0.610213	1.412001	1.002841
25	-2.712900	0.718395	1.412001	1.000000
26	-2.642500	0.542938	1.408000	0.997167
27	-2.571600	1.076409	1.417999	1.007102
28	-2.501200	0.900952	1.408000	0.992948
29	-2.430500	1.150784	1.413999	1.004260
30	-2.359900	1.258966	1.412001	0.998587
31	-2.289400	1.225159	1.409998	0.998582
32	-2.218700	1.475330	1.414003	1.002841

Digital	Output	LSB_{error}	$\frac{R_N}{R_{total}}$	$\frac{R_N}{R_{N-1}}$
33	-2.148100	1.583511	1.412001	0.998584
34	-2.077100	2.258634	1.419997	1.005663
35	-2.006600	2.225165	1.410003	0.992962
36	-1.936000	2.333009	1.411998	1.001415
37	-1.865100	2.866311	1.417999	1.004250
38	-1.794500	2.974324	1.412001	0.995770
39	-1.723700	3.365807	1.415999	1.002832
40	-1.653000	3.615639	1.414001	0.998589
41	-1.582600	3.440013	1.408000	0.995756
42	-1.511800	3.831496	1.415999	1.005681
43	-1.439600	6.208284	1.444001	1.019776
44	-1.369000	6.316297	1.412001	0.977839
45	-1.299300	5.148102	1.394000	0.987252
46	-1.228400	5.681405	1.417999	1.017216
47	-1.157900	5.647598	1.410000	0.994359
48	-1.087600	5.330152	1.406000	0.997163
49	-1.017000	5.438165	1.412001	1.004268
50	-0.946600	5.262538	1.407999	0.997166
51	-0.876300	4.945261	1.406001	0.998581
52	-0.805900	4.769720	1.408000	1.001422
53	-0.735600	4.452358	1.406000	0.998579
54	-0.665800	3.426068	1.396000	0.992888
55	-0.595500	3.108706	1.406000	1.007163
56	-0.525200	2.791345	1.406000	1.000000
57	-0.455000	2.332206	1.404000	0.998578
58	-0.384900	1.731290	1.402000	0.998576
59	-0.314500	1.555748	1.408000	1.004279
60	-0.243900	1.663782	1.412000	1.002841
61	-0.173900	0.921046	1.400000	0.991502
62	-0.103700	0.461886	1.404000	1.002857
63	-0.033500	0.002726	1.404000	1.000000
64	-	-	0.0067	-

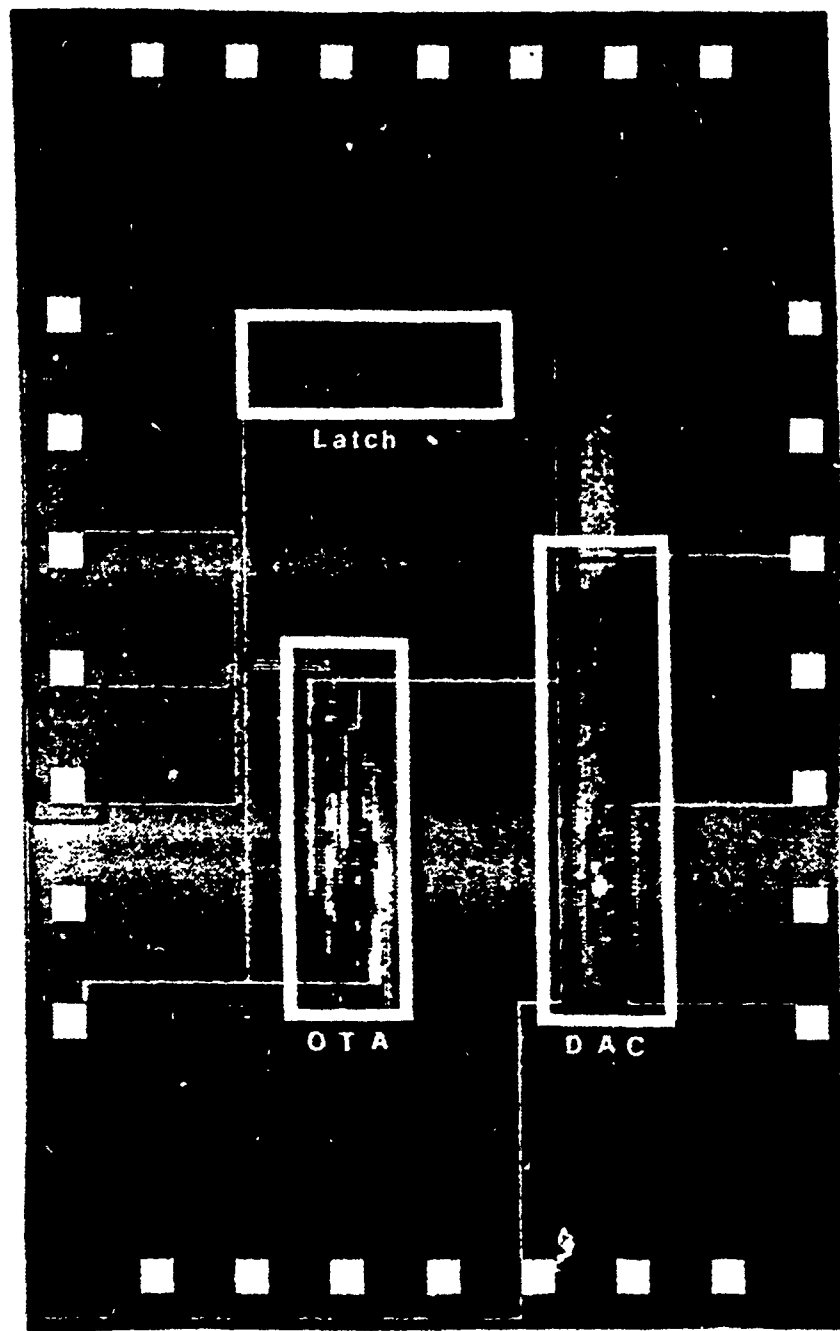


Fig. 5.9-1: The die photo of the small linear DAC test chip.

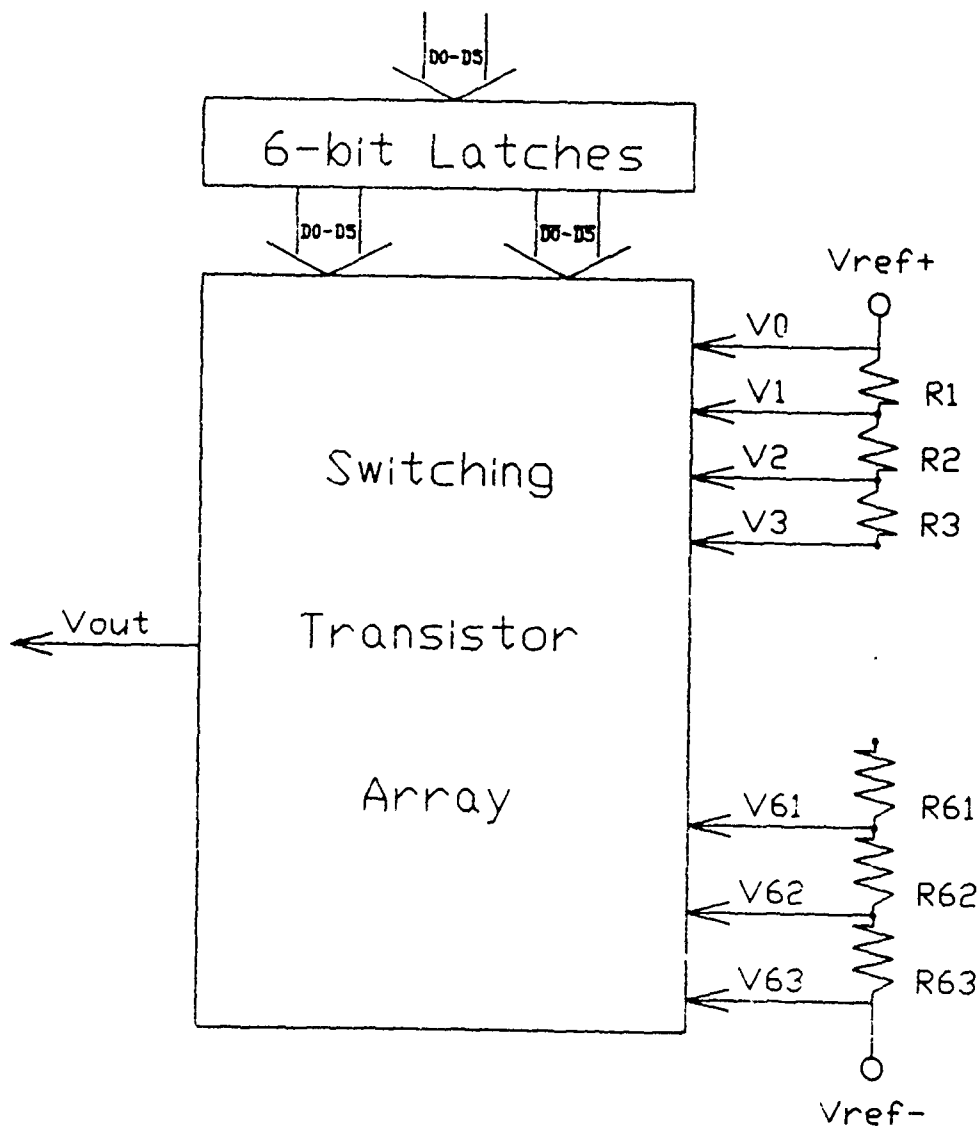


Fig. 5.9-2: Block diagram of the small DAC.

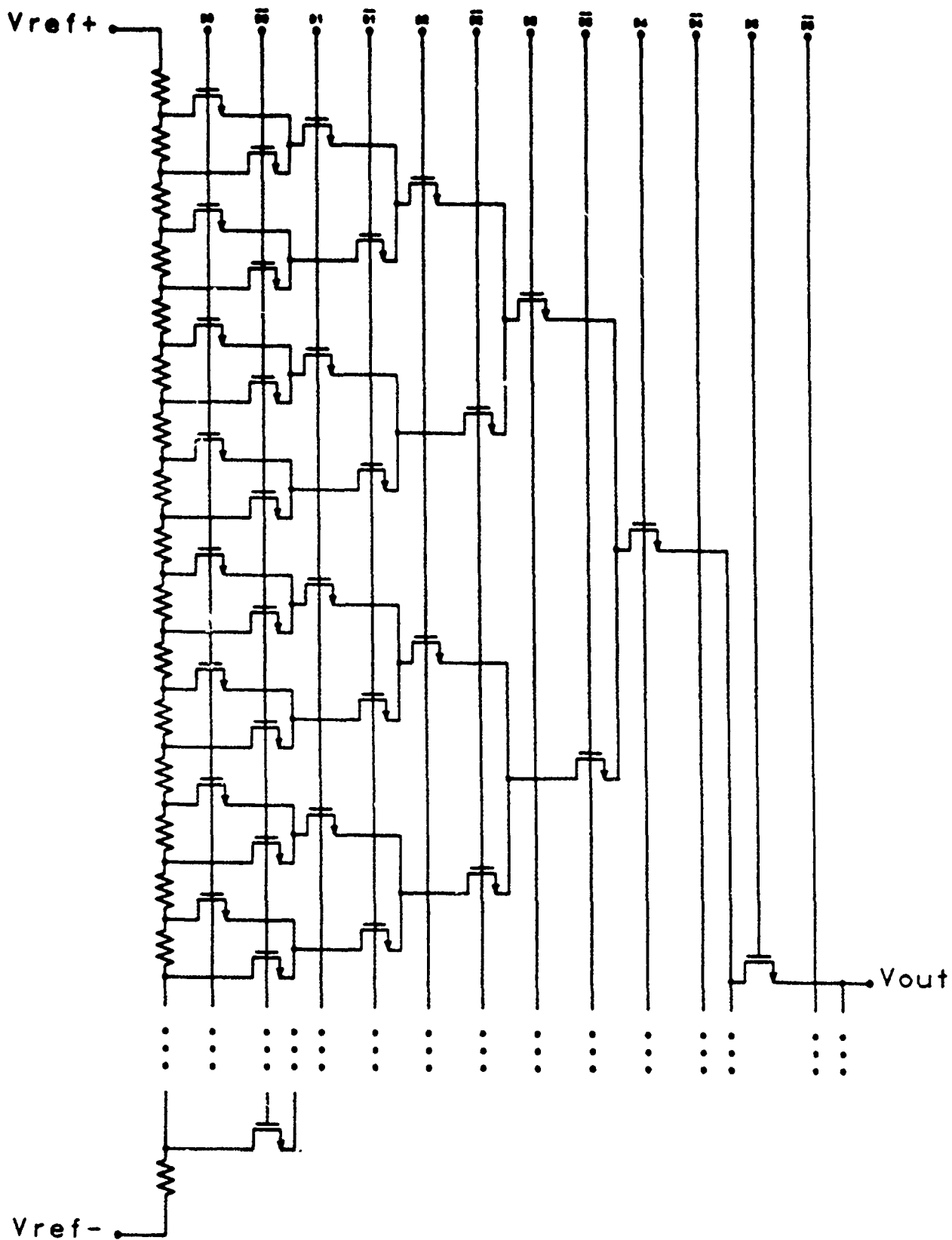


Fig. 5.9-3: The circuit schematic of the small linear DAC.

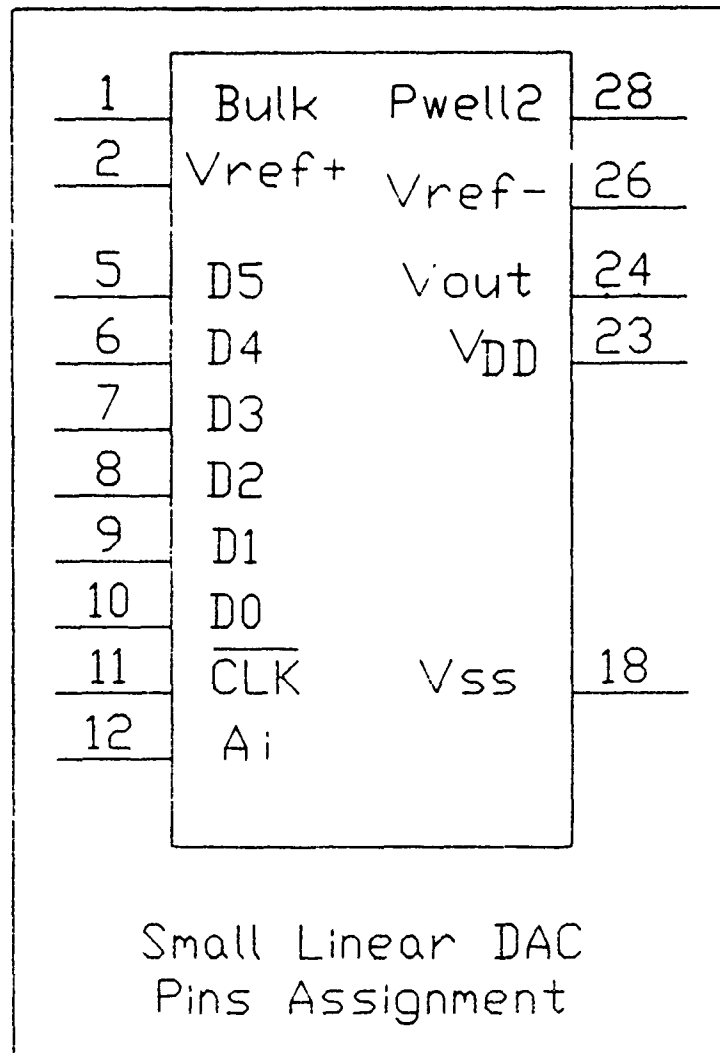


Fig. 5.9-4: Small linear DAC pins assignment.

DAC Performance Analysis of the Small DAC used in DCASP-2

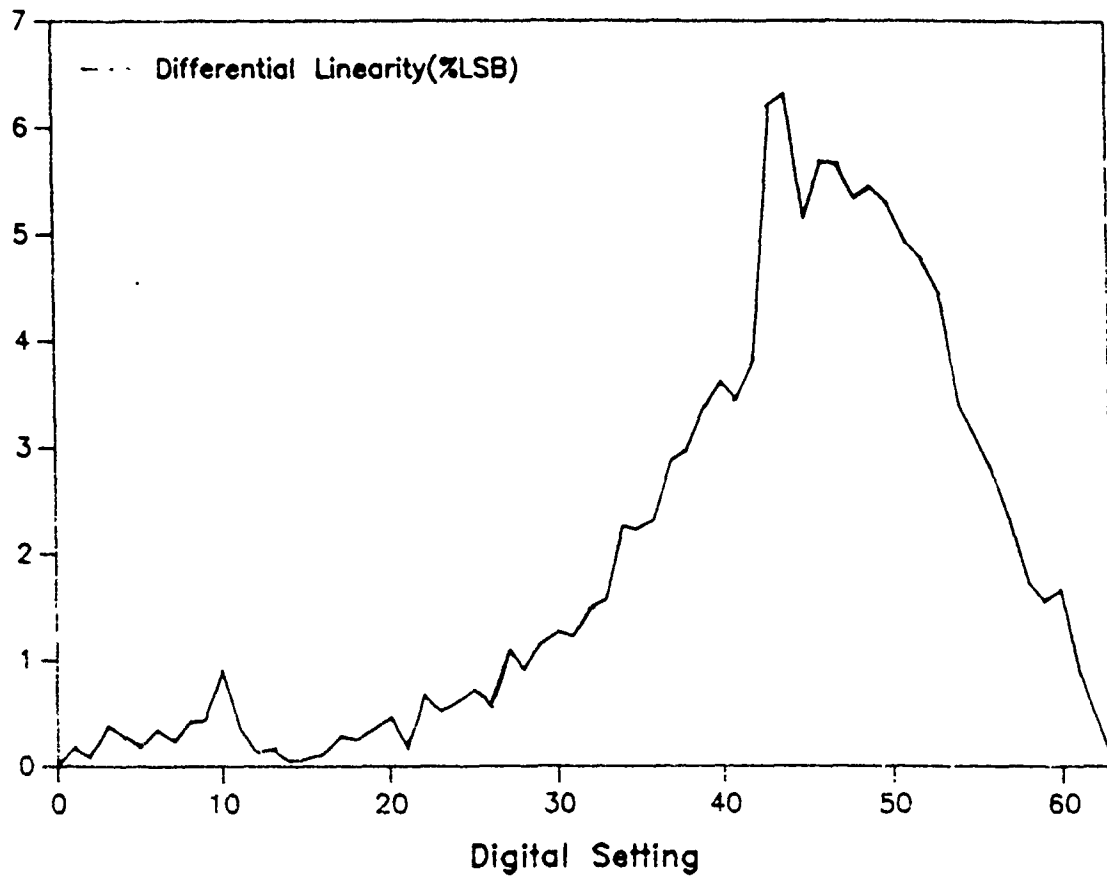


Fig. 5.9-5: DAC performance analysis of the small linear DAC.

5.10 DCASP-2 6th Filter Block

Test Chip:	DCASP-2 6 th -Order General Purpose Filter Block
Technology:	CBPE 3 μ CMOS double-poly p-well process
Fabricated:	July-August 1987
Chip Size:	7900 μ \times 9200 μ
Active Area:	5700 μ \times 7300 μ
Number of Pads:	29
Packaging:	64-pin package
MOSIS ID:	23496

Purpose:

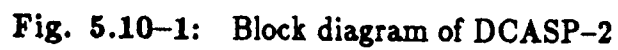
This test chip is the realization of a newer Controlled Signal Processor (CSP) in which the modified OTA and Logarithmic DAC building blocks are used to obtain increased adjustment range and improved resolution. Several experiments have been conducted to evaluate the performance. These are summarized below.

1. Functional Testings of biquads for different configurations, including Low-Pass, High-Pass, Band-Pass, and High-Pass Notch Filters, etc., and the cascaded configurations.
2. Validating the adjustability of capacitor arrays and OTA transconductances.
3. Finding the tuning range of f_o 's, $B\bar{W}$'s and Q 's for Bandpass configuration.
4. Measuring the tuning resolution of f_o , $B\bar{W}$, and Q for the Bandpass configuration.

Extensive tests on adjustment range, resolution, linearity and noise characteristics will be completed in the near future.

Description:

The block diagram of the DCASP test-chip is shown in Figure 5.10-1. A die photograph is shown in Fig. 5.10-2. As its predecessor DCASP-1, the chip contains 3 cascadable biquads and a Performance Detector; the latter is discussed in another section of this report. The three biquads can be cascaded so that up to 6th order filters can be realized. Each biquad consists of five Controllable Transconductance Amplifiers (CTA) as well as two switchable capacitor arrays. The capacitor arrays and transconductance amplifiers can be digitally programmed. Each biquad can be programmed to realize various filter functions including: HP, BP, LP, AP, LPN and HPN.



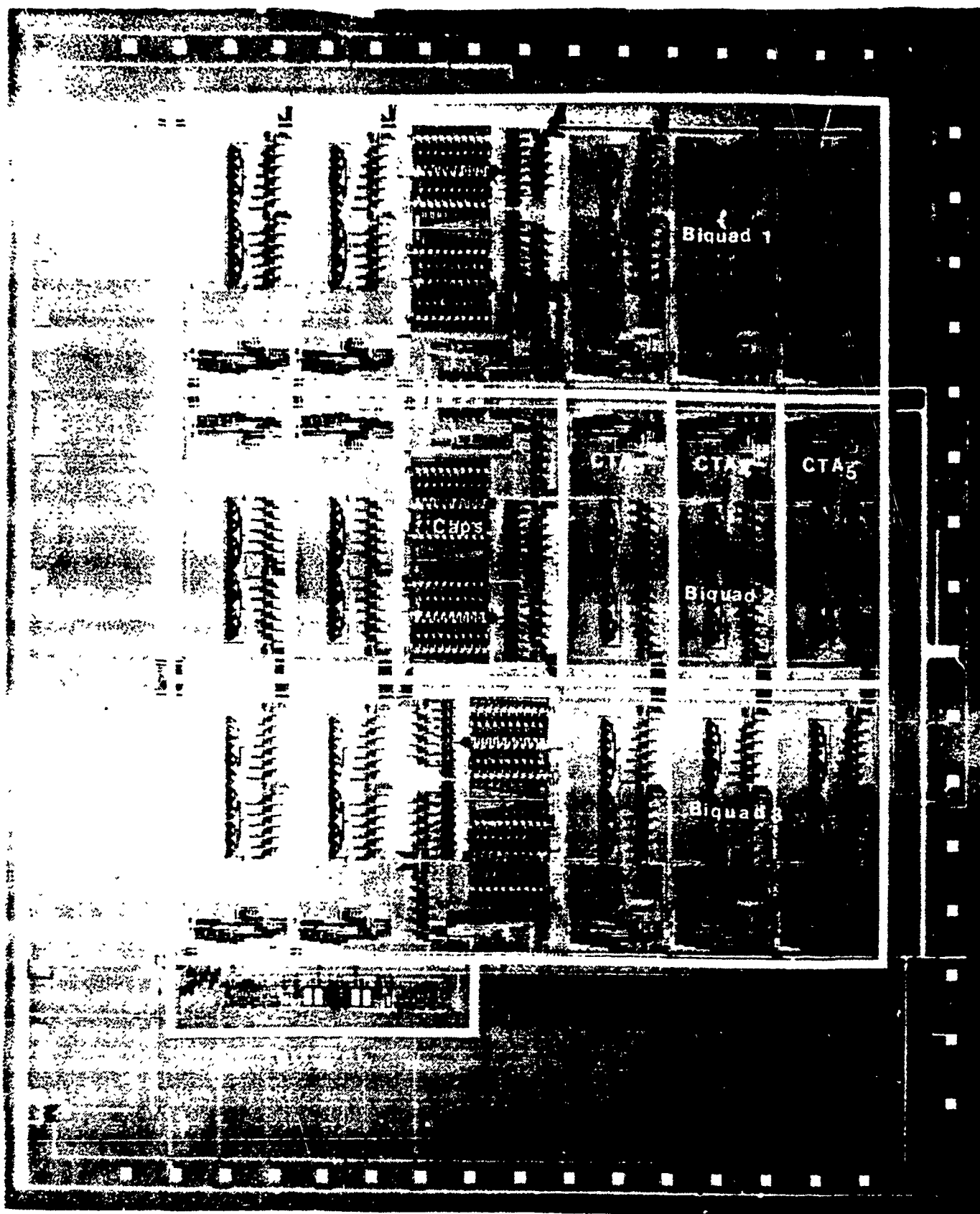


Fig. 5.10-2: The die photograph of DCASP-2.

Test Plans:

The DCASP-2 test chip has 29 pins which are dedicated to the CSP. Pin designations are shown in Fig. 5.10-3. The DCASP-2 chip is tested in the digital CSP controller board which is discussed in the Tuning Host Section (Sec. 2.4) of this report. The biasing voltages used for these tests are as follows:

$$V_{DD} = \text{Bulk} = +5V \quad (5.10 - 1)$$

$$V_{SS} = -5V \quad (5.10 - 2)$$

$$V_{bias} = -2.5V \quad (5.10 - 3)$$

$$V_{rq+} = V_{rf+} = -3.45V \quad (5.10 - 4)$$

$$V_{rq-} = V_{rf-} = -3.70V \quad (5.10 - 5)$$

The major instrument used for testing the filter characteristics is the HP 3585A which is a 20 Hz to 40MHz Spectrum Analyzer. This is used for both providing broadband input excitations and measuring frequency responses.

On the DCASP controller board, the HD6801 microcomputer is programmed to perform various tests. There are 4 DIP switches (with 16 total combinations) on the controller board which are used to configure the DCASP-2 chip in various ways for pertaining different tests. A brief description of the initial set of 16 test programs is provided below. A program listing appears in Table 5.10-1.

TEST 0 = Sets Biquad 1 up for testing on excitation and response busses with minimum f_o and BW values. The program sequence is as follows

Write zero's to every DCASP address

Turn on overall DCASP configuration

Turn on the first biquad

TEST 1 = Test basic functionality of Biquad 1. This test sequentially reconfigures BIQUAD 1 to realize nominal LP, BP, HP, and LPN filter functions. The input and output of Biquad are connected to the excitation and response busses for testing.

TEST 2 = Test for adjustment functionality via capacitor array for Biquad 1. Biquad 1 is connected in a BP configuration to the excitation and response busses. The capacitor array is sequentially scanned to change the center frequency of the filter.

TEST 3 = Test functional matching of each biquad and cascade circuitry. Initially, the three Biquads are configured in the bandpass configurations and sequentially connected to the excitation and response bus. They are then connected in cascades of first two and then three biquads.

TEST 4 = Tests for adjusted functionality via g_m control for Biquad 1. Biquad 1 is connected in a BP configuration to the excitation and response busses. The g_m value is sequenced by making coarse g_m adjustments to change the center frequency.

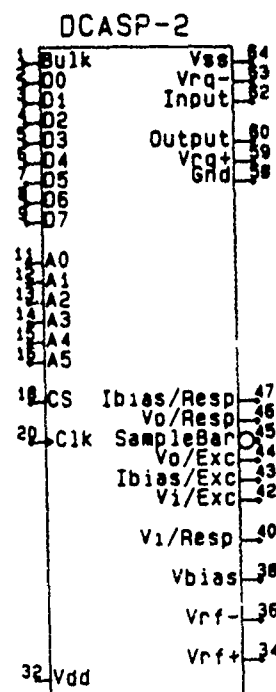


Fig. 5.10-3: The pin assignments of DCASP-2.

Table 5.10-1: Source listing of test programs

RESET PGM	"6801" SET SET	0FFFEH 0F000H	RESET VECTOR PROGRAM LOCATION
; DCASP-2 Filters : 16 TEST PROGRAMS HAVE BEEN INCLUDED			
; Date : 09/27/87 Time : 21:45			
;			
; by Lawrence Loh			
OUTPORT	SET	0FFH	DDR VALUE FOR OUT PORT
DDR1	SET	00H	DDR OF PORT1
PORT1	SET	02H	DATA REG. OF PORT1
DDR2	SET	01H	DDR OF PORT2
PORT2	SET	03H	DATA REG. OF PORT2
DDR3	SET	04H	DDR OF PORT 3
PORT3	SET	06H	DATA REG. OF PORT3
DDR4	SET	05H	DDR OF PORT4
PORT4	SET	07H	DATA REG. OF PORT4
CTR3	SET	0FH	CNTL AND STATUS REG. P3
TELL	MACRO	&ADR,&DATA	MACRO TO SEND DATA
	LDA	#&ADR	GET ADDRESS
	STAA	PORT4	SEND TO PORT4
	NOP		
	LDA	#&DATA	GET DATA
	STAA	PORT3	SEND TO PORT3
	NOP		
	MEND		
	ORG	RESET	
	FDB	PGM	INIT. RESET VECTOR
	DIRECT		SET ADR. MODE TO DIRECT
	ORG	PGM	PROGRAM
	SEI		SET INTRT. MASK
	LDS	#00FFH	DEFINE THE STACK
	LDA	#OUTPORT	LD CODE FOR OUT PORT
	STAA	DDR3	CONFIG. P3 AS OUT PORT
	STAA	DDR4	CONFIG. P4 AS OUT PORT
	LDA	#10H	
	STAA	CTR3	CONFIG. P3 C&S REG.
TELL		01H,03H	
TELL		02H,00H	
TELL		10H,00H	
TELL		12H,1FH	
TELL		13H,3FH	
TELL		14H,1FH	
TELL		15H,3FH	
TELL		16H,1FH	
TELL		17H,3FH	
TELL		18H,00H	
TELL		19H,00H	
TELL		1AH,00H	
TELL		1BH,3FH	
TELL		1CH,13H	
TELL		1EH,13H	
TELL		20H,00H	
TELL		22H,00H	
TELL		23H,00H	
TELL		24H,1FH	
TELL		25H,3FH	
TELL		26H,1FH	
TELL		27H,3FH	
TELL		28H,00H	
TELL		29H,3FH	
TELL		2AH,00H	
TELL		2BH,3FH	
TELL		2CH,13H	
TELL		2EH,13H	
TELL		30H,00H	
TELL		32H,00H	
TELL		33H,00H	
TELL		34H,1FH	
TELL		35H,3FH	

	TELL	36H, 1FH	
	TELL	37H, 3FH	
	TELL	38H, 00H	
	TELL	39H, 00H	
	TELL	3AH, 00H	
	TELL	3BH, 3FH	
	TELL	3CH, 13H	
	TELL	3EH, 13H	
BACK			
	LDA	PORT1	GET PORT1 SETTING
	CM	#0H	
	BEQ	T0	SET=0, GO TO TEST0
	CM	#1H	
	BEQ	T1	SET=1, GO TO TEST1
	CM	#2H	
	BEQ	T2	SET=2, GO TO TEST2
	CM	#3H	
	BEQ	T3	SET=3, GO TO TEST3
	CM	#4H	
	BEQ	T4	SET=4, GO TO TEST4
	CM	#5H	
	BEQ	T5	SET=5, GO TO TEST5
	CM	#6H	
	BEQ	T6	SET=6, GO TO TEST6
	CM	#7H	
	BEQ	T7	SET=7, GO TO TEST7
	CM	#8H	
	BEQ	T8	SET=8, GO TO TEST8
	CM	#9H	
	BEQ	T9	SET=9, GO TO TEST9
	CM	#0AH	
	BEQ	T10	SET=10 GOTO TEST10
	CM	#0BH	
	BEQ	T11	SET=11 GOTO TEST11
	CM	#0CH	
	BEQ	T12	SET=12 GOTO TEST12
	CM	#0DH	
	BEQ	T13	SET=13 GOTO TEST13
	CM	#0EH	
	BEQ	T14	SET=14 GOTO TEST14
	CM	#0FH	
	BEQ	T15	SET=15 GOTO TEST15
	JMP	BACK	OTHERWISE START AGAIN
	JMP	TEST0	ALL 0's
	JMP	TEST1	
	JMP	TEST2	
	JMP	TEST3	
	JMP	TEST4	
	JMP	TEST5	
	JMP	TEST6	
	JMP	TEST7	
	JMP	TEST8	
	JMP	TEST9	
	JMP	TEST10	
	JMP	TEST11	
	JMP	TEST12	
	JMP	TEST13	
	JMP	TEST14	
	JMP	TEST15	
T0			
T1			
T2			
T3			
T4			
T5			
T6			
T7			
T8			
T9			
T10			
T11			
T12			
T13			
T14			
T15			
TEST0			
	LDA	#00H	
	LDAB	#00H	
LOOP0			
	STAA	PORT4	
	NOP		
	NOP		
	STAB	PORT3	
	NOP		
	NOP		
	INCA		
	BNE	LOOP0	EXIT WHEN BACK TO 0
	TELL	01H, 03H	
	TELL	10H, 3FH	
	JMP	BLINK	

TEST1; Nominal LP, BP, HP, LPN Filters, (BIQUAD 1):

TELL	10H,00H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,00H
TELL	1AH,00H
TELL	1BH,3FH
TELL	1CH,09H
TELL	1EH,09H
JSR	DELAY_5,E

TELL	10H,03H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,3FH
TELL	1AH,00H
TELL	1BH,3FH
TELL	1CH,09H
TELL	1EH,09H
JSR	DELAY_5,E

TELL	10H,23H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,3FH
TELL	1AH,00H
TELL	1BH,3FH
TELL	1CH,09H
TELL	1EH,09H
JSR	DELAY_5,E

TELL	10H,2BH
TELL	12H,3FH
TELL	13H,3FH
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,00H
TELL	1AH,00H
TELL	1BH,3FH
TELL	1CH,09H
TELL	1EH,09H
JSR	DELAY_5,E
JMP	BLINK

TEST2 ; fo Sweep for BP Filter:

TELL	10H,03H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,3FH
TELL	1AH,00H
TELL	1BH,3FH

	TELL	1CH,13H	
	TELL	1EH,13H	
	JSR	DELAY_5,E	
	TELL	1CH,0FH	
	TELL	1EH,0FH	
	JSR	DELAY_5,E	
	TELL	1CH,09H	
	TELL	1EH,09H	
	JSR	DELAY_5,E	
	TELL	1CH,00H	
	TELL	1EH,00H	
	JSR	DELAY_5,E	
	TELL	1CH,13H	
	TELL	1EH,13H	
LOOP1	LDAB	#13H	
	LDAA	#1CH	SET C6
	STAA	PORT4	SET ADDRESS
	NOP		
	NOP		
	STAB	PORT3	SET DATA
	NOP		
	NOP		
	LDAA	#1EH	SET C7
	STAA	PORT4	SET ADDRESS
	NOP		
	NOP		
	STAB	PORT3	SET DATA
	NOP		
	NOP		
	JSR	LED_ON,E	
	JSR	DELAY_1,E	
	JSR	LED_OFF,E	
	JSR	DELAY_1,E	
	DECB		
	BNE	LOOP1	
WAIT1	JSR	LED_ON,E	
	BRA	WAIT1	

TEST3: Cascaded Bandpass Filters:

TELL	10H,00H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,3FH
TELL	1AH,00H
TELL	1BH,3FH
TELL	1CH,0FH
TELL	1EH,0FH
TELL	20H,00H
TELL	22H,00H
TELL	23H,00H
TELL	24H,3FH
TELL	25H,3FH
TELL	26H,3FH
TELL	27H,3FH
TELL	28H,00H
TELL	29H,3FH
TELL	2AH,00H
TELL	2BH,3FH
TELL	2CH,00H
TELL	2EH,00H
TELL	30H,00H
TELL	32H,00H
TELL	33H,00H
TELL	34H,3FH
TELL	35H,3FH

	TELL	36H,3FH	
	TELL	37H,3FH	
	TELL	38H,00H	
	TELL	39H,3FH	
	TELL	3AH,00H	
	TELL	3BH,3FH	
	TELL	3CH,00H	
	TELL	3EH,00H	
	TELL	10H,03H	
	JSR	DELAY_5,E	
	TELL	10H,00H	
	TELL	20H,03H	
	JSR	DELAY_5,E	
	TELL	20H,00H	
	TELL	30H,03H	
	JSR	DELAY_5,E	
	TELL	30H,00H	
	TELL	10H,05H	
	TELL	20H,02H	
	JSR	DELAY_5,E	
	TELL	20H,04H	
	TELL	30H,02H	
	JMP	BLINK	
TEST4	;TEST FOR DIFFERENT gm COARSE VALUES		
	TELL	10H,03H	
	TELL	12H,00H	
	TELL	14H,3FH	
	TELL	16H,3FH	
	TELL	18H,00H	
	TELL	1AH,00H	
	TELL	1CH,09H	
	TELL	1EH,09H	
LOOP2	LDAB	#3FH	
	LDAA	#13H	
	STAA	PORT4	
	STAB	PORT3	
	LDAA	#15H	
	STAA	PORT4	
	STAB	PORT3	
	LDAA	#17H	
	STAA	PORT4	
	STAB	PORT3	
	LDAA	#19H	
	STAA	PORT4	
	STAB	PORT3	
	LDAA	#1BH	
	STAA	PORT4	
	STAB	PORT3	
	JSR	LED_ON,E	
	JSR	DELAY_1,E	
	JSR	LED_OFF,E	
	JSR	DELAY_1,E	
	DECB		
	BNE	LOOP2	
BLINK	LDAA	#0FFH	LED ON
	LDAB	#03FH	LED OFF
LOOPBLNK	JSR	DELAY,E	
	STAA	PORT4	ON
	JSR	DELAY,E	
	STAB	PORT4	OFF
	JMP	LOOPBLNK	
DELAY	; Delay .5 seconds		
	PSHA		
	PSHB		

```

LDAA      #0FFH
LDAB      #0FFH
DELAY_A
DECA
DELAY_B
DECB
BNE       DELAY_B
TSTA
BNE       DELAY_A
PULB
PULA
RTS

DELAY_1  ; Delay 1 second
PSHA
PSHB
JSR
JSR       DELAY,E
PULB
PULA
RTS

DELAY_5  ; Delay 5 seconds
PSHA
PSHB
JSR       DELAY_1,E
JSR       DELAY_1,E
JSR       DELAY_1,E
JSR       DELAY_1,E
JSR       DELAY_1,E
PULB
PULA
RTS

DELAY_10 ; Delay 10 seconds
PSHA
PSHB
JSR       DELAY_5,E
JSR       DELAY_5,E
PULB
PULA
RTS

DELAY_20 ; Delay 20 seconds
PSHA
PSHB
JSR       DELAY_10,E
JSR       DELAY_10,E
PULB
PULA
RTS

LED_ON  ; Turns the LED on.
PSHA
TELL      0FFH,0AAH
PULA
RTS

LED_OFF ; Turns the LED off.
PSHA
TELL      03FH,55H
PULA
RTS

TEST5   ;CASE1: MIN BW, MIN W0
TELL      10H,03H
TELL      12H,00H
TELL      13H,00H
TELL      14H,00H

```

TELL	15H,01H
TELL	16H,00H
TELL	17H,01H
TELL	18H,00H
TELL	19H,01H
TELL	1AH,00H
TELL	1BH,01H
TELL	1CH,13H
TELL	1EH,13H
JMP	BLINK

TEST6 ;CASE2: MAX BW, MAX W0

TELL	10H,03H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,3FH
TELL	19H,3FH
TELL	1AH,3FH
TELL	1BH,3FH
TELL	1CH,00H
TELL	1EH,00H
JMP	BLINK

TEST7 ;CASE3: MAX W0 AND SMALLEST BW

TELL	10H,03H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,01H
TELL	1AH,00H
TELL	1BH,01H
TELL	1CH,00H
TELL	1EH,00H
JMP	BLINK

TEST8 ;CASE4: MIN BW, LARGEST W0

TELL	10H,03H
TELL	12H,00H
TELL	13H,00H
TELL	14H,3FH
TELL	15H,3FH
TELL	16H,3FH
TELL	17H,3FH
TELL	18H,00H
TELL	19H,01H
TELL	1AH,00H
TELL	1BH,01H
TELL	1CH,00H
TELL	1EH,13H
JMP	BLINK

TEST9 ;CASE5: MIN W0, Q= 0.5

TELL	10H,03H
TELL	12H,00H
TELL	13H,00H
TELL	14H,00H
TELL	15H,01H
TELL	16H,00H
TELL	17H,01H
TELL	18H,19H
TELL	19H,02H
TELL	1AH,19H
TELL	1BH,02H
TELL	1CH,13H

	TELL	1EH, 13H
	JMP	BLINK
TEST10	;CASE6: MAX BW, Q = 0.5	
	TELL	10H, 03H
	TELL	12H, 00H
	TELL	13H, 00H
	TELL	14H, 3FH
	TELL	15H, 3FH
	TELL	16H, 3FH
	TELL	17H, 3FH
	TELL	18H, 3FH
	TELL	19H, 3FH
	TELL	1AH, 3FH
	TELL	1BH, 3FH
	TELL	1CH, 00H
	TELL	1EH, 00H
	JMP	BLINK
TEST11	;CASE7: W0 DAC @ Vref+	
	TELL	10H, 03H
	TELL	12H, 00H
	TELL	13H, 00H
	TELL	14H, 3EH
	TELL	15H, 3FH
	TELL	16H, 3FH
	TELL	17H, 3FH
	TELL	18H, 3FH
	TELL	19H, 3FH
	TELL	1AH, 3FH
	TELL	1BH, 3FH
	TELL	1CH, 00H
	TELL	1EH, 00H
	JMP	BLINK
TEST12	;CASE8: BW DAC @ Vref+	
	TELL	10H, 03H
	TELL	12H, 00H
	TELL	13H, 00H
	TELL	14H, 3FH
	TELL	15H, 3FH
	TELL	16H, 3FH
	TELL	17H, 3FH
	TELL	18H, 3EH
	TELL	19H, 3FH
	TELL	1AH, 3EH
	TELL	1BH, 3FH
	TELL	1CH, 00H
	TELL	1EH, 00H
	JMP	BLINK
TEST13	;CASE9: W01, BW, DAC @ Vref-	
	TELL	10H, 03H
	TELL	12H, 00H
	TELL	13H, 00H
	TELL	14H, 00H
	TELL	15H, 3FH
	TELL	16H, 00H
	TELL	17H, 3FH
	TELL	18H, 00H
	TELL	19H, 3FH
	TELL	1AH, 00H
	TELL	1BH, 3FH
	TELL	1CH, 00H
	TELL	1EH, 00H
	JMP	BLINK
TEST14	;CASE10: W02 DAC @ Vref-	
	TELL	10H, 03H
	TELL	12H, 00H
	TELL	13H, 00H

TELL	14H,01H
TELL	15H,3FH
TELL	16H,00H
TELL	17H,3FH
TELL	18H,00H
TELL	19H,3FH
TELL	1AH,00H
TELL	1BH,3FH
TELL	1CH,00H
TELL	1EH,00H
JMP	BLINK

TEST15 ;CASE11: BW2 DAC @ Vref-

TELL	10H,03H
TELL	12H,00H
TELL	13H,00H
TELL	14H,00H
TELL	15H,3FH
TELL	16H,00H
TELL	17H,3FH
TELL	18H,01H
TELL	19H,3FH
TELL	1AH,01H
TELL	1BH,3FH
TELL	1CH,00H
TELL	1EH,00H
JMP	BLINK

END

Test 5(case 1)-15(case 10)

These tests are for determining the f_o and $B\bar{W}$ adjustment range of Biquad 1 which is configured in the BP mode. Eleven different f_o and $B\bar{W}$ values are set which correspond to extreme settings on the g_m and capacitor array values, as well as at positions for determining limited LSB resolution on f_o and $B\bar{W}$. These tests are summarized in Table 5.10-2.

For example, Test 5(Case 1) corresponds to the minimum f_o , minimum $B\bar{W}$ filter attainable with Biquad 1. A brief flow diagram of the program for this test appears in Table 5.10-3.

Experimental Results

Test 0 through Test 4 are intended only to verify basic functionality of the CSP. A spectrum analyzer was connected to the CSP via the excitation and response busses when these tests were run. Basic functionality was verified in all of these tests. Preliminary test results for Tests 5-15 are summarized in Table 5.10-4. Emphasis in these tests was on quantifying g_m and $B\bar{W}$ adjustment range. These measurements were obtained from an HP3585A Spectrum Analyzer by the following procedures:

1. Set DIP switches to the desired test (5 to 15).
2. Reset the microcomputer (HD6801).
3. Measure h_{max} [the peak value].
4. Find f_{3db1} and f_{3db2} .
5. Obtain f_o , $B\bar{W}$, and Q by calculating:

$$f_o = \sqrt{f_{3db1} \times f_{3db2}} \quad (5.10 - 6)$$

$$B\bar{W} = f_{3db2} - f_{3db1} \quad Q = \frac{f_o}{B\bar{W}} \quad (5.10 - 7)$$

The results from experiments have shown that, in general, the biquads and switching capacitors in DCASP-2 are functional. The domain of f_o and $B\bar{W}$ values is somewhat smaller than the theoretical as anticipated. This reduction can be seen by comparing the results in Table 5.10-4 with those in Table 5.10-5. For Case 1 and Case 2, the attainable ranges of f_o and $B\bar{W}$ are found to be smaller than expected. Cases 3 and 4 correspond to the most stringent filter specifications, namely the smallest bandwidths at the highest frequencies. The theoretical corresponding pole Q 's are 188 and 600 respectively and any significant Q -enhancement will cause instability. Experimentally, the circuit of Case 3 oscillated and that of Case 4 is still being investigated. The performance of the circuits corresponding to Cases 6-11 are much as expected.

The measured adjustment ranges are depicted in Fig. 5.10-4. The theoretical and experimental adjustment ranges are superimposed in Fig. 5.10-5.

The basic functionality of DCASP-2 has been experimentally verified. The results are consistent with theoretical expectations. A preliminary investigation of the f_o and BW adjustment ranges has also been made. Additional detailed tests relating to linearity, resolution, adjustment range and noise are planned in the near future.

CASE	g_{m2} (14H,15H)	g_{m3} (16H,17H)	g_{m5} (1AH,1BH)	C_6 (1CH)	C_7 (1EH)	Description
1	0100	0100	0100	13H	13H	minimum f_o , minimum $B\bar{W}$
2	3F3F	3F3F	3F3F	00H	00H	maximum f_o , maximum $B\bar{W}$
3	3F3F	3F3F	0100	00H	00H	maximum f_o at smallest $B\bar{W}$
4	3F3F	3F3F	0100	00H	13H	minimum $B\bar{W}$ at largest f_o
5	0100	0100	0219	13H	13H	minimum f_o , $Q=0.5$
6	3F3F	3F3F	3F3F	0BH	00H	maximum $B\bar{W}$, $Q=0.5$
7	3F3F	3F3F	3F3F	00H	00H	1 bit resolution for f_o
8	3F3F	3F3F	3F3F	00H	00H	1 bit resolution for $B\bar{W}$
9	3F00	3F00	3F00	00H	00H	some f_{o1} and $B\bar{W}_1$
10	3F01	3F00	3F00	00H	00H	1 bit resolution for f_{o1}
11	3F00	3F00	3F01	00H	00H	1 bit resolution for $B\bar{W}_1$

Table 5.10-2: Configuring BP Filters for Several Cases

Common Settings: BIQUAD1 (Address 10H)=03H

g_{m1} (Address 12H, 13H)=03H

g_{m4} (Address 18H, 19H)= g_{m5} (Address 1AH; 1BH)

		Address	Data
1.	Select Biquad 1	10 _H	03 _H
2.	Set g_{m1} to zero		
	(g_{m1} coarse= 0)	13 _H	00 _H
	(g_{m1} fine= 0)	12 _H	00 _H
3.	Set ($g_{m2} = g_{m3} = g_{m4} = g_{m5}$		
	to minimum g_m		
	(g_{m2} coarse= 0)	15 _H	00 _H
	(g_{m3} coarse= 0)	17 _H	00 _H
	(g_{m4} coarse= 0)	19 _H	00 _H
	(g_{m5} coarse= 0)	1B _H	00 _H
	(g_{m2} fine=minimum)	14 _H	01 _H
	(g_{m3} fine=minimum)	16 _H	01 _H
	(g_{m4} fine=minimum)	18 _H	01 _H
	(g_{m5} fine=minimum)	1A _H	01 _H
4.	Set $C_6 = C_7$ =maximum		
	(C_6 =maximum)	1C _H	13 _H
	(C_7 =maximum)	1E _H	13 _H

Table 5.10-3: Flow diagram for Test 5.

CASE	$f_{3db1}(Hz)$	$f_{3db2}(Hz)$	$f_o(Hz)$	$B\bar{W}(Hz)$	Q	$H_{MAX}(d)$
1	1250.8 ± 1.3	3156.0 ± 1.3	1986.8	1905.2	1,0429	-8.28
2	$987,000 \pm 920$	$1,802,593 \pm 920$	1,333,851.3	815,593	1.6354	-7.49
3	Oscillates at 11.45 MHz					
4	Oscillates at 1.7 MHz					
5	281.5 ± 3.2	$3,337 \pm 3.2$	969.2	3,055.5	0.3172	-8.97
6	$574,700 \pm 950$	$1,460,100 \pm 950$	916,034.6	885,400	1.0346	-7.88
7	$985,100 \pm 920$	$1,801,150 \pm 920$	1,332,033.4	816,050	1.6323	-7.33
8	$987,460 \pm 920$	$1,801,720 \pm 920$	1,333,838.9	814,260	1.6381	-7.30
9	$734,300 \pm 870$	$1,560,800 \pm 870$	1,070,558.5	826,500	1.2953	-7.33
10	$736,200 \pm 870$	$156,270 \pm 870$	1,072,594.9	826,500	1.2978	-7.31
11	$733,350 \pm 870$	$1,560,800 \pm 870$	1,069,865.7	827,450	1.2930	-7.32

Table 5.10-4: Results of DCASP-2 for Case 1--Case 1--Case 11 in Table 5.10-1.

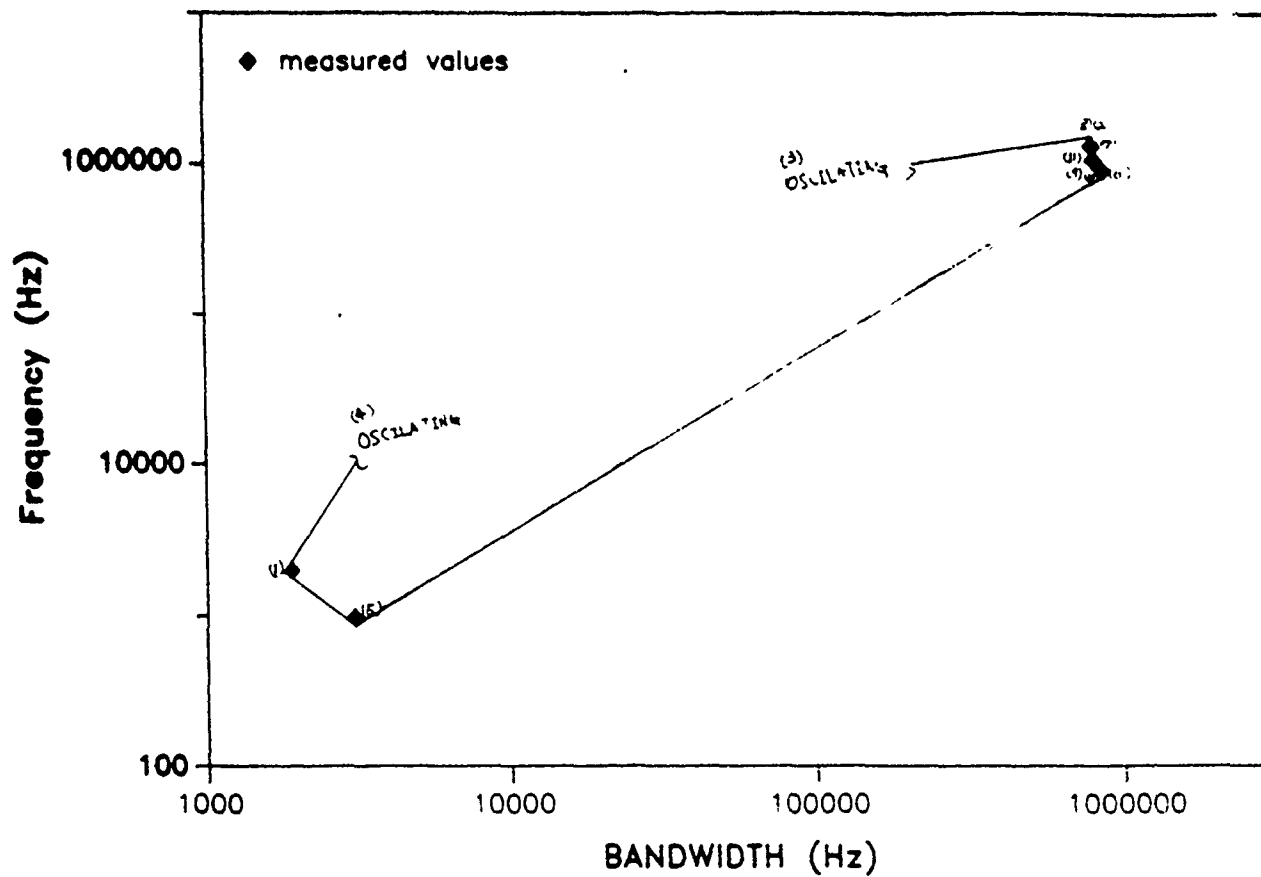


Fig. 5.10-4: The tuning range measured from DCASP-2.

CASE	f_o	$B\bar{W}$	Q
1	1552.83	1552.83	1
2	2,976,000	2,976,000	1
3	2,976,000	15,834.86	187.94
4	931,939.5	1,552.83	600.16
5	1552.83	2,942.589	0.5278
6	1,519,502	2,976,000	0.5106
7	2,965,038	2,976,000	0.9963
8	2,976,000	2,954,126	1.0074
9	1,947,150	1,947,150	1
10	1,953,043	1,947,150	1.0030
11	1,947,150	1,958,953	0.9940

Table 5.10-5: Theoretic Values of Parameters for Case 1 through Case 11 in Table 5.10-1.

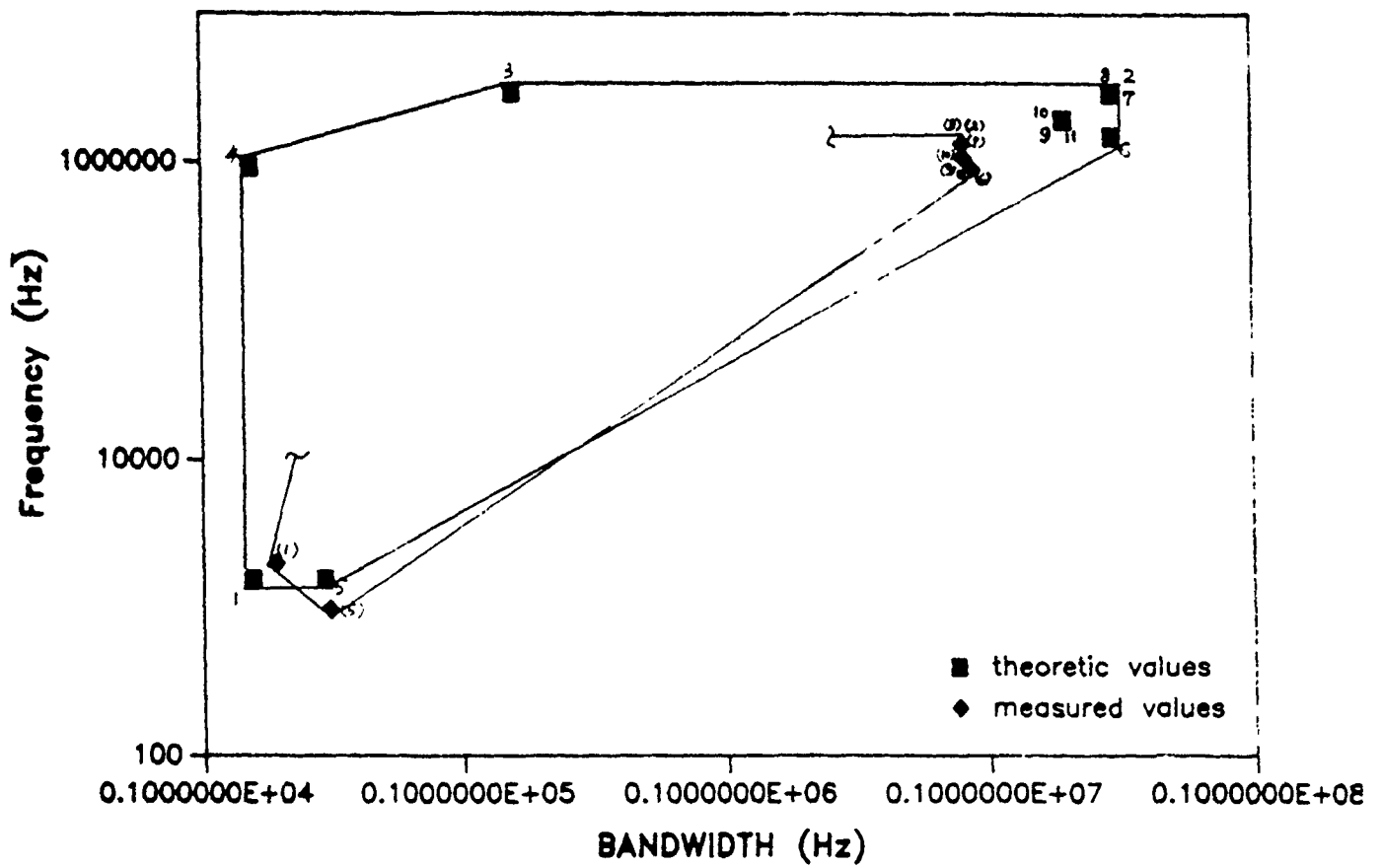


Fig. 5.10-5: Comparison of tuning ranges between measure and theoretic values.

5.11 OTA with 6 Selectable Output Stages

Name:	OTA 6-bit
MOSIS ID:	23528
Fab. ID:	M72LJH-1
Technology:	CBPE-MOSIS 3μ CMOS double-poly p-well process
Fabricated:	July-August 1987
Chip Size:	$2300\mu \times 3400\mu (7.82mm^2)$
Active Area:	$300\mu \times 750\mu (0.225mm^2)$
Number of Pads:	17
Packaging:	28 pin package
Status:	Currently being tested.

Purpose:

This test chip is used to characterize the 6-output stage OTA used in the controlled transconductance amplifier (CTA) of DCASP-2. As was reported in Section 2.1.2.1, the 2-output stage OTA used in DCASP-1 exhibits a large "gap" in the attainable values of g_m . The 6-output stage OTA described in this section was designed to eliminate such gaps as well as to allow much smaller values of g_m than possible with the previous designs.

In addition to the characterization of the g_m adjustment range for the OTA, the following will be studied: effect of V_{bias} ; dynamic range; linearity; noise characteristics; frequency response; power dissipation.

Description:

A circuit schematic and device sizes are given in Section 2.1.2.1 and repeated as Fig. 5.11-1 and Table 5.11-1. In addition to the OTA circuit, the test chip contains a 6-bit latch which is used to hold the digital control word for the 6 output stages of the OTA. The die photograph of the test cell is shown in Fig. 5.11-2 (Note: The DAC contained on this test cell is described in Sec. 5.12). A diagram showing the pinouts on the test IC is given in Fig. 5.11-3. Following is a description of each pin:

Pin 1: Bulk	The connection to the $n+$ substrate of the chip
-------------	--

Pin 5-10: $D_5 D_4 D_3 D_2 D_1 D_0$	Digital input to the 6-bit latch. D_5 controls the largest OTA output stage, D_0 the smallest.
Pin 11: CLK	Clock input to the 6-bit latch.
Pin 12: LOAD	Enable input to the 6-bit latch.
Pin 14: I_{out}	OTA output current.
Pin 18: V_{SS}	Negative supply for the test circuit.
Pin 19: V_{bias}	DC input voltage used to bias the currents in the cascoded structure of the OTA input stage.
Pin 20: V_{tail}	DC input voltage used to adjust the g_m of the OTA by adjusting the tail current in the cascoded structures of the OTA input stage.
Pin 21: V_{in}^-	Negative input terminal of the OTA.
Pin 22: V_{in}^+	Positive input terminal of the OTA.
Pin 23: V_{DD}	Positive supply for the test circuit.

As discussed in Sec. 2.1.2.1, the 6-output stage OTA was designed to provide 11 equally spaced (in the logarithmic sense) gain factors. Table 5.11-2 (repeated from Sec. 2.3.3.1) lists the digital input settings used to achieve these 11 gain factors.

Test Plan:

(a) Coarse and fine g_m adjustment range measurement

The circuit shown in Fig. 5.11-4 was used to test the OTA. The op amp in the test circuit allows the OTA output to be ideally terminated in a short circuit by maintaining the output voltage at approximately 0V. The experimental value of g_m is computed from measurements of V_{out} , R_F and V_{in} using the equation

$$g_m = \frac{I_{out}}{V_{in}} = \frac{V_{out}}{R_F V_{in}} \quad (5.11 - 1)$$

This is done for several values of the control voltage V_{tail} for measurement of the fine

g_m adjustment characteristics. To obtain the coarse adjustment characteristics, the procedure is repeated for all 11 of the coarse control digital input states of interest, i.e., for those states which were designed to yield 11 equally spaced (in the logarithmic sense) gain factors (see Section 2.1.2.1). From the resulting data, a plot of g_m versus V_{tail} is constructed for each of the coarse control settings.

(b) Effect of V_{bias}

Experimental determination of the optimal value of V_{bias} is desired. The circuit shown in Fig. 5.11-4 is again used. The procedure is similar to that in (a), except that the measurements are repeated for different values of V_{bias} . Only the largest gain state ($D_5 D_4 D_3 D_2 D_1 D_0 = 111111$) is considered.

Complete test plans to study the additional characteristics of concern are under development.

Experimental Results:

(a) Coarse and fine g_m adjustment range

Fig. 5.11-5 shows the g_m versus V_{tail} curves for each of the 11 states of interest. It can be seen that the curves are not exactly equally spaced; some variation is to be expected from transistor mismatches and process variations.

Recall from Section 2.1.2.2 the estimate that, while maintaining a resolution of better than 1% in g_m , a fine g_m adjustment by a factor of approximately 1.8 is allowed with the DAC of DCASP-2. It follows that the coarse g_m adjustment provided by the differently-sized OTA output stages must always be by a factor less than 1.8, in order that there are no undesirable gaps in the attainable values of g_m . Looking at Fig. 5.11-5, and in particular for $V_{tail} = -3.7V$, it appears the coarse g_m values do vary by a factor less than 1.8; i.e., the curves appear to be separated by less than $\log_{10}(1.8) = .255$. The design goal of maintaining a g_m resolution better than 1% appears to have been achieved (assuming, of course, that the fine adjustment provided by the DAC does indeed permit a g_m adjustment by a factor greater than 1.8).

Note that measurements for $V_{tail} \lesssim -3.9$ are not included in Fig. 5.11-5. The output signals for such values of V_{tail} are excessively distorted due to this gate voltage approaching the negative supply rail.

(b) Effect of V_{bias}

Fig. 5.11-6 shows the g_m versus V_{tail} curve for three different bias voltages V_{bias} . All six output stages are enabled for these cases.

The curves suggest that the fine g_m adjustment by a factor of 1.8 can be achieved

with any of the three values of V_{bias} . However, in the range of interest ($-3.9 \lesssim V_{tail} \lesssim -3.4$), the curves are clearly more linear for $V_{bias} = -2.0V$ and $-2.5V$ than for $V_{bias} = -3.0V$. Recall that the design of the DAC was based upon a linear relationship between g_m and V_{tail} , for this reason a V_{bias} of $-2.0V$ or $-2.5V$ is favored. However, dynamic range considerations favor the more negative value of V_{bias} . In any case, the value $V_{bias} = -2.5V$ appears to be acceptable.

Further tests of this 6-output stage OTA are pending.

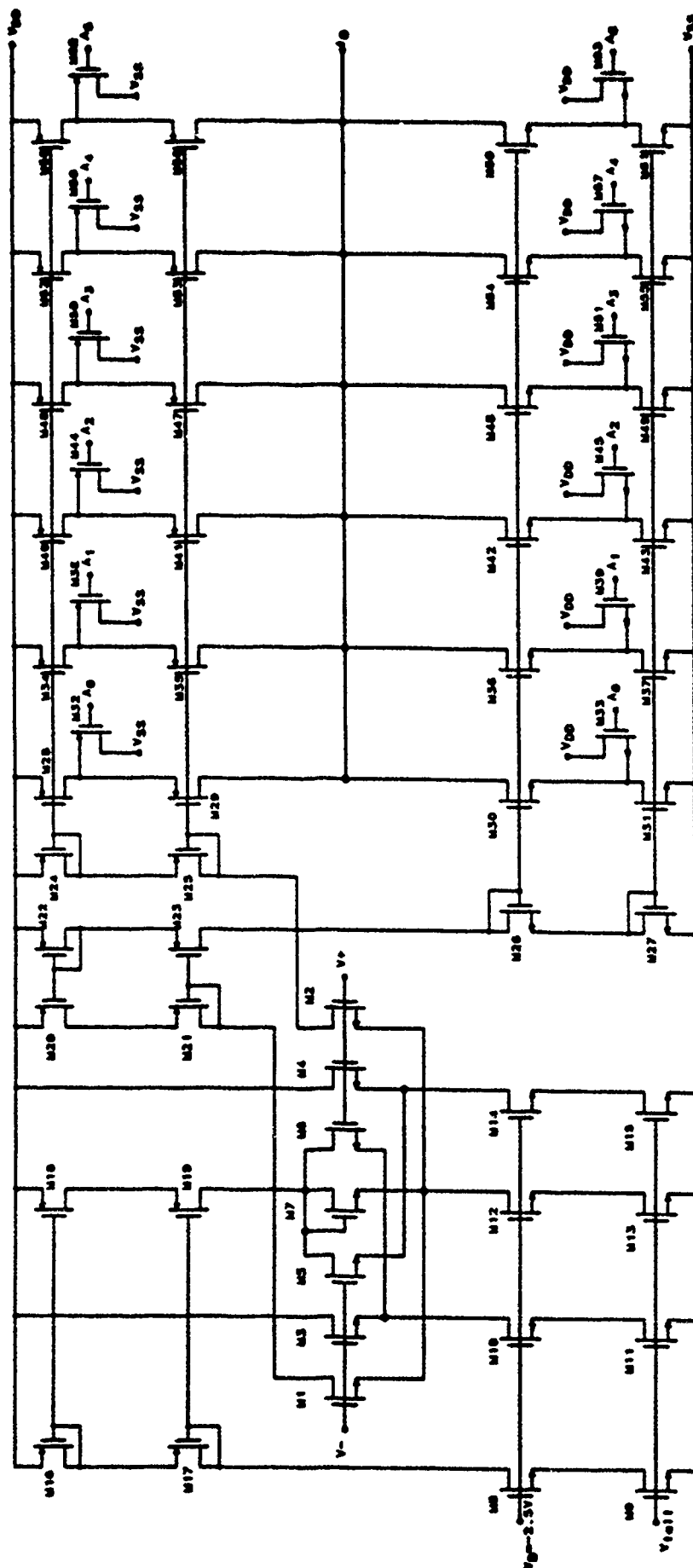


Fig. 5.11-1: Circuit schematic of 6-output stage OTA.

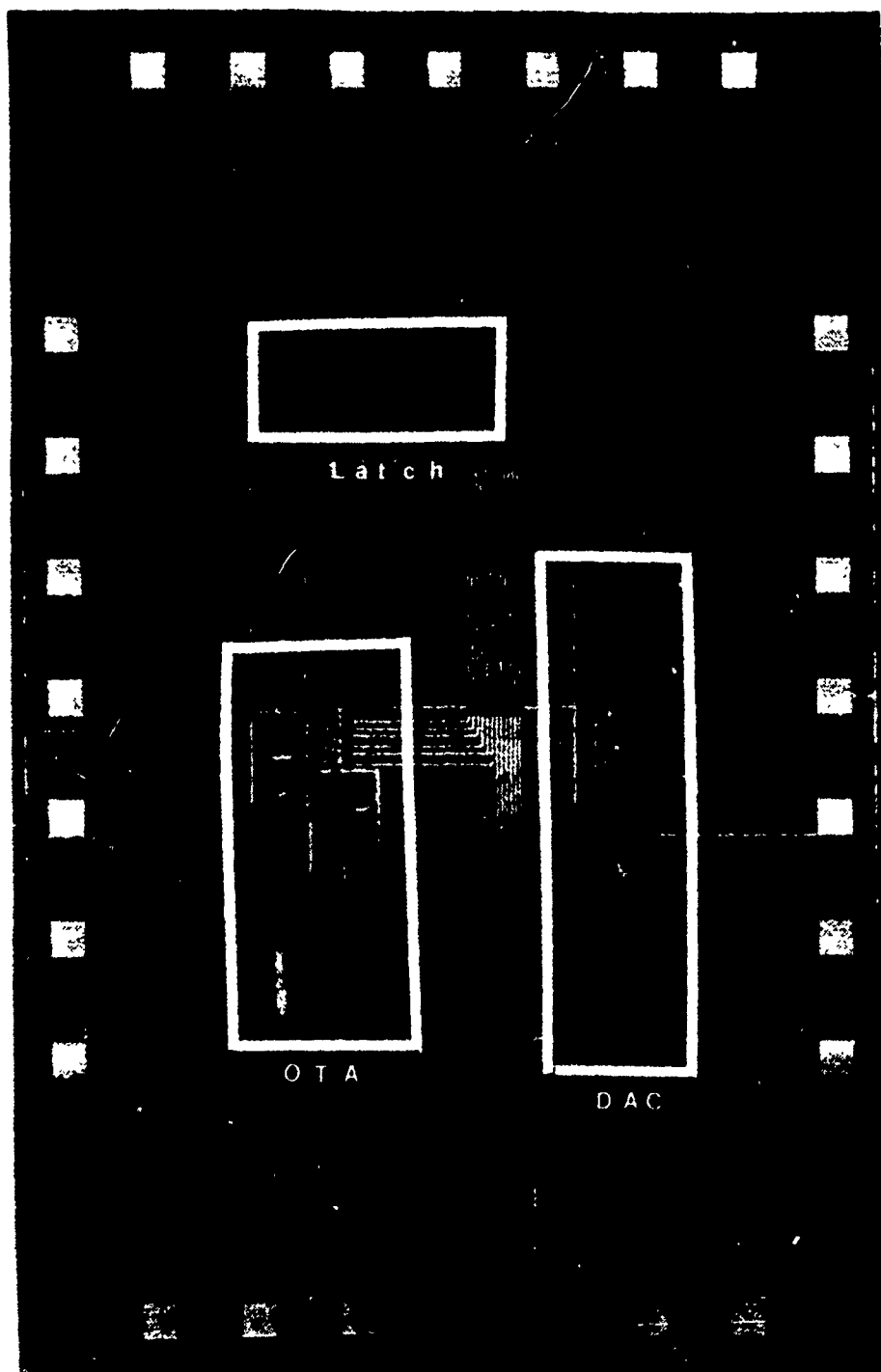


Fig. 5.11-2: Layout of 6-output stage OTA cell.

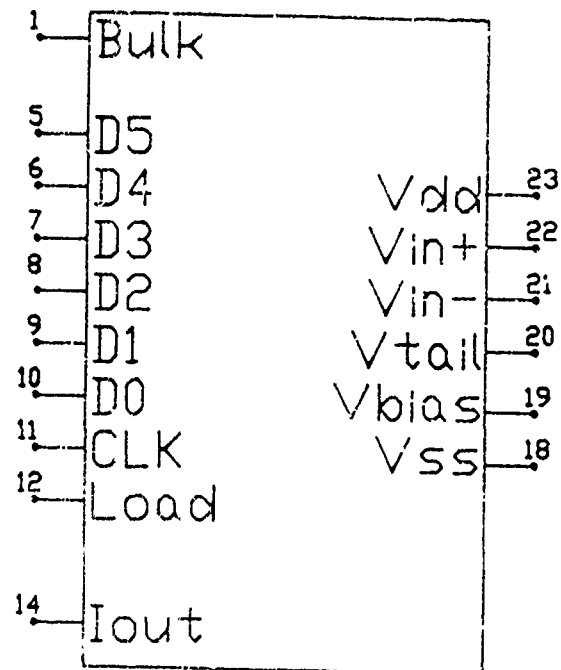


Fig. 5.11-3: Pinouts for the 6-output stage OTA test cell.

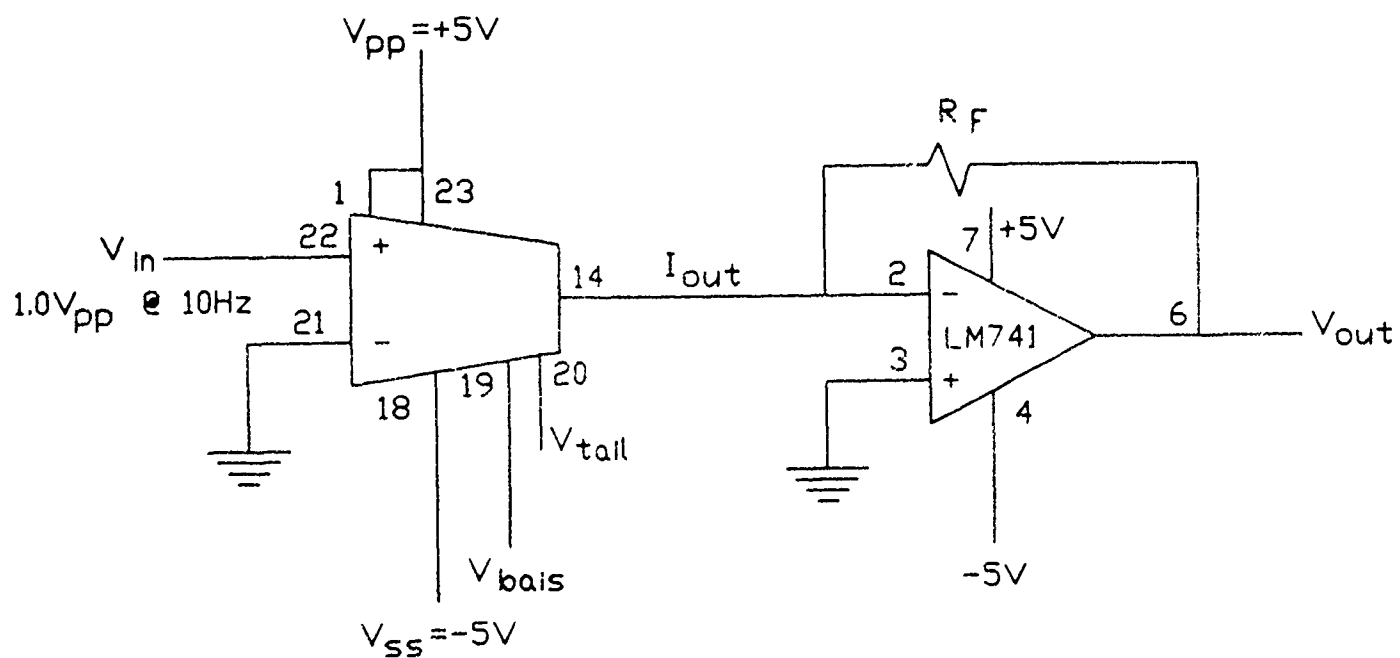


Fig. 5.11-4: Circuit used to obtain g_m versus V_{tail} curves for the 6-bit output stage OTA of DCASP-2.

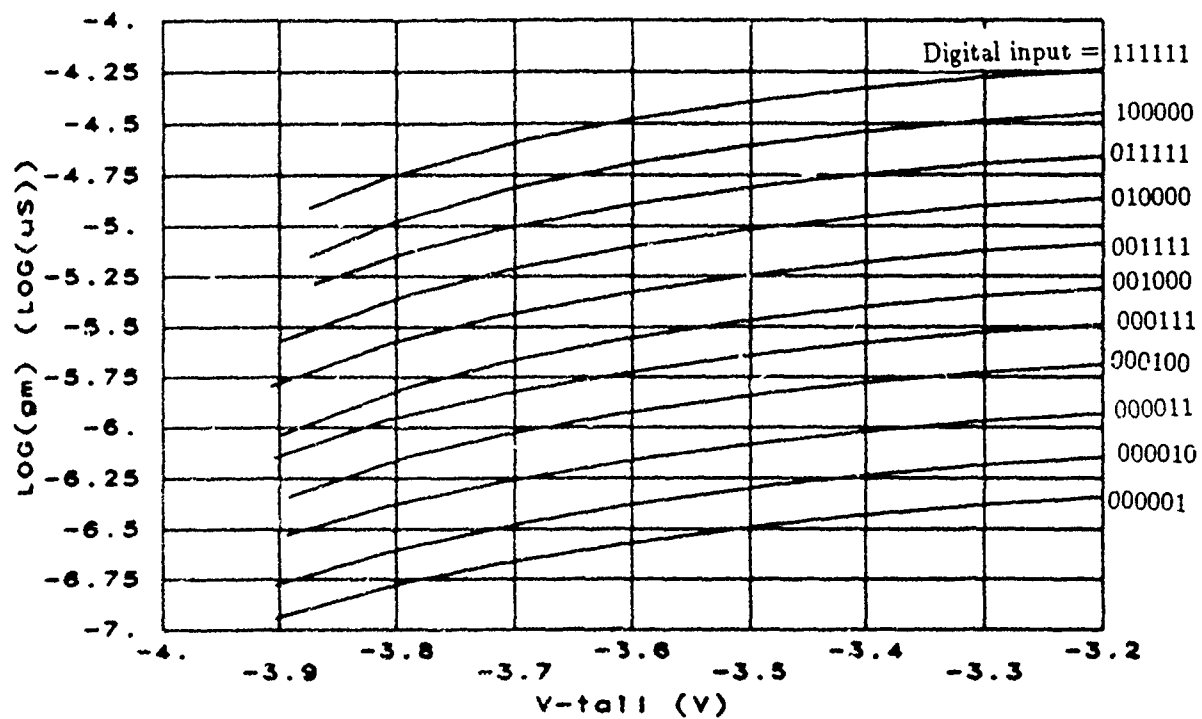


Fig. 5.11-5: g_m vs V_{tail} for different digital inputs.

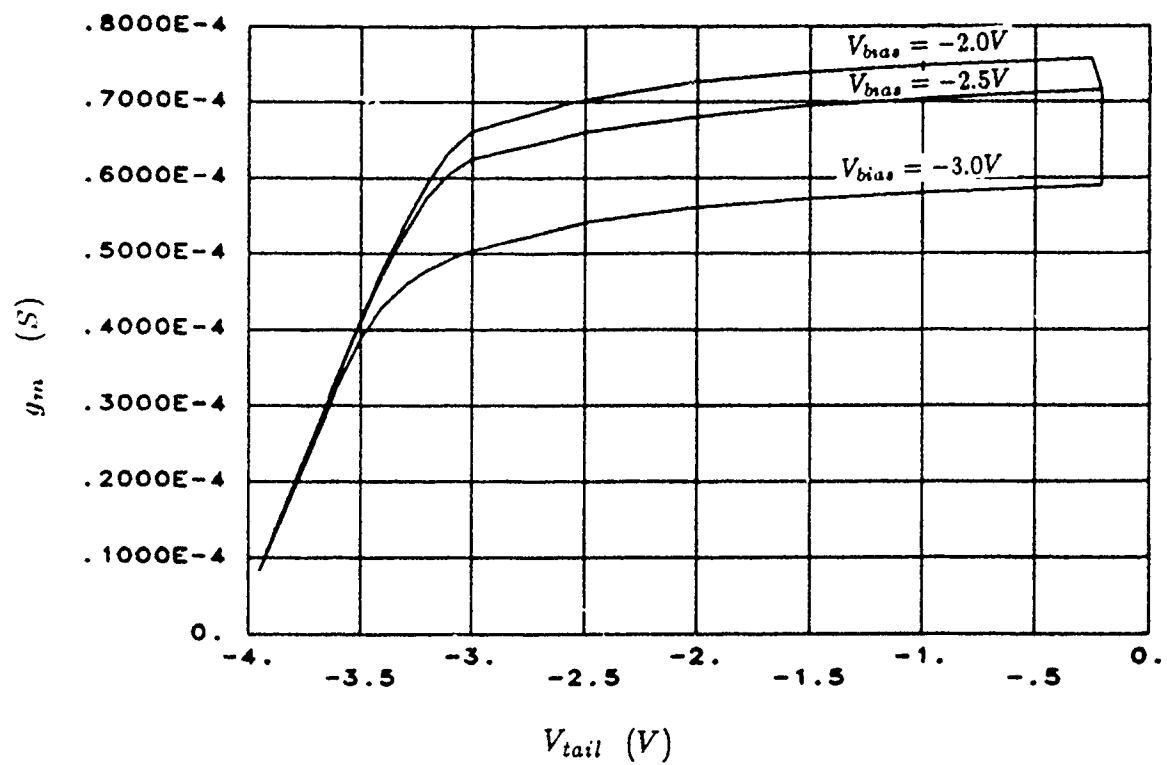


Fig. 5.11-6 g_m versus V_{tail} for different values of V_{bias} .

Table 5.11-1: Device Sizing for 6-output stage OTA Fig. 5.11-1.

DEVICE	SIZE (microns)	
	W	L
M1-M2	8	5
M3-M4	16	5
M5-M6	8	5
M7	7	5
M8-M9	40	3
M10-M15	80	3
M16-M17	60	3
M18-M21	120	3
M22-M23	60	3
M24-M25	120	3
M26-M27	60	3
M28-M31	5	11
M32-M33	7	3
M34-M37	6	9
M38-M39	7	3
M40-M43	15	9
M44-M45	7	3
M46-M49	21	6
M50-M51	7	3
M52-M55	17	3
M56-M57	7	3
M58-M61	44	3
M62-M63	17	3

Table 5.11-2: Theoretical gain of 6-output stage OTA as a function of coarse control digital input, assuming gain of first stage is $(1.618)^{-10}$.

A_5	A_4	A_3	A_2	A_1	A_0	Gain
0	0	0	0	0	1	$(1.618)^{-10} = .00813$
0	0	0	0	1	0	$(1.618)^{-9} = .01316$
0	0	0	0	1	1	$(1.618)^{-8} = .0213$
0	0	0	1	0	0	$(1.618)^{-7} = .0344$
0	0	0	1	1	1	$(1.618)^{-6} = .0557$
0	0	1	0	0	0	$(1.618)^{-5} = .0902$
0	0	1	1	1	1	$(1.618)^{-4} = .1459$
0	1	0	0	0	0	$(1.618)^{-3} = .236$
0	1	1	1	1	1	$(1.618)^{-2} = .382$
1	0	0	0	0	0	$(1.618)^{-1} = .618$
1	1	1	1	1	1	$(1.618)^0 = 1.000$

5.12 6-Bit Logarithmic DAC With Switching Tree

MOSIS ID: 23528
Fab. ID: M72LJH-1
Technology: CBPE-MOSIS 3μ CMOS Double-Poly p-Well
Fabricated: March-April 1987
Chip Size: $2300\mu \times 3400\mu$
Active Area:
Number of Pads: 14
Packaging: 28 Pin Package
Status: Tested

Purpose:

This test chip is used to characterize the monotonicity as well as logarithmic-increment feature of the Digital-to-Analog Converter (DAC) circuit using the switching tree decoding. This building block has been designed and fabricated into the DCASP-2 chip (refer to Sec. 5.10) to provide the OTA g_m fine-control voltages in biquads.

Description:

The test chip, also referred to as Log DAC, has almost the same structure as previous Small DAC test chips. A block diagram of the Log DAC appears in Fig. 5.12-1 along with a circuit diagram in Fig. 5.12-2. Device sizes and geometries are summarized in Table 5.12-3. A pin diagram appears in Fig. 5.12-3 and a die photograph in Fig. 5.12-4. The only difference is that the incremental voltages changes are equally spaced on a logarithmic scale. The reasons for employing this scheme are fully discussed in Sec. 2.1 (DAC and Fine g_m Adjustments) and will not be repeated in this section. The resistive poly string is therefore spaced logarithmically instead of linearly. In Table 5.12-1, the resistor values and the incremental rates are listed. It is expected that each incremental rate will be maintained at a value around 1.01.

Test Plans: (See Test Plans, Sec 5.9)

Experimental Results:

The performance of the Log DAC can be characterized by the results shown in TABLE

DAC3.1. The average value of incremental ratios $\frac{R_N}{R_{N-1}}$ can be easily calculated by

$$\begin{aligned}\left(\frac{R_N}{R_{N-1}}\right)_{average} &= \left(\frac{R_{63}}{R_1}\right)^{\frac{1}{62}} = \left(\frac{R_{63}/R}{R_1/R}\right)^{\frac{1}{62}} \\ &= \left(\frac{2.01\%}{1.17\%}\right)^{\frac{1}{62}} = 1.00866174\end{aligned}\tag{5.12 - 1}$$

Table 5.12-1: Resistor values used in small log DAC and DCASP-2. (Refer to Fig. 5.12-6 for the definitions of X, Y, Z).

N	X (μm)	Y (μm)	Z (μm)	# Squares	R_N (Ω)	$\frac{R_N}{R_N - 1}$
1	7	4	9	5.794	231.8	—
2	7	4	8	5.850	234.0	1.010
3	6	4	4	5.900	236.0	1.009
4	5	5	4	5.950	238.0	1.008
5	8	4	19	6.010	240.4	1.010
6	7	5	14	6.057	242.3	1.008
7	8	4	13	6.108	244.3	1.008
8	8	4	11	6.164	246.6	1.009
9	8	4	10	6.200	248.0	1.006
10	7	5	9	6.255	250.2	1.009
11	7	5	8	6.325	253.0	1.011
12	8	4	7	6.371	254.8	1.007
13	8	5	21	6.438	257.5	1.011
14	8	5	17	6.494	259.8	1.009
15	8	5	14	6.557	262.3	1.010
16	8	4	5	6.600	264.0	1.007
17	8	5	11	6.655	266.2	1.008
18	7	5	5	6.700	268.0	1.007
19	8	5	9	6.755	270.2	1.008
20	8	5	8	6.825	273.0	1.010
21	10	4	20	6.900	276.0	1.011
22	10	4	16	6.950	278.0	1.007
23	9	5	16	7.012	280.5	1.009
24	9	5	13	7.085	283.4	1.010
25	10	4	9	7.144	285.8	1.008
26	10	4	8	7.200	288.0	1.008
27	9	5	9	7.255	290.2	1.008
28	9	5	8	7.325	293.0	1.010
29	11	4	17	7.385	295.4	1.008
30	10	5	20	7.450	298.0	1.009

Table 5.12-1, con't.

N	X (μm)	Y (μm)	Z (μm)	# Squares	R_N (Ω)	$\frac{R_N}{R_N - 1}$
31	11	4	11	7.514	300.6	1.009
32	10	5	13	7.585	303.4	1.009
33	11	4	8	7.650	306.0	1.009
34	11	4	7	7.721	308.8	1.009
35	10	5	9	7.755	310.2	1.004
36	12	4	16	7.850	314.0	1.012
37	10	5	7	7.914	316.6	1.008
38	11	5	17	7.994	319.8	1.010
39	11	5	14	8.057	322.3	1.008
40	11	5	12	8.117	324.7	1.007
41	10	5	5	8.200	328.0	1.010
42	11	5	9	8.255	330.2	1.007
43	13	4	14	8.336	333.4	1.010
44	13	4	11	8.414	336.5	1.009
45	12	5	17	8.494	339.8	1.010
46	12	5	14	8.557	342.3	1.007
47	13	4	7	8.621	344.8	1.007
48	13	4	6	8.716	348.6	1.011
49	14	4	14	8.786	351.4	1.008
50	14	4	11	8.864	354.6	1.009
51	14	4	9	8.944	357.8	1.009
52	13	5	16	9.012	360.5	1.008
53	13	5	13	9.085	363.4	1.008
54	13	5	11	9.154	366.2	1.008
55	13	5	9	9.255	370.2	1.011
56	13	5	8	9.325	373.0	1.008
57	13	5	7	9.413	376.5	1.009
58	14	4	4	9.500	380.0	1.009
59	14	5	13	9.585	383.4	1.009
60	14	5	11	9.654	386.2	1.007
61	15	4	5	9.750	390.0	1.010
62	14	5	8	9.825	393.0	1.008
63	14	5	7	9.914	396.6	1.009

Table 5.12-2: The DC output voltages and the linearity characteristics with different digital settings.

Digital Settings	Output Voltages	LSB_{error} (%)	$\frac{R_n}{R_{total}}$ (%)	$\frac{R_n}{R_{n-1}}$
0	-4.945800		1.084003	0.000000
1	-4.887300	6.994959	1.169996	1.079329
2	-4.828600	0.529624	1.174002	1.003423
3	-4.771200	3.064963	1.147995	0.977848
4	-4.713300	0.005135	1.157999	1.008714
5	-4.654000	1.528767	1.186008	1.024188
6	-4.590700	5.816428	1.265993	1.067440
7	-4.528100	1.964485	1.252003	0.988949
8	-4.465300	0.552609	1.255999	1.003192
9	-4.402400	0.710925	1.258001	1.001595
10	-4.338500	0.706895	1.278000	1.015897
11	-4.274600	0.868994	1.278000	1.000000
12	-4.212200	3.196212	1.247997	0.976524
13	-4.146900	3.738266	1.306000	1.046476
14	-4.078400	3.988960	1.370001	1.049005
15	-4.009900	0.868994	1.370001	1.000000
16	-3.945000	.078626	1.298003	0.947447
17	-3.876500	4.629601	1.370001	1.055468
18	-3.810400	4.342428	1.321998	0.964961
19	-3.741600	3.180370	1.375999	1.040849
20	-3.672500	0.436491	1.382003	1.004363
21	-3.603000	0.295404	1.389999	1.005786
22	-3.534800	2.723382	1.363997	0.981294
23	-3.464900	1.602259	1.398001	1.024929
24	-3.391100	4.661992	1.476002	1.055795
25	-3.319100	3.286904	1.440001	0.975609
26	-3.246800	0.456049	1.445999	1.004166
27	-3.172900	1.324812	1.478000	1.022130
28	-3.098800	0.600670	1.482000	1.002707
29	-3.024300	0.334106	1.489997	1.005396
30	-2.951100	2.598609	1.464000	0.982552
31	-2.874700	3.464671	1.528001	1.043717
32	-2.795900	2.244969	1.575999	1.031413

Table 5.12-2, con't

Digital Settings	Output Voltages	LSB_{error} (%)	$\frac{R_n}{R_{total}}$ (%)	$\frac{R_n}{R_{n-1}}$
33	-2.719100	3.384828	1.536002	0.974621
34	-2.641900	0.352907	1.543999	1.005206
35	-2.562700	1.699291	1.584001	1.025908
36	-2.463200	24.539461	1.989999	1.256312
37	-2.383600	20.695053	1.592002	0.800001
38	-2.302500	0.998913	1.622000	1.018843
39	-2.218900	2.186898	1.672001	1.030827
40	-2.129400	6.126976	1.789999	1.070573
41	-2.048200	10.061960	1.624002	0.907264
42	-1.964300	2.426908	1.677997	1.033248
43	-1.870600	10.710330	1.874001	1.116808
44	-1.785200	9.650138	1.708000	0.911419
45	-1.699400	0.404608	1.716001	1.004685
46	-1.610300	2.943681	1.782000	1.038461
47	-1.524000	3.984339	1.725998	0.968573
48	-1.437000	0.064789	1.740000	1.008113
49	-1.347000	2.549336	1.800001	1.034483
50	-1.256800	0.648802	1.803999	1.002221
51	-1.166500	0.758939	1.806002	1.001110
52	-1.076200	0.869124	1.805999	0.999999
53	-0.982000	3.412474	1.884000	1.043190
54	-0.887700	0.763808	1.885999	1.001061
55	-0.793200	0.658716	1.890000	1.002121
56	-0.698400	0.554298	1.896000	1.003175
57	-0.603500	0.764411	1.898000	1.001055
58	-0.509600	1.913564	1.878000	0.989463
59	-0.410000	5.148500	1.992000	1.060702
60	-0.310600	1.068057	1.988000	0.997992
61	-0.213700	3.362198	1.938000	0.974849
62	-0.113800	2.200063	1.998000	1.030960
63	-0.013300	0.273613	2.010000	1.006006

Final $dR/R=0.266000$

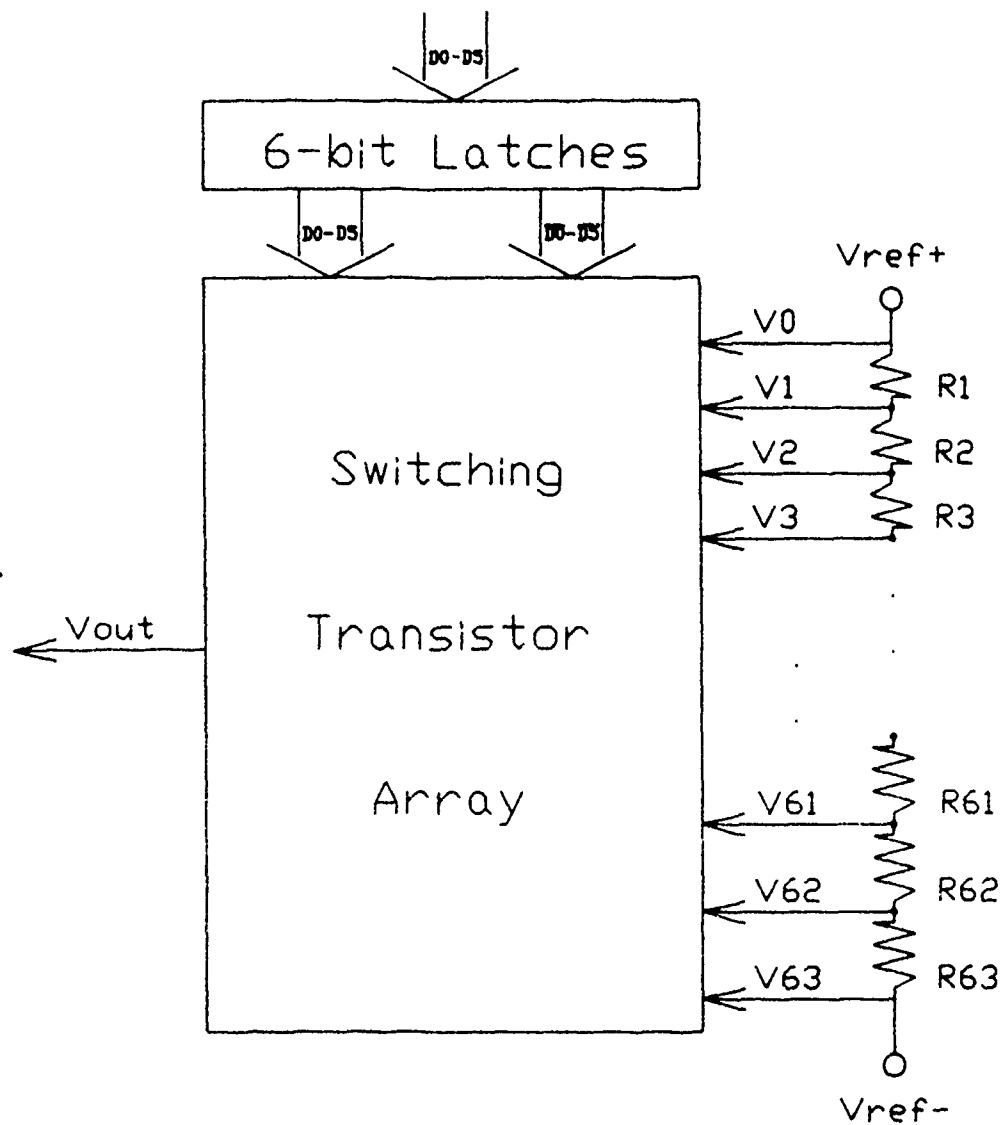


Fig. 5.12-1: The block diagram of the small log DAC.

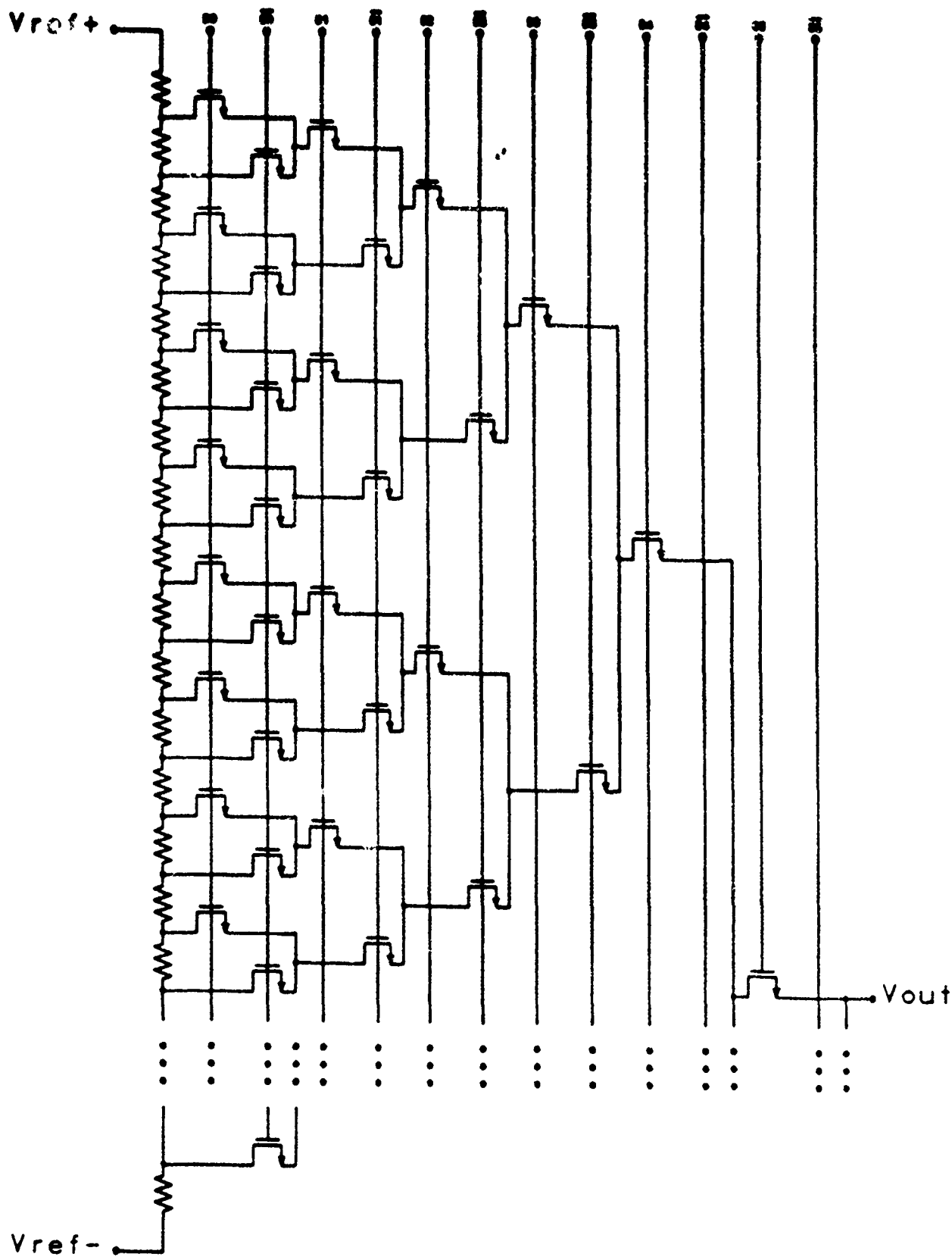


Fig. 5.12-2: The circuit schematic of the small log DAC.

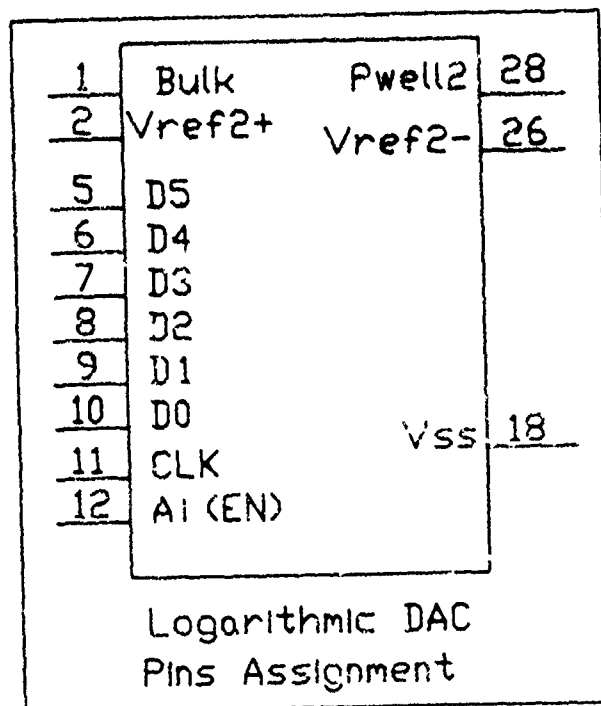


Fig. 5.12-3: Logarithmic DAC pins assignment.

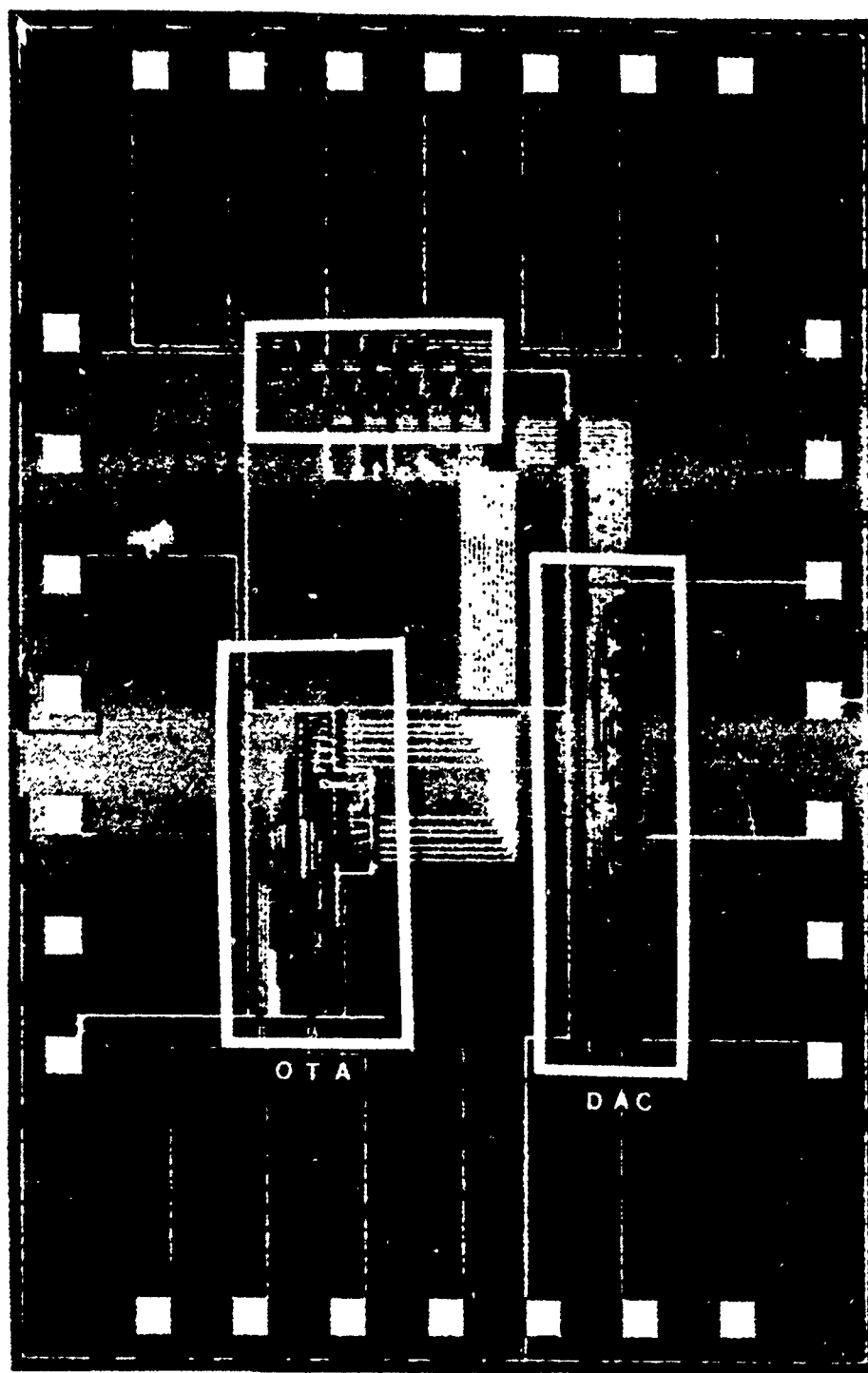


Fig. 5.12-4: The die photograph of the small log DAC test chip.

The above value is very close to the ideal incremental ratio=1.01. However, it can also be observed that the average LSB error is somewhat larger than the small linear DAC's. Note that the LSB error shown in TABLE DAC3.1 is defined differently from the linear DAC's by the following:

$$\text{LSB}_{\text{error}}[n] \triangleq \left[\frac{\left(\frac{R_N}{R_{n-1}} \right) - \left(\frac{R_N}{R_{N-1}} \right)_{\text{average}}}{\left(\frac{R_N}{R_{N-1}} \right)_{\text{average}}} \right] \times 100\% \quad (5.12 - 2)$$

where $\frac{R_N}{R_{N-1}}_{\text{average}}$ has been defined previously. The measured error is plotted in Fig. 5.12-5.

It can be observed that the errors are unusually large at digital inputs 36 and 37. These unusual points are expected to be fixed in the next fabrication. Moreover, the offset voltage in the Small DAC, described in Section 5.9, was not found in the Logarithmic DAC, although their layout designs are essentially the same.

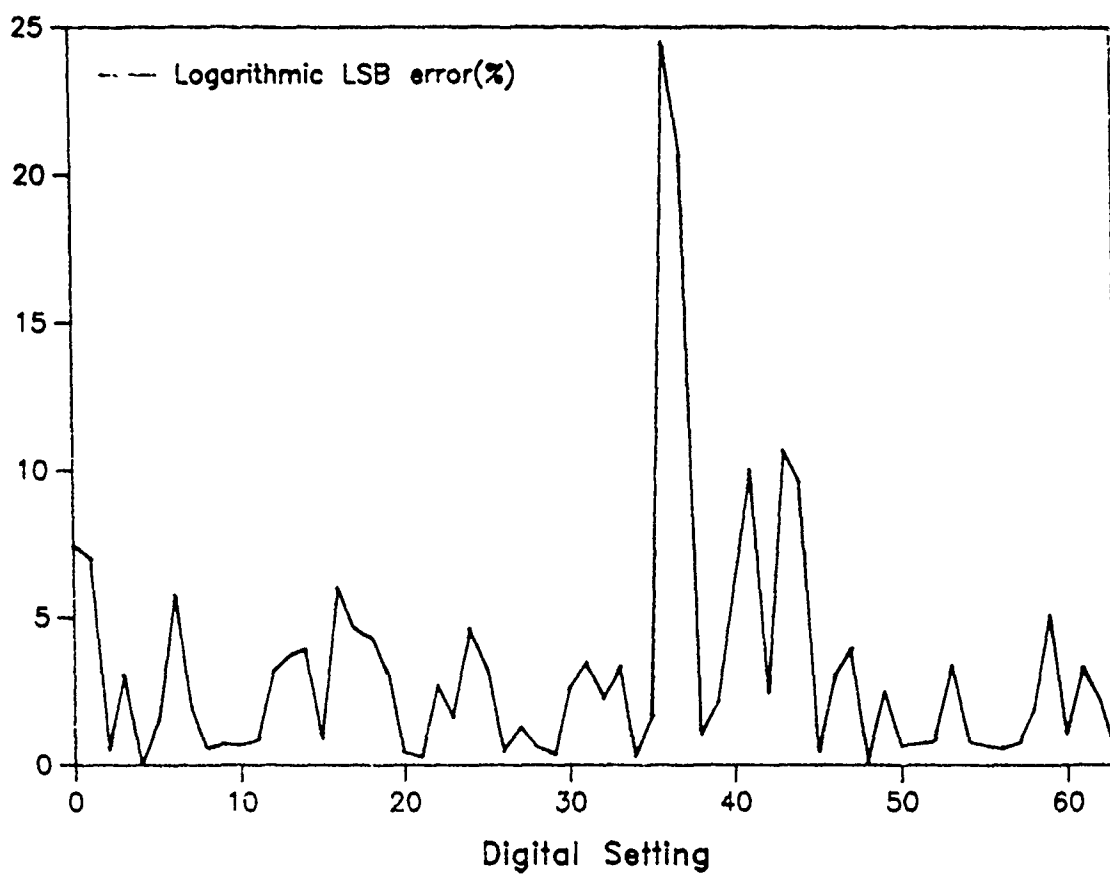


Fig. 5.12-5: DAC performance analysis of the small log DAC.

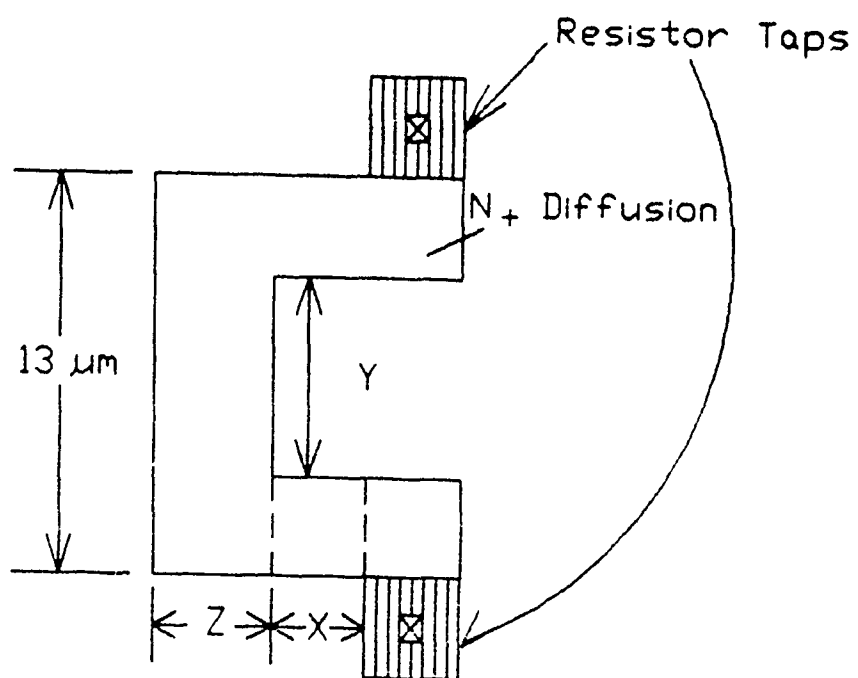


Fig. 5.12-6: Definitions of X, Y, and Z in Table 5.12-1.

5.13 Performance Detector based upon S/H-2

Name: S/H-2
MOSIS ID: 23496
Fab. ID: M76LLA-1
Technology: CBPE — MOSIS $3\mu\text{m}$ CMOS double-poly p-well process
Fabricated: July - August 1987
Chip Size: $7900\mu\text{m} \times 9200\mu\text{m}$ (72.68mm^2)
Active Area: $235\mu\text{m} \times 1940\mu\text{m}$ ($.45\text{mm}^2$)
Number of Pads: 11
Packaging: 64 pin package
Status: Currently being tested.

Name: DCASP-2
MOSIS ID: 23528
Fab. ID: M72LJH-1
Technology: CBPE — MOSIS $3\mu\text{m}$ CMOS double-poly p-well process
Fabricated: July - August 1987
Chip Size: $2300\mu\text{m} \times 3400\mu\text{m}$ (7.82mm^2)
Active Area: $235\mu\text{m} \times 1940\mu\text{m}$ ($.45\text{mm}^2$)
Number of Pads: 11
Packaging: 28 pin package
Status: Currently being tested.

Purpose:

This Performance Detector is a pair of Sample/Hold-2 cells as discussed in Section 2.2.2.3c, controlled by a common sampling control logic and external trigger to simultaneously sample the excitation and response signals. The purpose of this test chip is to dynamically characterize the performance and performance limitations of the S/H-2 based Performance Detector architecture and its associated physical design and to accurately sample high-frequency large-amplitude signals in the presence of circuit non-idealities such as switch feed-through, voltage dependent switch "on" resistance, statistical process variations, etc..

The focus of this test vehicle is to characterize the analog performance of an individual S/H-2 cell, and the matching characteristics between two adjacent S/H-2 cells. This test structure does not provide for multiple samples of the excitation and response signals nor does it provide the complex control and interface logic necessary to multiplex an external A/D. Only the minimum necessary control logic has been provided on-chip so as to not preclude the characterization of the analog portion of this architecture.

Description:

This test-cell was included on two different IC's: (1) the S/H test chip (MOSIS ID:

23496) and (2) DCASP-2 chip (MOEIS ID: 23528). Pin-outs and a die photograph of the S/H test cell are shown in Figs. 5.13-1 and 5.13-2, respectively. This structure requires four bias voltages and two bias currents as follows:

- | | |
|-----------------------------------|----------------------------------|
| (1) $V_{DD} = +5V$ | (2) $Bulk = +5V$ |
| (3) $V_{SS} = -5V$ | (4) $Gnd = 0V$ |
| (5) $I_{bias}/R_{esp} = 100\mu A$ | (6) $I_{bias}/E_{xc} = 100\mu A$ |

The two analog inputs, V_i/E_{xc} and V_i/R_{esp} are simultaneously sampled on the rising edge of the $\pm 5V$ digital signal *SampleBar*, with the resultant sampled and held output voltages brought external via the analog outputs, V_o/E_{xc} and V_o/R_{esp} . This is illustrated in the block diagram shown in Fig. 5.13-3.

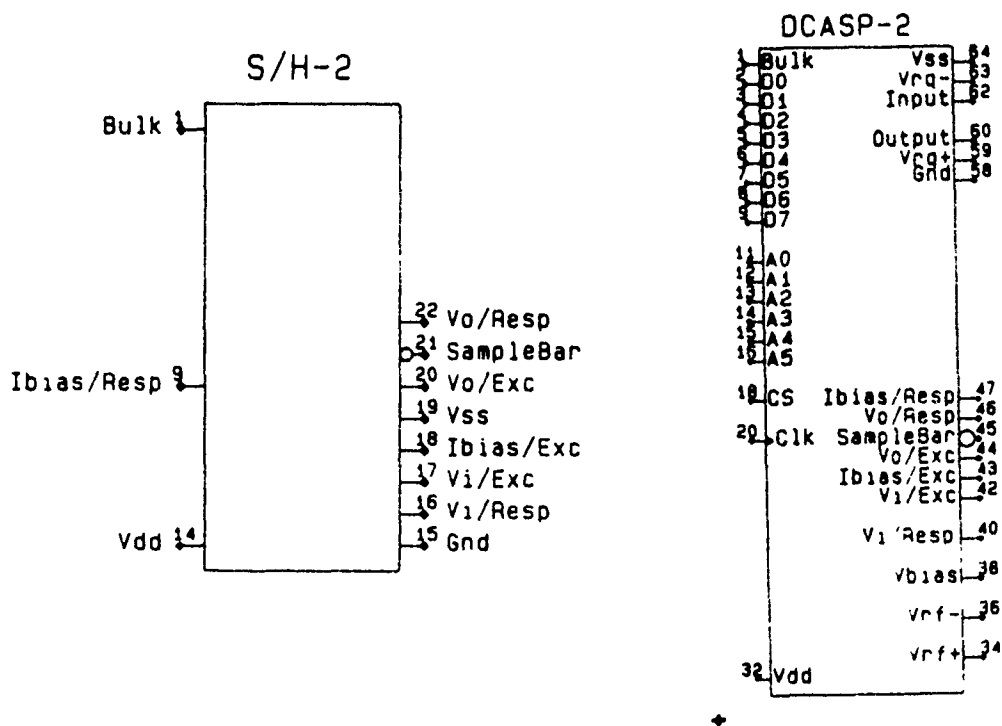
In this figure, it is easy to see how the excitation signal, V_i/E_{xc} and the response signal, V_i/R_{esp} are sampled at the same instances, via the common or shared control logic, which is shown in its entirety in Fig. 5.13-4 with its associated devices sizes listed in Table 5.13-1. The circuit schematic, timing diagram and equivalent circuits for the S/H-2 cell are provided in Fig. 5.13-5, and its device sizes contained in Table 5.13-2. A more detailed discussion of the functionality of this design is provided in Section 2.2.2.3c.

The poly resistors R_{ext} of value $2.5k\Omega$ was added to this test vehicle to limit the external capacitive load seen by the load sensitive output node of the S/H. If this capacitive load is too large, then it drastically reduces the phase margin of the S/H OpAmp and may cause oscillation. The resistor R_{ext} in series with a typical load capacitance of $10 - 15pF$ produces a pole at $\approx 5MHz$, thus for frequencies near the bandwidth of this OpAmp ($30MHz$), this RC load looks much more resistive than capacitive. Furthermore this additional pole associated with the output signal slightly increases the settling-time required for the output voltage to settle to 0.1% of its final sample and held voltage level, but does not at all effect the accuracy of the voltage sampling.

The purpose of the control logic circuitry is to generate the *Track*, *Hold* and *Sample* signals which control the analog switches of the S/H-2 circuit. The externally provided trigger, *SampleBar* is inverted by I_1 , thus generating the internal control line, *Sample*. A delay in excess of $10\eta sec$ is added to the *Sample* signal via the inverters I_2 , I_3 and the $1pF$ capacitor. This delayed signal and its compliment are logically equivalent to the control signals *Track* and *Hold*, respectively. The gates, I_4 through I_8 are sized so that the gate delay due to I_4 and I_5 is equal to that of I_6 , I_7 and I_8 . Thus signals, *Track* and *Hold* will change simultaneously.

Test Plan:

- (1) Functional Test — For this test, tie the V_i/E_{xc} and V_i/R_{esp} signals together and connect to a sinusoidal function generator of frequency f_o and amplitude V_m , as shown in



(a) S/H test-chip (b) DCASP-2 chip

Fig. 5.13-1. Pin-outs for S/H-2 test vehicles.

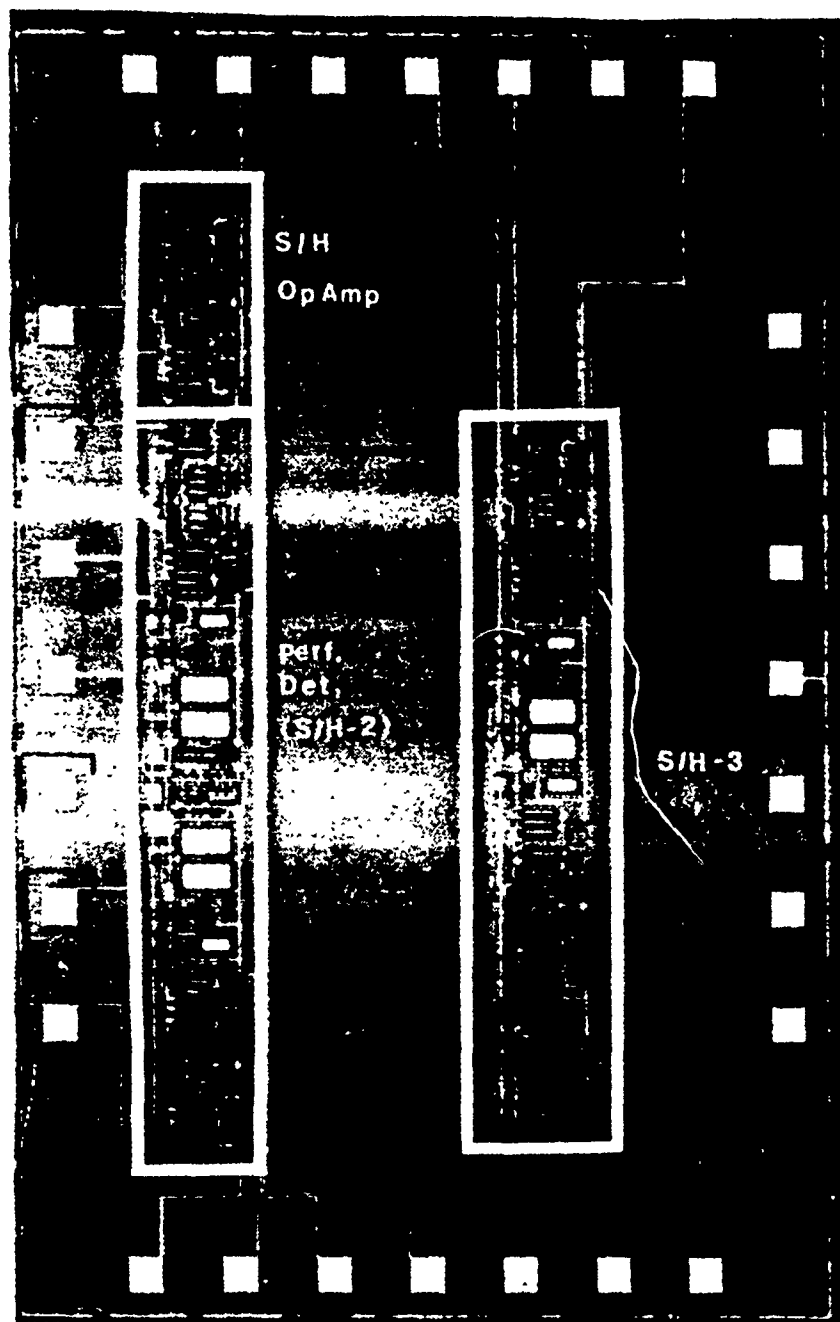


Fig. 5.13-2. Die photograph of S/H test cell containing a Performance Detector based up on two phase-correlated S/H-2 cells as shown in the lower left hand portion of the photograph and labeled "Perf. Det".

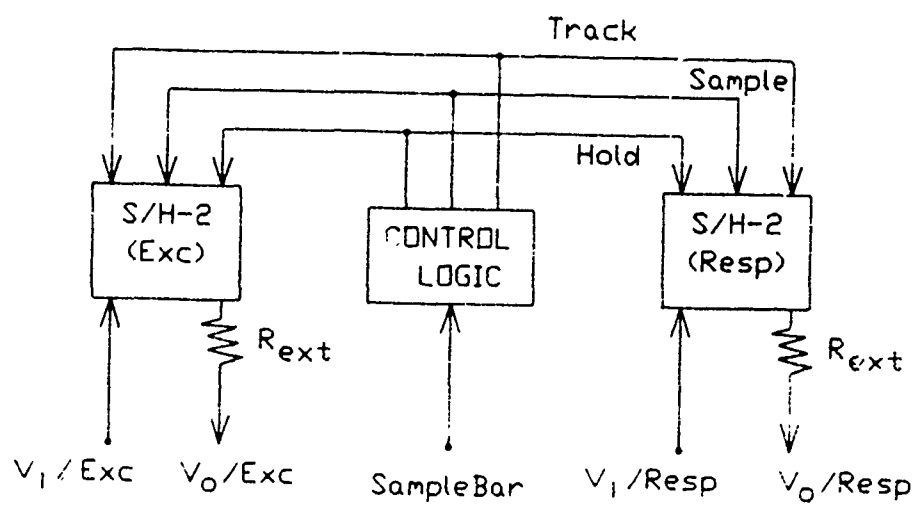


Fig. 5.13-3. Block diagram of S/H-2 test circuit.

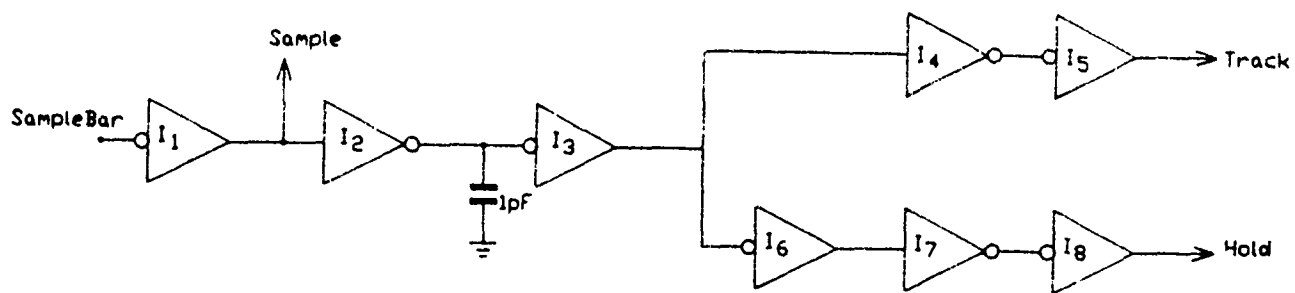
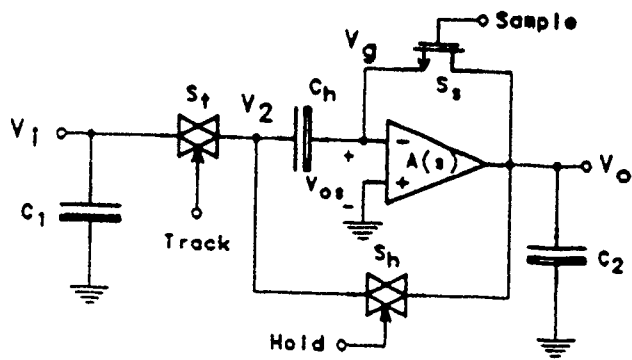


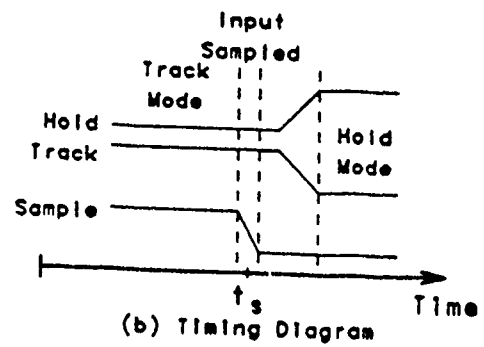
Fig. 5.13-4. S/H-2 control logic circuit schematic.

Table 5.13-1. Devices sizes for S/H-2 control logic of Fig. 5.13-4.

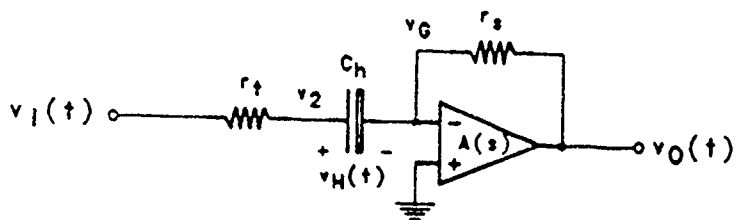
Device	P-channel		N-channel	
	<i>W</i>	<i>L</i>	<i>W</i>	<i>L</i>
<i>I</i> ₁	15μm	3μm	7μm	4μm
<i>I</i> ₂	7μm	7μm	7μm	4μm
<i>I</i> ₃	15μm	3μm	7μm	4μm
<i>I</i> ₄	15μm	3μm	7μm	4μm
<i>I</i> ₅	30μm	3μm	14μm	4μm
<i>I</i> ₆	30μm	3μm	14μm	4μm
<i>I</i> ₇	30μm	3μm	14μm	4μm
<i>I</i> ₈	30μm	3μm	14μm	4μm



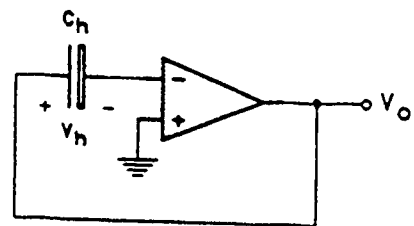
(a) Circuit Schematic



(b) Timing Diagram



(c) Track Mode Equiv. Circuit



(d) Hold Mode Equiv. Circuit

Fig. 5.13-5. S/H-2

Table 5.13-2. Device sizes and component values for S/H-2 circuit schematic of Fig. 5.13-5.

Component	n-channel		p-channel		Value
	<i>W</i>	<i>L</i>	<i>W</i>	<i>L</i>	
<i>S_s</i>	12 μm	3 μm			
<i>S_i</i>	9 μm	3 μm	23 μm	3 μm	
<i>S_n</i>	9 μm	3 μm	23 μm	3 μm	
<i>C₁</i>					5pF
<i>C₂</i>					5pF
<i>C_h</i>					1.5pF

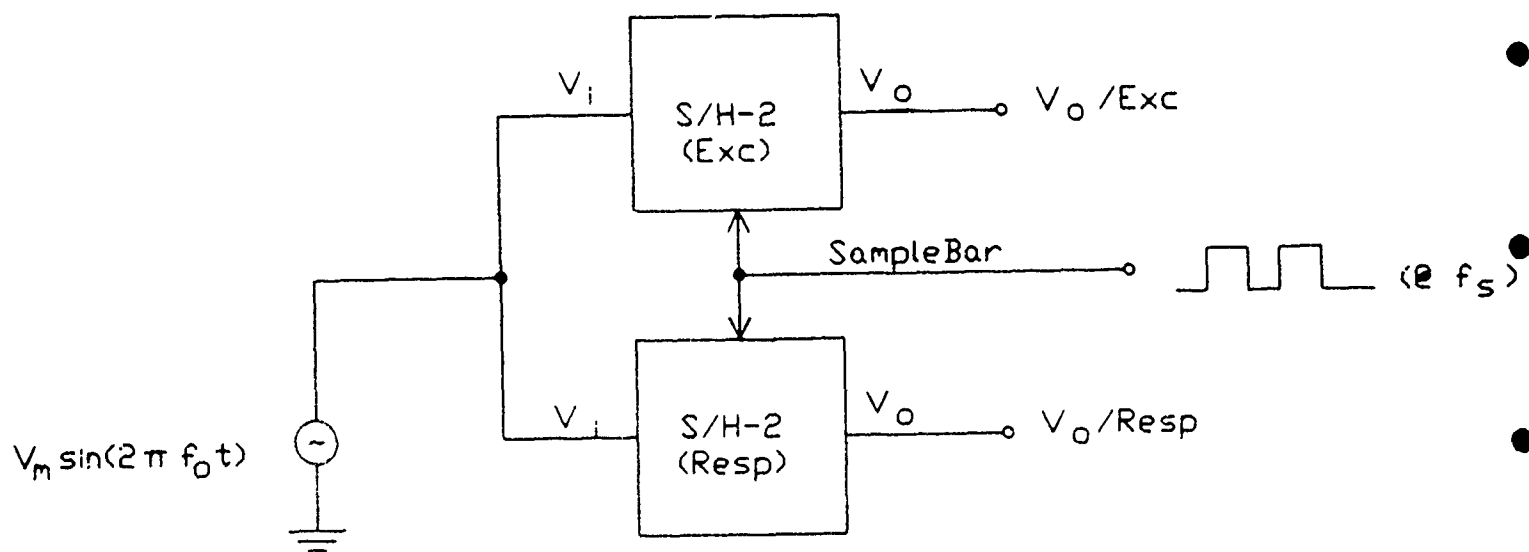


Fig. 5.13-6. S/H-2 functional test setup.

f_s , such that f_s is approximately 10 – 20 times greater than f_o . Now with the system in this configuration, perform the following tests.

Input a low-frequency low-amplitude sinusoid ($\approx 1V_{p-p} @ 10kHz$), display the input signal and one of the two sampled output waveforms (V_o/Exc or $V_o/Resp$) on a high-frequency oscilloscope, triggered off of the *SampleBar* signal. V_o should resemble an amplitude varying square-wave waveform, toggling between ground when *SampleBar* is high and the S/H is in track-mode, and various amplitudes as a function of the time-sampled input signal $V_i(t)$ when *SampleBar* is low and the S/H is in the hold-mode. The amplitude of the square-wave during the hold-mode state should follow track the input signal up and down. From this continuous-time display, the following characteristics should be examined.

- (a) Check the phase margin of the S/H OpAmp by looking for ringing or oscillation present in the step response on each of the transitions between ground and the sampled-output voltage. In the S/H application, the S/H OpAmp is loaded by a predominantly capacitive load, thus this test setup gives us the capability of examining the "in use" S/H OpAmp for marginal phase margins associated with either a ringing effect in the step response, or possibly even oscillations. This aspect of the S/H OpAmp is difficult to measure with the stand-alone OpAmp since it is difficult to control this load capacitance, as discussed in Section 5.15.
- (b) With the *SampleBar* superimposed on V_i , visually compare the instantaneous value of $V_i(t)$ at the instances the rising edge of *SampleBar* crosses 0V, with the corresponding sampled value V_o . These two values should tightly track each other over the complete signal swing. Check for any obvious offset or gain errors between these two instantaneous values.
- (c) To determine the range of operation, increase the the input amplitude, until an appreciable distortion between the sampled output V_o and the theoretical time-sampled input V_i becomes apparent. The expected range of operation is $\pm 2V$.
- (d) Increase the input frequency and sample frequency until the sampled value V_o quits tracking the input waveform. No severe limitations should be observable for frequencies less than 1MHz. Above this frequency, the instrumentation is of question. Note the sample frequency f_s can not be increased much above 1MHz, because the sampled output signal must be brought external and the associated transients must have ample time to die out. This test is very subjective but some insight may be gained.
- (e) Remove the input signal from channel-A of the oscilloscope and replace with the other sampled output waveform. Now by subtracting trace A from trace B, the two sample/holds can be compared for basic match characteristics. The two signals should be almost identical. Look for offset problems characterized by a DC shift in the subtracted sampled values; gain problems characterized

by the subtracted waveform still slightly tracking the original input waveform; and/or timing-jitter problems characterized by randomly varying spikes near the sampling transition.

- (2) DC Characterization — Once again tie the two input signals V_i/Exc and $V_i/Resp$ together and attach an accurate DC voltage source, and DVOM to this input, as shown in Fig. 5.13-7. Connect a pulse generator of frequency f_s to the *SampleBar* pin. Now with this test setup, the output waveform should be a pulse waveform jumping between the DC reference and ground.
 - (a) Vary the DC reference between $\pm 5V$ and record the associated sampled output voltage for both of the outputs. These measurements should be concentrated between $-2V$ and $+2V$.
 - (b) Decrease the sampling rate to very low-frequency and measure the slope of the sampled output voltage, V_o . The sampled output should droop because of the charge on the S/H leaking off of the hold-capacitor.
- (3) Dynamic Characterization — Once again tie the two inputs together and input a triangle wave of amplitude $\pm 2.5V$. Connect one of the outputs to an external A/D with references set at exactly $\pm 2V$, and with the digital output word connected to data collection hardware as shown in Fig. 5.13-8. Also shown here is the *SampleBar* pin driven by a pseudo random pulse generator. The basic idea of this test structure is that for an ideal sample/hold and test setup, the probability distribution function of the quantized samples is uniformly distributed except at the end points. Thus for a series of independent random samples, the histogram of number of samples collected for a specific digital word, should be ideally flat. Any deviation from this can then be attributed to differential linearity problems of the S/H under test. This concept is illustrated in Fig. 5.13-9. For more information on this dynamic characterization technique, see [5.13-1]. The exact specifics of this test setup will be divulged at a later date.
- (4) Application Specific Performance Detector Testing — In this test, the Performance Detector should be used to measure a known transfer function, via the discrete-time sampling algorithm, discussed in Section 2.2.1.1. The specifics of this test setup, will be discussed at a later date.

Experimental Results:

This structure is still being tested, but the results so far indicate the design is operational as detailed below. A minor layout error was also detected. This error was that pin 9 ($I_{bias}/Resp$) of the S/H-2 test cell (MOSIS ID: 23537) was not connected; and thus only the excitation S/H is operational on this test vehicle. This is not severe problem, since this Performance Detector was repeated on the DCASP-2 test structure (MOSIS ID: 23496),

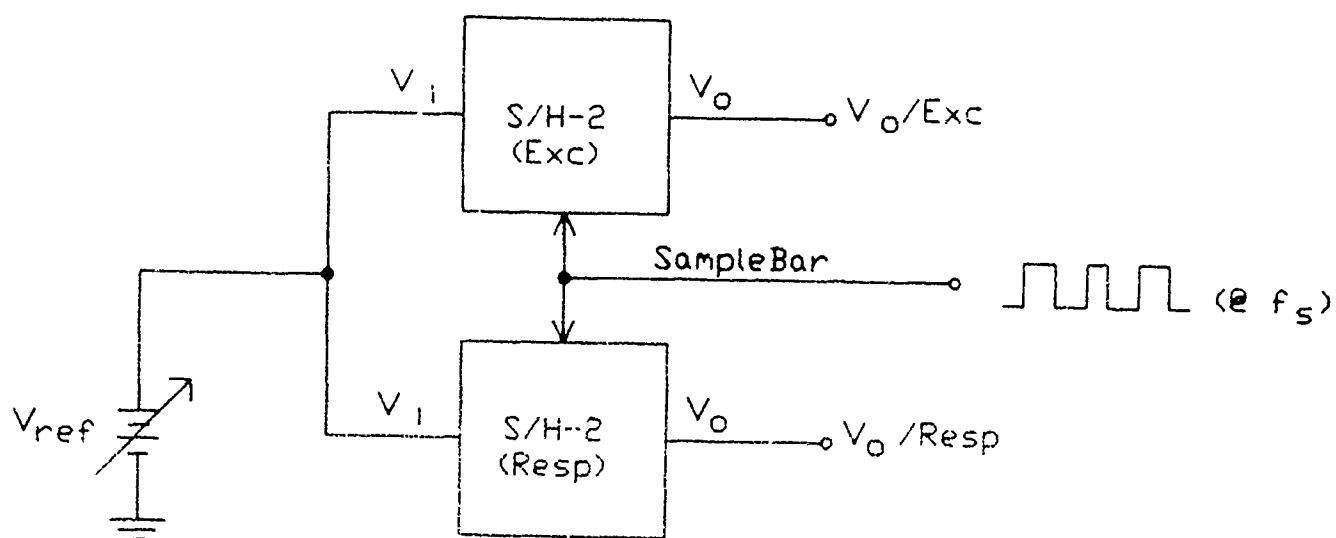


Fig. 5.13-7. S/H-2 DC characterization test setup.

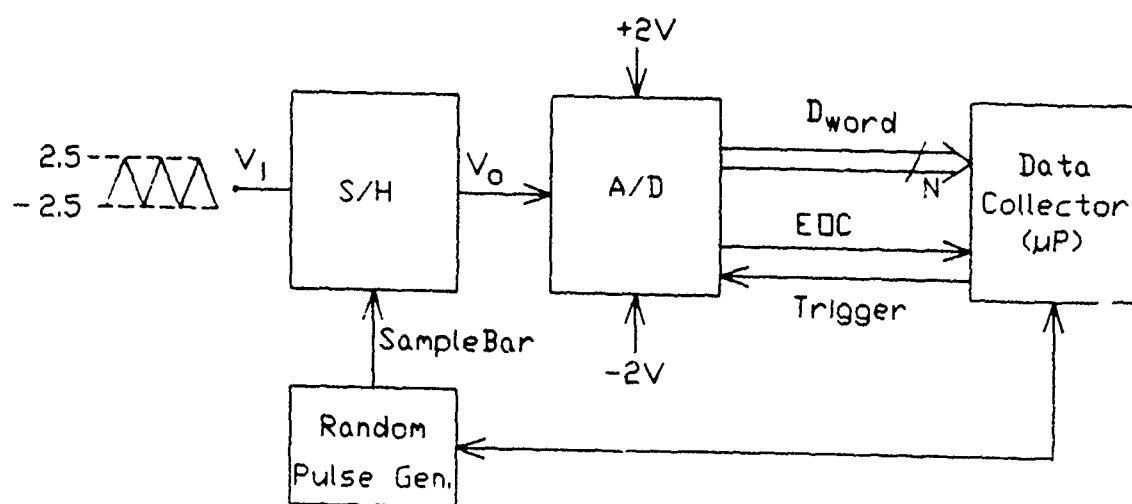
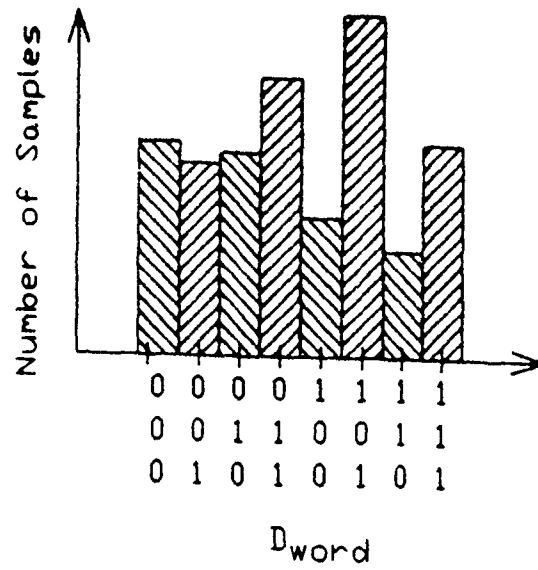
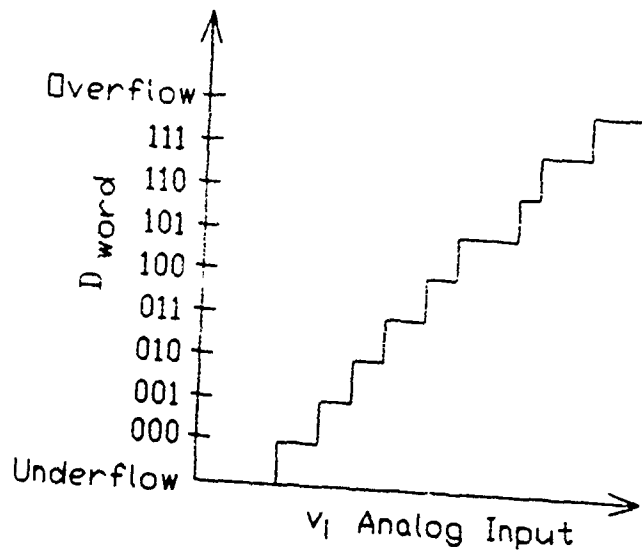


Fig. 5.13-8. S/H-2 dynamic characterization test setup.



(a) Histogram



(b) Transfer Characteristics

Fig. 5.13-9. Example dynamic characterization test results.

but requires a digital controller to configure DCASP-2 to patch externally provided excitation and response signals directly to the Performance Detector. This complicates testing, but should not impede characterization.

To date, only the functional test (item (1) of the Test Plan) has been completed. In the functional test the following results can be reported.

(1) Based upon simulation results as summarized in Table 2.2-21 and the preliminary test results presented in Section 5.15, the high-frequency S/H OpAmp is borderline stable with a predicted 18° phase margin. The results seen thus far implies that indeed the OpAmp is stable, but borderline, as supported by the following observations.

- (a) In the track mode, there was no observable oscillation on the output of the OpAmp.
- (b) The step response generated by the sharp transition to hold mode, exhibited a definite ringing effect, indicating a low phase margin.
- (c) The sample and held outputs correlated with the original input excitation signal, and thus indicating that the current OpAmp design did not inhibit the low-frequency operation of the S/H.

These results will be quantified when a low-capacitance high input-impedance active probe is made available.

(2) The digital control logic is operational since it is obvious that the Sample/Hold switches between track mode, where the output of the OpAmp is near zero, and hold mode, where the output voltage is approximately the sample and held voltage of the input signal at a given time instance.

(3) The analog portion of the S/H seems to be operational based upon the following observations.

- (a) For a DC input signal the amplitude of the sampled output signal closely approximated the amplitude of the input signal.
- (b) The sampled output signal showed no appreciable errors in sampling an input voltage between $\pm 2V$.
- (c) Based upon visual inspection and for a sample frequency much larger than the input signal frequency the linear interpolation between sample points nearly approximated the input signal.

These preliminary results shown here, by no means accurately characterize the Per-

5.14 Single S/H-3 test cell

Name: S/H-3
MOSIS ID: 23537
Fab. ID: M76LJG-3
Technology: CBPE — MOSIS 3 μ m CMOS double-poly p-well process
Fabricated: July - August 1987
Chip Size: 2300 μ m \times 3400 μ m (7.82mm²)
Active Area: 1825 μ m \times 290 μ m (0.53mm²)
Number of Pads: 14
Packaging: 28 pin package
Status: Currently being tested.

Purpose:

This test cell contains a single Sample/Hold-3 cell as discussed in Section 2.2.2.3d. The purpose of this test chip is to dynamically characterize the performance and performance limitations of the S/H-3 architecture and its associated physical design and to accurately sample high-frequency large-amplitude signals in the presences of circuit non-idealities. The performance of this archeticture will be compared to that of test cell S/H-2, as discussed in Section 5.13.

Description:

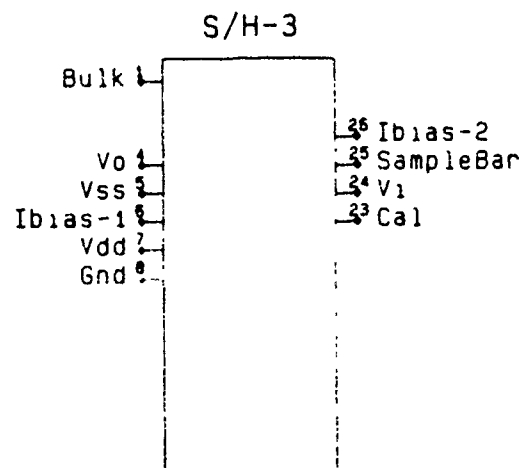
The pin-outs and die photograph for this test cell are shown in Figs. 5.14-1a and 5.14-1b. This structure requires four bias voltages and two bias currents as follows:

- | | |
|-----------------------------|-----------------------------|
| (1) $V_{DD} = +5V$ | (2) $Bulk = +5V$ |
| (3) $V_{SS} = -5V$ | (4) $Gnd = 0V$ |
| (5) $I_{bias-1} = 100\mu A$ | (6) $I_{bias-2} = 100\mu A$ |

The analog input signal, v_i is sampled on the rising edge of the trigger signal, *SampleBar* with its corresponding sample and held output signal then provided on v_o pin. The *Cal* is the calibration signal, as described in Section 2.2.2.3d, and should be pulsed prior to each sampling, with a pulse width of 1-10 μ sec. The block diagram for this test-circuit is shown in Fig. 5.14-2.

The control logic for this test cell is shown in Fig. 5.14-3 with its associated devices sizes listed in Table 5.14-1. The contents of the single sample and hold block are discussed in Section 2.2.2.3d and the associated circuit schematic, timing diagram and equivalent circuits appears in Fig. 5.14-4.

The purpose of the control logic circuitry is to generate the *Track*, *Hold* and *Sample* signals which control the analog switches of the S/H-3 circuit, as shown in the timing



+

Fig. 5.14-1a. Pin-outs for S/H-3 test vehicles.

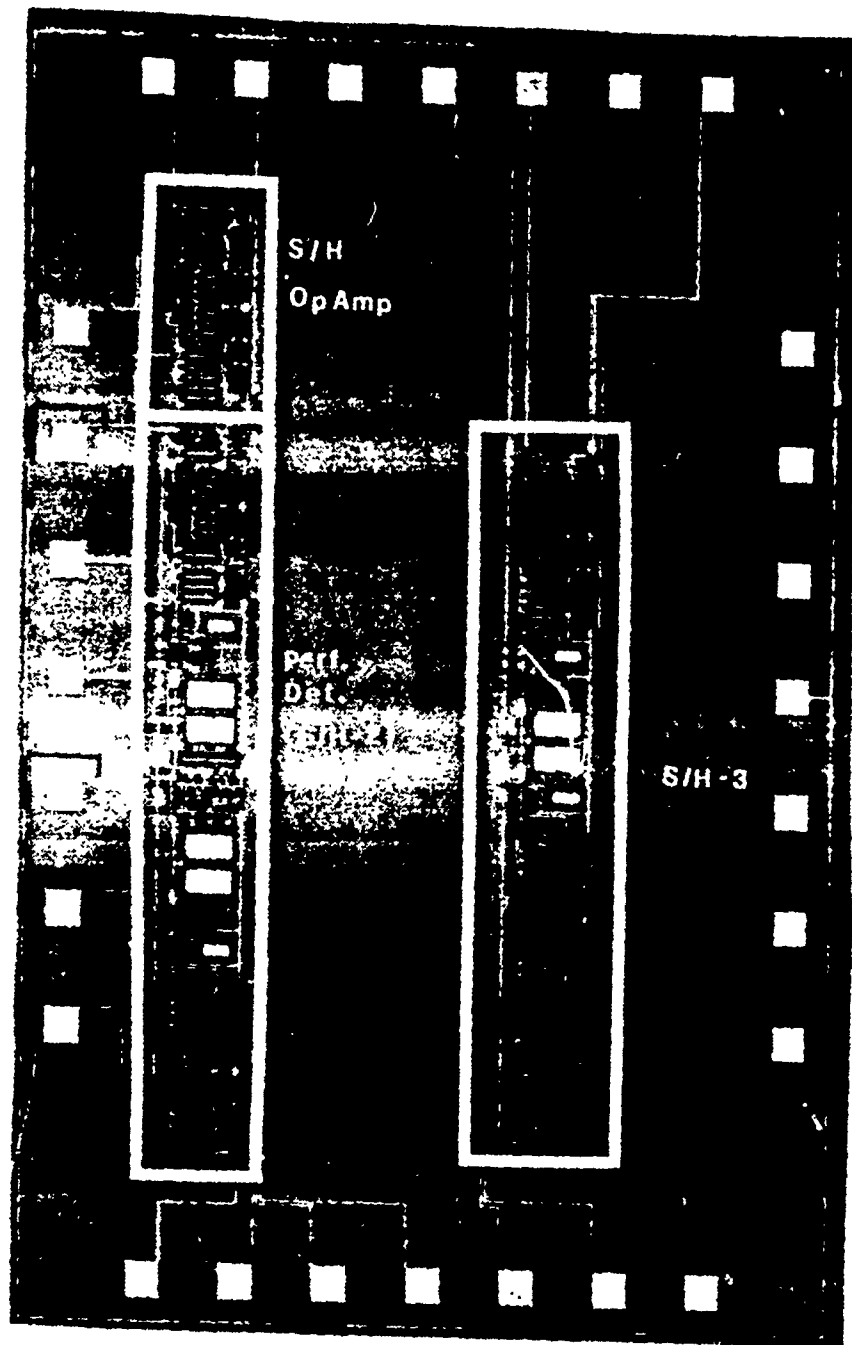


Fig. 5.14-1b. Die photograph of S/H test cell containing a single S/H-3 cell as shown in the right-hand portion of the photograph.

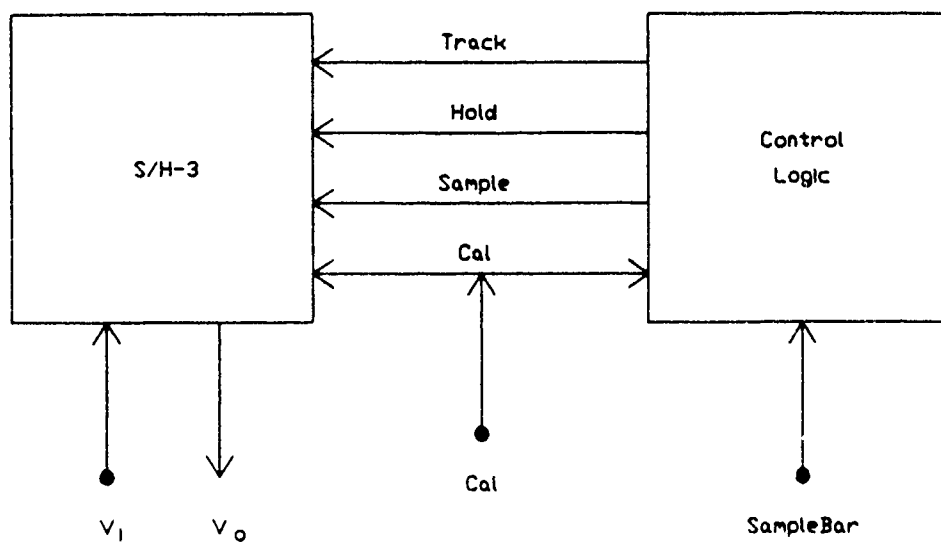


Fig 5.14-2. Block diagram of S/H-3 test circuit.

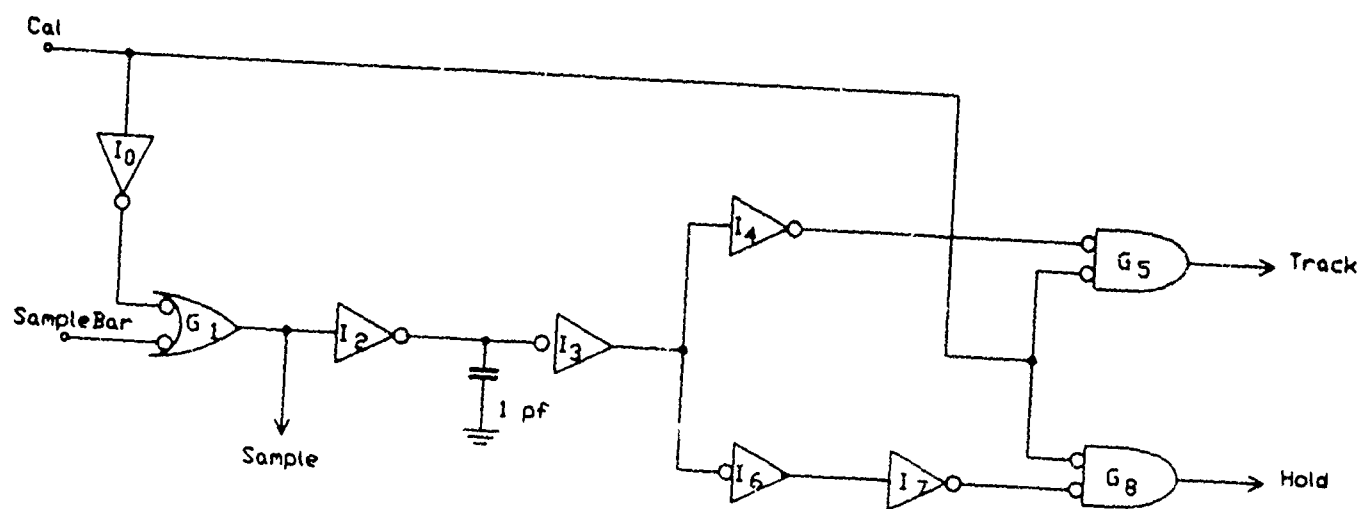
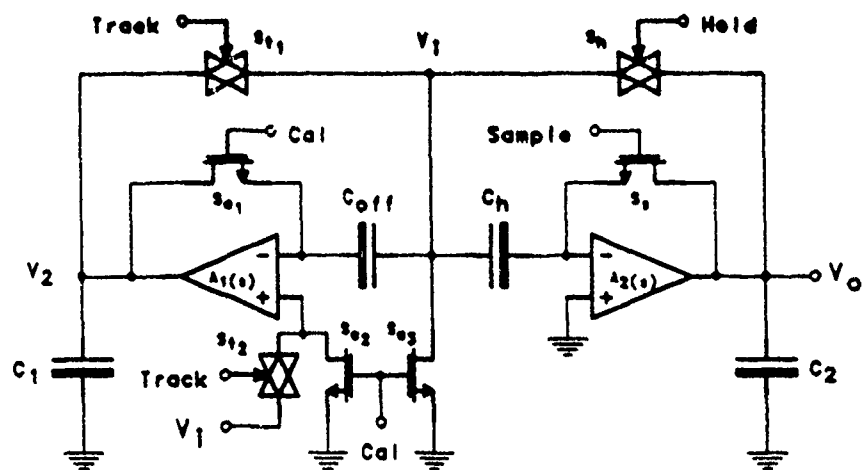


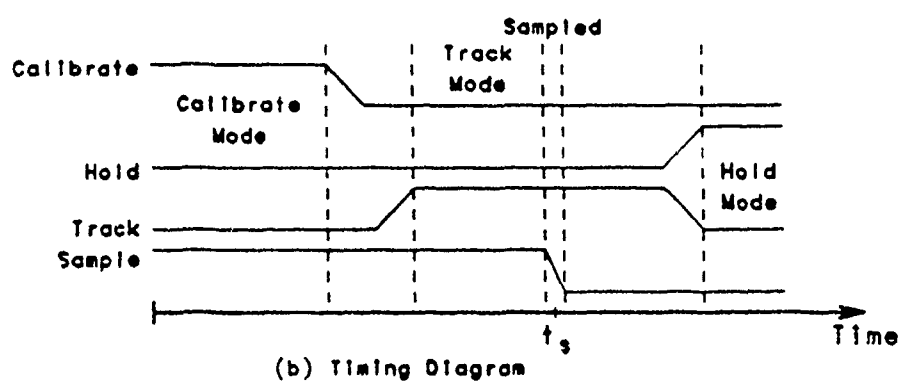
Fig. 5.14-3. S/H-3 control logic circuit schematic.

Table 5 14-1. Devices sizes for S/H-3 control logic of Fig. 5.14-3.

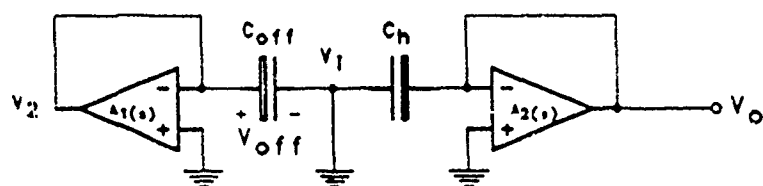
Device	P-channel		N-channel	
	<i>W</i>	<i>L</i>	<i>W</i>	<i>L</i>
I_0	15 μm	3 μm	7 μm	4 μm
G_1	15 μm	3 μm	15 μm	3 μm
I_2	7 μm	7 μm	7 μm	4 μm
I_3	15 μm	3 μm	7 μm	4 μm
I_4	15 μm	3 μm	7 μm	4 μm
G_5	45 μm	3 μm	14 μm	4 μm
I_6	30 μm	3 μm	14 μm	4 μm
I_7	30 μm	3 μm	14 μm	4 μm
G_8	45 μm	3 μm	14 μm	4 μm



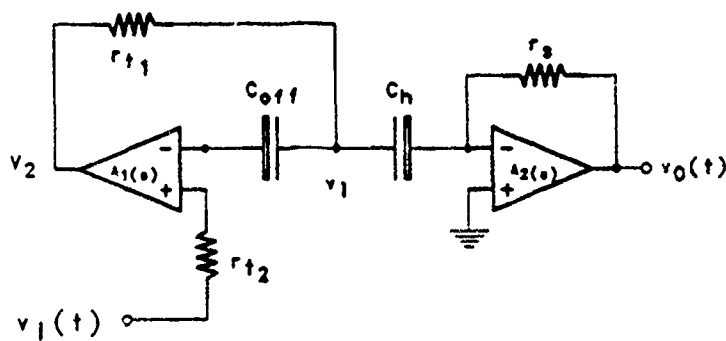
(a) Circuit Schematic



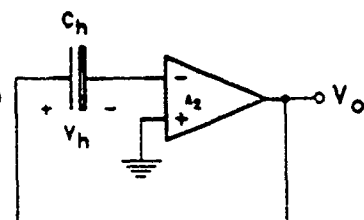
(b) Timing Diagram



(c) Calibrate Mode Equiv. Circuit



(d) Track Mode Equiv. Circuit



(e) Hold Mode Equiv. Circuit

Fig. 5.14-4. S/H-3.

diagram of Fig. 5.14-4, such that

$$\begin{aligned} \text{Sample} &\stackrel{\text{def}}{=} \overline{\text{SampleBar}} + \text{Cal} \\ \text{Track} &\stackrel{\text{def}}{=} \text{Track}_{old} \cdot \overline{\text{Cal}} = \text{Sample} \cdot \overline{\text{Cal}} \\ \text{Hold} &\stackrel{\text{def}}{=} \text{Hold}_{old} \cdot \overline{\text{Cal}} = \overline{\text{Sample}} \cdot \overline{\text{Cal}} \end{aligned} \quad (5.14 - 1)$$

Test Plan:

This circuit will undergo functionality tests, DC characterization and dynamic characterization, much like that described in Section 5.13, of this report.

Experimental Results:

Because of a layout error, this chip is currently non-functional. Pin 26 ($I_{bias}-2$) of the S/H-3 test cell (MOSIS ID: 23537) was not connected; and thus only by probing the chip and externally providing this bias current can this cell be tested. There is 75% probability of being able to successfully probe this chip. This architecture has been resubmitted for fabrication as described in Section 5.18.

After this circuit was resubmitted for fabrication, a second design or layout error was discovered, in which the internal signal *Sample* was unintentionally inverted. This error implies that the track and hold analog switches will be out of phase with the sampling analog switch, resulting in this circuit being non-operational. Laser-repair, probing and other repair techniques would be of no avail. A third submission will be made when silicon resources are available.

5.15 High-Frequency S/H OpAmp

Name:	S/H OpAmp
MOSIS ID:	23537
Fab. ID:	M76LJG-3
Technology:	CBPE — MOSIS $3\mu\text{m}$ CMOS double-poly p-well process
Fabricated:	July - August 1987
Chip Size:	$2300\mu\text{m} \times 3400\mu\text{m}$ (7.82mm^2)
Active Area:	$515\mu\text{m} \times 235\mu\text{m}$ (0.12mm^2)
Number of Pads:	7
Packaging:	28 pin package
Status:	Currently being tested.

Purpose:

This test cell is the S/H high-frequency OpAmp as documented in Fig. 5.15-1 and Table 5.15-1, and described in Section 2.2.2.3e. The overall limitations of the Performance Detector architecture depends on the performance of this challenging OpAmp design, which will be characterized by this test vehicle.

The primary characteristics of interest are bandwidth, phase margin and open loop gain, which are critical to the high-frequency operation of the sample and holds. Also the slew rate, dynamic range, offset voltage, settling time, and percent overshoot will be estimated from experimental results.

Description:

This test vehicle with pin-outs and die photograph shown in Figs. 5.15-2a and 5.15-2b requires three bias voltages, $V_{DD} = +5V$, $V_{SS} = -5V$, $Bulk = +5V$ and one bias current, $I_{bias} = 100\mu\text{A}$. The differential inputs are V^+ and V^- , and the corresponding output is V_o . V_o is typically loaded by an external load capacitor and any parasitic capacitance associated with the packaging and/or test configuration. The parasitics typically dominate the loading with typical parasitic capacitive loads anywhere in the range of $1 - 20\text{pF}$, depending on the specific test setup. The phase margin and the OpAmp stability depend on the capacitive loading seen by the output stage. The OpAmp was designed to be unity gain stable with a total capacitance load of $5 - 6\text{pF}$. In this OpAmp design, the parasitic poles and zeros are in close proximity to each other thus making the phase margin quite sensitive to small changes in either the parasitic pole or zero locations.

Test Plan:

- (1) Functional Test — The purpose of this test is to determine if the OpAmp is operational, to determine if the structure is unity gain stable and to make preliminary measurements of the 3dB bandwidth, open-loop gain and offset voltage.

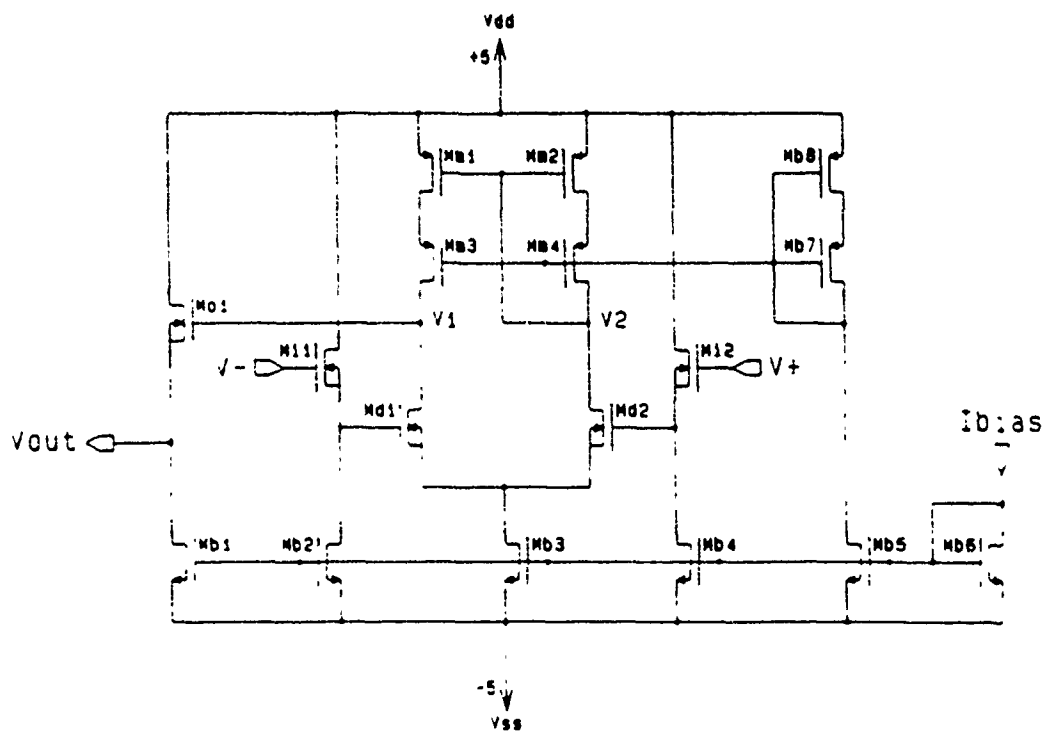


Fig. 5.15-1. S/H OpAmp circuit schematic.

Table 5.15-1. S/H OpAmp devices sizes for Fig. 5.15-1.

DEVICE	SIZE		DEVICE	SIZE	
	W	L		W	L
M_{i_1}, M_{i_2}	174μ	3μ	$M_{b_1}, M_{b_2}, M_{b_4}$	74μ	3μ
M_{d_1}, M_{d_2}	300μ	3μ	M_{b_3}	30μ	3μ
$M_{m_1}, M_{m_2}, M_{b_8}$	100μ	3μ	M_{b_5}, M_{b_6}	15μ	3μ
$M_{m_3}, M_{m_4}, M_{b_7}$	25μ	3μ	M_{o_1}	498μ	3μ

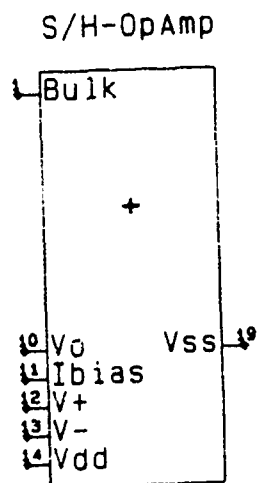


Fig. 5.15-2a. S/H high-frequency OpAmp pin-outs.

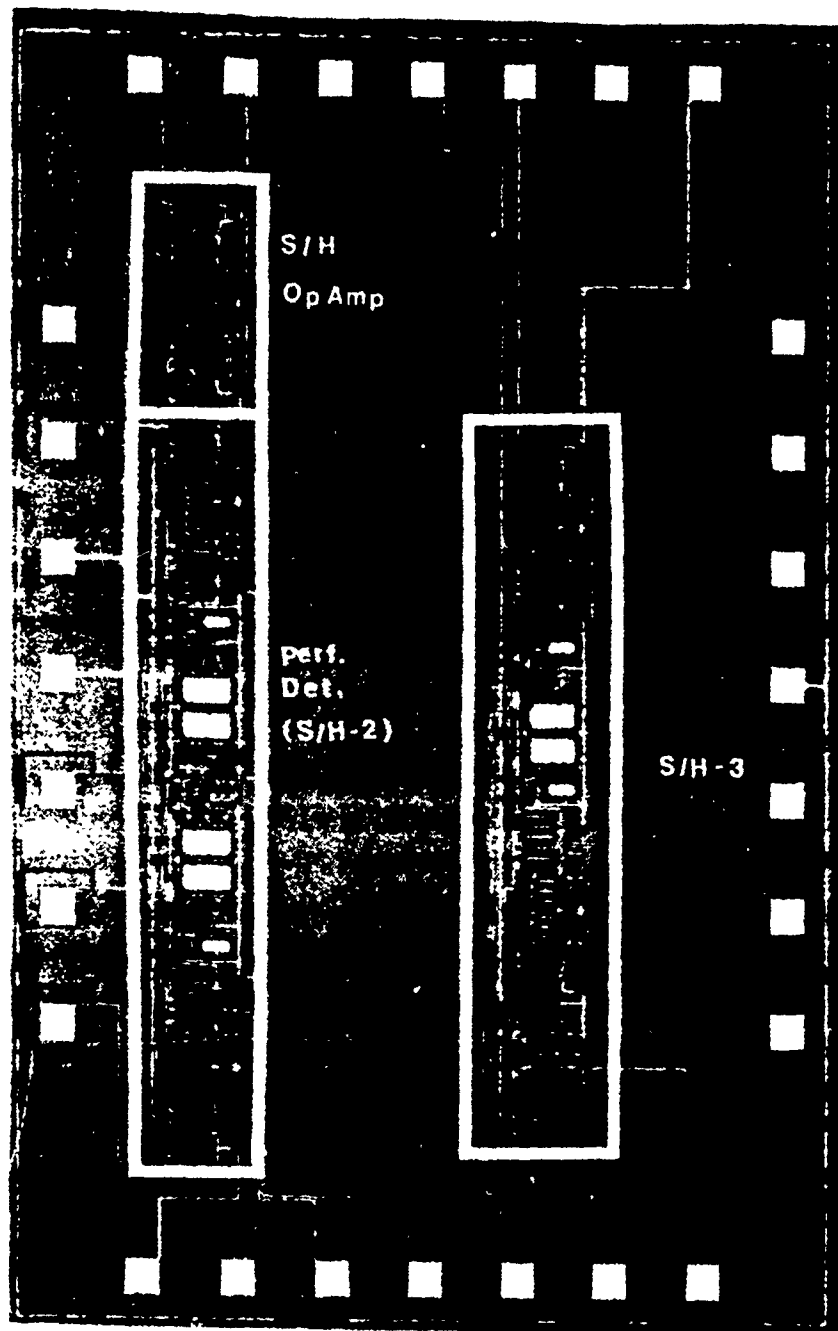


Fig. 5.15-2b. Die photograph of S/H test cell containing a single S/H OpAmp as shown in the upper left-hand portion of the photograph.

- (a) **Open-Loop Test** — Configure the OpAmp as shown in Fig. 5.15-3, with an effective load capacitance near 5pF . Input a low frequency sinusoid, and adjust the DC voltage source, V_{offset} , to cancel any noticeable DC offset voltages present on the output of the OpAmp. This DC value corresponds to the DC offset voltage of the OpAmp. Measure the open-loop gain and slowly increase the excitation frequency until the output amplitude drops 3dB . Record this frequency as the open-loop 3dB bandwidth for the V^+ input.

Switch the input signal and the offset voltage cancellation source, and repeat the open-loop test above for the V^- input.

- (b) **Close-Loop Test** — Configure the OpAmp in the unity gain mode with the test configuration shown in Fig. 5.15-4. Ground the input signal, V_i , and check for possible oscillation present on the output signal, V_o . This tests for unity-gain stability. If no oscillation is present, the step-response will serve as a quick check for phase margin. Marginal phase margin will be characterized by severe ringing in the output at each step excitation.

- (2) **Parasitic Load Capacitance Measurement** — This OpAmp has been designed so that the slew rate is essentially determined by the total load capacitance, C_t , where C_t includes parasitic device and instrumentation capacitances as well as any external load capacitance. The slew rate is related to C_t by the expression

$$SR = \frac{k}{C_t} \quad (5.15 - 1)$$

where k is a constant characteristic of the OpAmp. Our goal in this measurement is to determine C_L , the parasitic and instrumentation load capacitance. To determine C_L , configure the OpAmp in the open-loop configuration shown in Fig. 5.15-3. Apply a square wave to the plus terminal of the OpAmp and measure the slew-rate SR_{20} with a load capacitance of $C_L + 20\text{pF}$ (e.g., a 20pF capacitor is added to the output) on the output. Repeat the slew rate measurements with a load capacitance of $C_L + 50\text{pF}$ to yield SR_{50} .

From (5.15-1), it follows that

$$\begin{aligned} SR_{20} &= \frac{k}{C_L + 20\text{pF}} \\ SR_{50} &= \frac{k}{C_L + 50\text{pF}} \end{aligned} \quad (5.15 - 2)$$

The simultaneous solution of these two equations with two unknowns (k and C_L) yields the parasitic load and instrumentation capacitance

$$C_L = \frac{50SR_{50} - 20SR_{20}}{SR_{20} - SR_{50}} \text{pF} \quad (5.15 - 3)$$

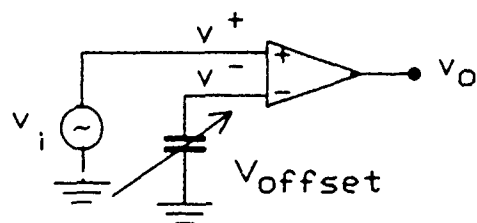


Fig. 5.15-3. Open-Loop test configuration for the S/H OpAmp.

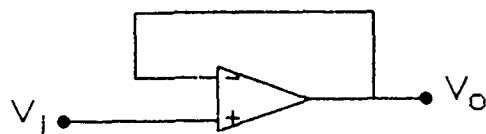


Fig. 5.15-4. Close-Loop test configuration for the S/H OpAmp.

The load capacitance dominance of the SR as expressed in (5.15-1) can be verified by adding a different load capacitance and verifying (5.15-1) remains valid with the values for k and C_L determined from solving the equations in (5.15-2).

- (3) Frequency Response — With the total effective load capacitance set at near the design value of $6pF$, the open-loop frequency response for the OpAmp can be measured via the test configuration shown in Fig. 5.15-3. In this configuration we wish to measure the following items:
 - (a) gain/phase BODE plot for both V^+ and V^- inputs,
 - (b) DC open-loop gain for both input signals, (V^+ and V^-),
 - (c) open-loop $3dB$ bandwidth for both V^+ and V^- inputs,
 - (d) gain and phase margin
 - (e) DC input offset-voltage.
- (4) Step Response — Configure the OpAmp in the closed loop test configuration, shown in Fig. 5.15-3. Note that in this configuration, the load capacitance has been slightly increased with the addition of the input and parasitic capacitance associated with the V^- input terminal. This additional capacitance should be minimized if possible. In this test setup, we wish to place a square wave function generator on the input V_i and measure the following characteristics:
 - (a) slew rate — the slope of the output waveform at or near the zero crossing for both rising and falling transistions,
 - (b) the time required to settle within 1% of the final value, and
 - (c) the percent overshoot of the output waveform relative to its final value.
- (5) Noise Measurements — Ground both inputs and measure the rms noise voltage present on the output node, V_o , as a function of frequency, via the HP Spectrum Analyzer. Project (reference) these measurements back to the input by dividing by the average of the DC open-loop gain for V^+ and that for V^- of the OpAmp, as measured in item (3b) above. Extract from this data the following characterisitcs:
 - (a) $\frac{1}{f}$ corner frequency, and
 - (b) the thermal or white rms voltage noise floor.
- (6) Power Supply Rejection Ratio — Place the amplifier in the closed-loop configuration shown in Fig. 5.15-3. Ground V_i and inject an input signal generated by a Spectrum Analyzer connected in series with V_{DD} . Record the frequency response of V_o on the Spectrum Analyzer, which corresponds to $\frac{1}{PSRR}$. Repeat the above measurement for V_{SS} .

The following standard characterization parameters can be readily determined from these measurements.

- (a) the DC PSRR for both power supplies, and
- (b) the corner frequency at which the PSRR starts to roll off.

Experimental Results:

This test structure is still being tested, but the preliminary results thus far indicate the design is functional. The functional test has been completed with the following results.

- (1) With a large-capacitive load, the open-loop amplifier had a DC open-loop gain of approximately 50, as expected. The amplifier gain started rolling off around 20MHz . This was a slightly lower frequency than expected because the pole location due to the g_m of the output stage and the load capacitance was decreased by the additional capacitive loading placed on the output. The load capacitance consisted primarily of the parasitic packaging capacitance ($\approx 1\text{pF}$) and the probe capacitance ($\approx 10 - 15\text{pF}$). The proto board capacitance ($\approx 4 - 5\text{pF}$) was minimized by bending the output pin up away from the proto board, and soldering it to a test lead. The total load capacitance was thus in the $5 - 6\text{pF}$ range.
- (2) The closed-loop unity gain configuration oscillated at approximately $20 - 22\text{MHz}$. This oscillation was expected because of the large load capacitance associated with instrumentation parasitics. Since the unity gain configuration places the most stringent requirements on phase margin, the phase margin at higher gains will be investigated.
- (3) Since the stability of this amplifier is in question, in particular when it is applied to the S/H application and has the intended load capacitance, the S/H-2 design was tested where results showed some ringing, but no oscillation. For more information on this test, see Section 5.13.
- (4) The input offset voltage was measured around $10 - 15\text{mV}$.

Additional detailed characterization of this Operational Amplifier will be undertaken in the future.

5.16 Performance Detector - Subcomponent Linearities

Name:	Test-Devices
MOSIS ID:	23625
Fab. ID:	M770BH-4
Technology:	CBPM — MOSIS $3\mu\text{m}$ CMOS double-metal p-well process
Fabricated:	July - August 1987
Chip Size:	$1230\mu\text{m} \times 1650\mu\text{m}$ (2.03mm^2)
Active Area:	$600\mu\text{m} \times 1100\mu\text{m}$ (0.66mm^2)
Number of Pads:	17
Packaging:	28 pin package
Status:	Fabricated awaiting testing.

Purpose:

This test chip will be used to characterize both the nonlinearities in the *on-resistance* of n-channel and p-channel MOSFETs used for switching as a function of the channel width, and the nonlinearities associated with the parasitic n^+ -diffusion and p^+ -diffusion capacitors. The underlying motivation is to track system level nonlinearities associated with the biquad and sample/hold circuits back to process dependent parasitic nonlinearities and thus predict the overall performance limitations of the various architectures as a function of their nonlinear distortion. For example, the single OpAmp sample/hold circuit's sampling error is very sensitive to nonlinearities induced by the analog switches through both the nonlinearities of the *on-resistance* and parasitic diffusion capacitors associated with the switches. For more information on performance limitations due to intrinsic nonlinearities, see the biquad and sample/hold design discussions.

Also contained on this chip is a p^+/n^+ and a p^-/n^+ lateral diode, with the intentions of characterizing the DC and high frequency performance of these devices. The MOSIS process specifications [30] do not describe nor provide the appropriate simulation information for these devices, thus the data collected from these test devices will be used in designing future generations of performance detectors such as peak detectors and the more classical sample/hold structures.

Description:

The pin-outs, die photograph and basic floor-plan for this test chip is shown in Fig. 5.16-1a, -1b and 5.16-2 respectively. The main test cell can be divide into three independent test blocks, MOSFET, diffusion capacitor and diode test cells. Complete circuit schematics for these three test cells are shown in Fig. 5.16-3.

The MOSFET test cell consists of three n-channel and three p-channel MOSFETs configured to allow for individual testing of each device. The channel widths of all six devices were set at $1000\mu\text{m}$ each, so that the packaging and external load capacitance would not greatly hinder high frequency characterization of these devices. The channel

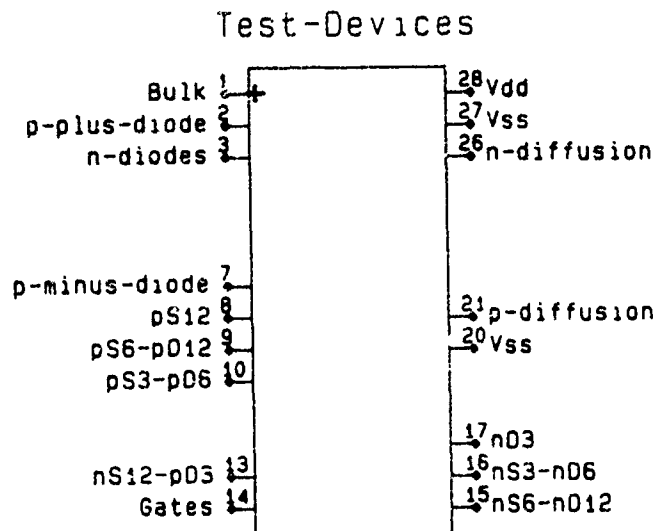


Fig. 5.16-1a. Pin-out for the nonlinear devices test cell.

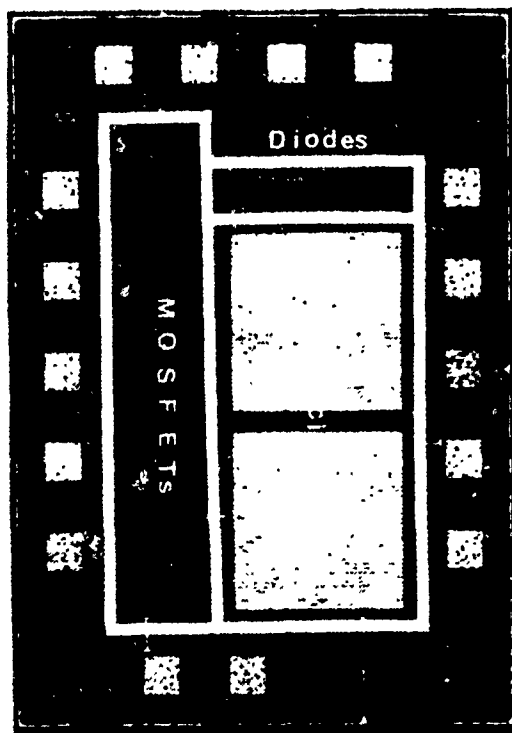


Fig. 5.16-1b. Die photograph of nonlinear test devices.

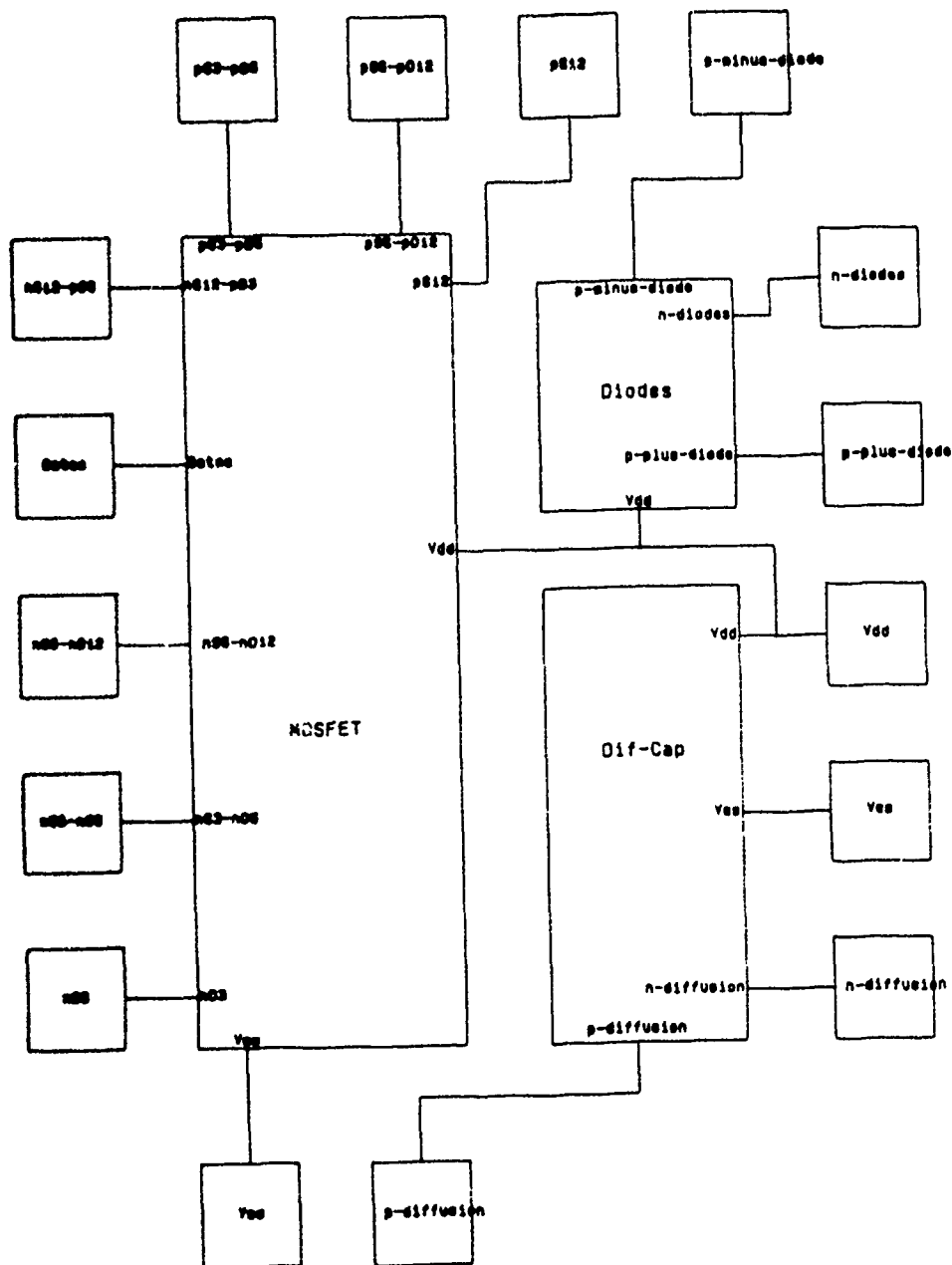


Fig. 5.16-2. Floor-plan for the nonlinear devices test cell.

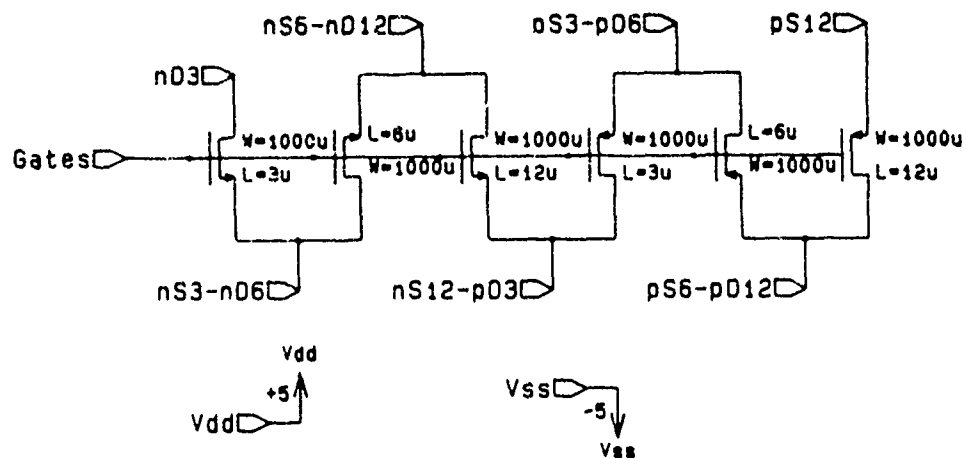


Fig. 5.16-3a. MOSFET test structure.

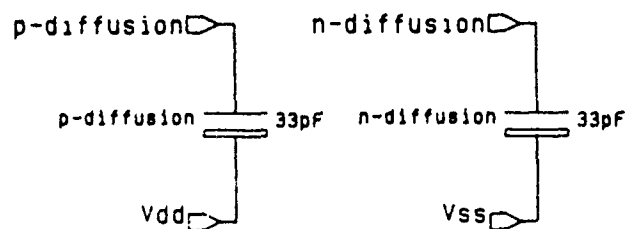


Fig. 5.16-3b. Diffusion capacitor test structure.

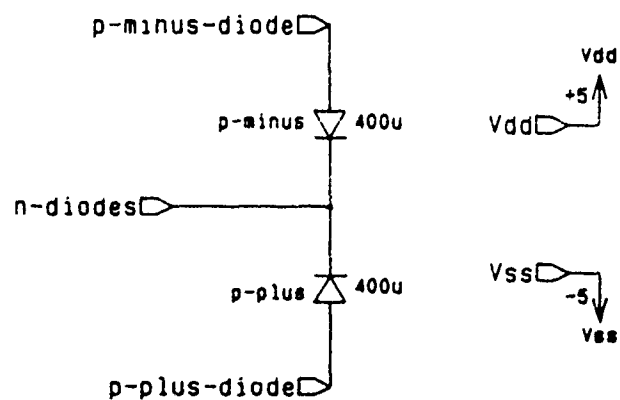


Fig. 5.16-3c. Lateral Diode test structure.

lengths were varied between $3\mu m$, $6\mu m$ and $12\mu m$, to ascertain information about nonlinear distortion as a function of short-channel effects.

The capacitor test cell consists of an n^+ -diffusion and a p^+ -diffusion capacitor, each $400\mu m \times 400\mu m$ or $\sim 33pF$. These capacitors are large enough that the probe capacitance will not be dominant.

The diode test cell consists of a p^+/n^+ lateral diode $400\mu m$ long by the diffusion depth tall, and a p^-/n^+ lateral diodes $400\mu m$ long by 2 times the diffusion depth plus $4\mu m$, as illustrated by the cross-sectional sketches shown in Fig. 5.16-4 represents the physical process driven layout of the lateral devices. These large device sizes allow for high frequency testing of the test devices without requiring on-chip buffering. The p^+ diffusions on the p^-/n^+ diodes are included to maintain good electrical contact to the p^- -well.

Test Plan:

MOSFET Cell

With each MOSFET biased "on" with a $\pm 5V$ power supply, the small signal impedance modeling the device's *on-resistance* will be measured using the LF Impedance Analyzer, HP4192A [†] at $100kHz$, $1MHz$ and $5MHz$ with a DC-offset between varied between $-2V$ and $+2V$ in increments of $0.05V$. This instrument has the capabilities of automatically measuring the small-signal impedance of a two-port test device at selected frequencies and DC-offsets. This instrumentation is controlled by a HP-Vectra through an IEEE 488 bus.

Capacitor Cell

The small signal capacitance of each diffusion capacitor will be measured using the same test setup as described above at $100kHz$, $1MHz$ and $5MHz$ with a reverse bias varied between $-3V$ and $-7V$ in increments of $0.05V$.

The DC I-V characteristics and the AC characteristics (e.g., turn off speed, charge feed-through effects, and other basic model parameters) for the lateral diodes will be measured next year. A more detail test plan for these devices will be supplied at that time.

Experimental Results:

No results are available at this time.

[†] The specifications describing the HP4192A capabilities are included in Appendix-C of this document.

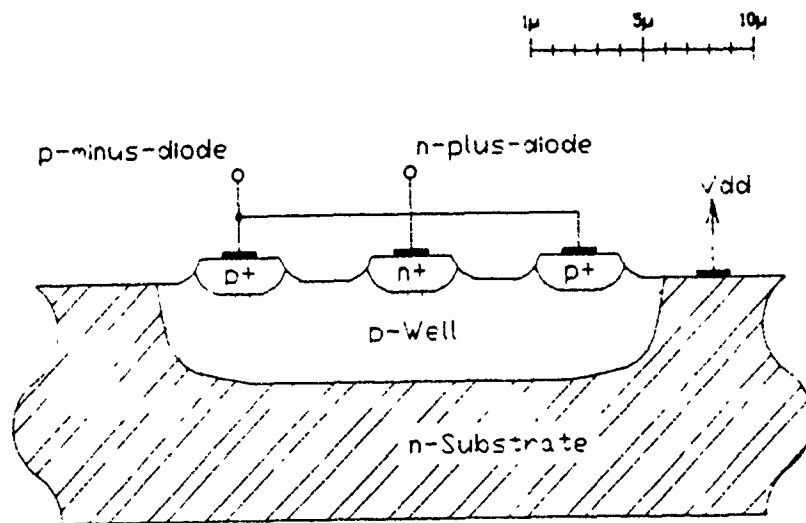


Fig. 5.16-4a. Cross-section of p^-/n^+ lateral diode.

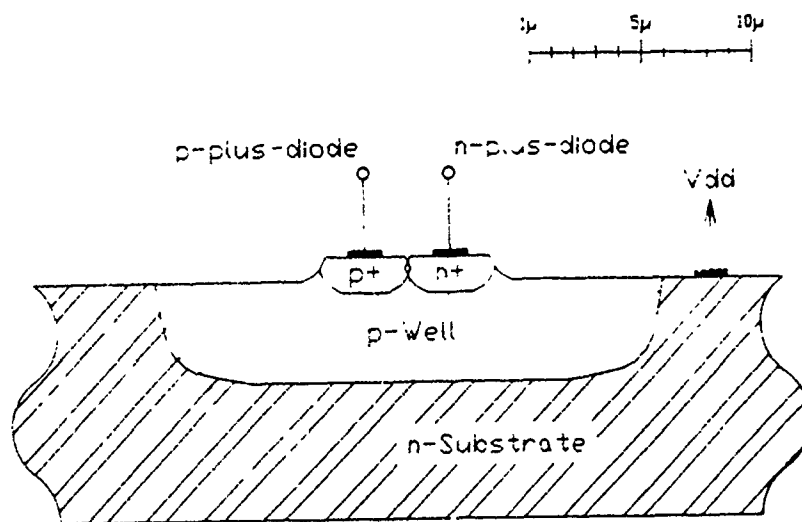


Fig. 5.16-4b. Cross-section of p^+/n^+ lateral diode.

5.17 Performance Detector based upon S/H-2 with modified OpAmp

Name:	S/H-2 w/ zero
MOSIS ID:	23983
Fab. ID:	M79YDD2-1
Technology:	CBPE — MOSIS $3\mu m$ CMOS double-poly p-well process
Fabricated:	September - October 1987
Chip Size:	$2300\mu m \times 3400\mu m$ ($7.82mm^2$)
Active Area:	$235\mu m \times 1940\mu m$ ($.45mm^2$)
Number of Pads:	11
Packaging:	28 pin package
Status:	Currently being fabricated.

Purpose:

This test vehicle will be used to dynamically characterize the performance and performance limitations of the S/H-2 based Performance Detector architecture incorporating a more stable Operational Amplifier design, to accurately sample high-frequency large-amplitude signals in the presences of circuit non-idealities, such as switch feed-through, voltage dependent switch "on" resistance, statistical process variation, etc..

Description:

The circuit schematic, pin-out and block diagram of this test structure, is identical to the S/H-2 test structure presented in Section 5.13 of this report, with two exceptions: (1) a more stable OpAmp design was substituted for the original design; (2) the layout error, where $I_{bias}/Resp$ was not connected to the bonding pad, was corrected. The circuit schematic and a detailed description of this modified OpAmp design is discussed in Section 5.19.

Test Plan:

The same test procedure will be used for this test vehicle as was outlined in Section 5.13.

Experimental Results:

No experimental results are available at this time, circuit under fabrication.

5.18 Single S/H-3 test cell with modified Opamp

Name:	S/H-3 w/ zero
MOSIS ID:	23983
Fab. ID:	M79YDD2-1
Technology:	CBPE — MOSIS $3\mu\text{m}$ CMOS double-poly p-well process
Fabricated:	September - October 1987
Chip Size:	$2300\mu\text{m} \times 3400\mu\text{m}$ (7.82mm^2)
Active Area:	$1825\mu\text{m} \times 290\mu\text{m}$ (0.53mm^2)
Number of Pads:	14
Packaging:	28 pin package
Status:	Currently being fabricated.

Purpose:

This test cell contains a single Sample/Hold-3 cell as discussed in Section 2.2.2.3d and 5.14, with a more stable OpAmp design incorporated. The purpose of this test chip is to dynamically characterize the performance and performance limitations of the S/H-3 architecture and its associated physical design and to accurately sample high-frequency large-amplitude signals in the presences of circuit non-idealities. The performance of this archeticture will be compared to the test cell S/H-2, as discussed in Section 5.17.

Description:

The circuit schematic, pin-out and block diagram of this test structure, are identical to those of the S/H-3 test structure presented in Section 5.14 of this report with two exceptions: (1) a more stable OpAmp design was substituted for the original design; (2) the layout error, where I_{bias-2} (the bias current for the 2nd OpAmp referred as simply I_{bias} in Fig. 5.19-1) was not connected to the bonding pad, was corrected. The circuit schematic and a detailed description of this modified OpAmp design appear in Section 5.19.

Test Plan:

The same test procedure will be used for this test vehicle as was outlined in Section 5.14.

Experimental Results:

A design/layout error was discovered in the control logic, as discussed in Section 5.14. This error will render this test vehicle non-operational. Additional testing will not be performed on this chip.

5.19 High-Frequency S/H OpAmp with added zero

Name:	S/H OpAmp w/ zero
MOSIS ID:	23983
Fab. ID:	M79YDD2-1
Technology:	CBPE — MOSIS $3\mu\text{m}$ CMOS double-poly p-well process
Fabricated:	September - October 1987
Chip Size:	$2300\mu\text{m} \times 3400\mu\text{m}$ (7.82mm^2)
Active Area:	$515\mu\text{m} \times 235\mu\text{m}$ (0.12mm^2)
Number of Pads:	5
Packaging:	28 pin package
Status:	Currently being fabricated.

Purpose:

This test cell is the S/H high-frequency OpAmp. The compensation of this OpAmp differs from that of its predecessor discussed in Sec. 5.15 in that a single additional zero has been added to the gain function, as described in Section 2.2.2.3f. The circuit schematic is shown in Fig. 5.19-1 with associated device sizes contained in Table 5.15-1, and with $C_x = 1.37\text{pF}$. The overall limitations of the Performance Detector architecture depend on the performance of this OpAmp which will be characterized by this test vehicle.

The primary characteristics of interest are bandwidth, phase margin and open loop gain, which are critical to the high-frequency operation of the sample and holds. Especially of interest is the comparison of the frequency response and corresponding phase margin achieved by adding a zero to the gain function of the previous design and test structure discussed in Section 5.15.

Description:

The circuit schematic, pin-out and block diagram of this test structure, is identical to the S/H-OpAmp test structure presented in Section 5.15 of this report, with one exception: a more stable OpAmp design of Fig 5.19-1 was substituted for the original design.

Test Plan:

The same test procedure will be used for this test vehicle as was outlined in Section 5.15.

Experimental Results:

No experimental results are available at this time; circuit in fabrication.

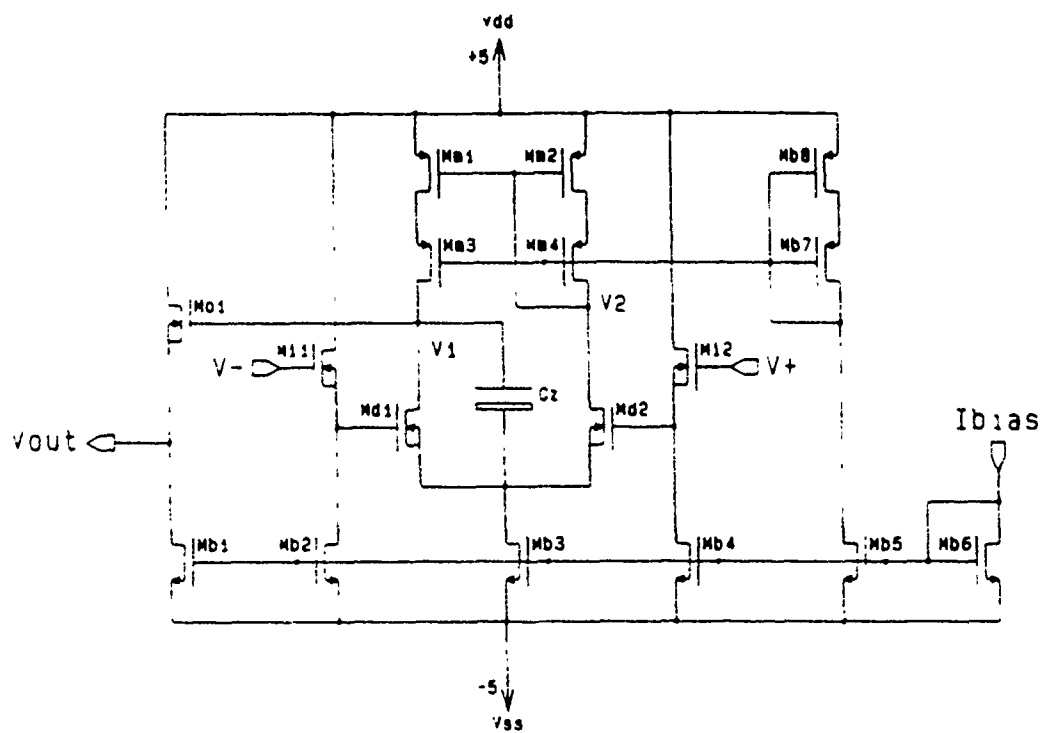


Fig. 5.19-1. S/H OpAmp with added zero circuit schematic.

6.0 SUMMARY

In the initial phase of this project, a design methodology for designing precision high-frequency monolithic continuous-time signal processors was introduced. These structures are comprised of an analog digitally controlled signal processing path along with performance monitoring and control circuitry. Local intelligence is used to dynamically tune the signal path thus yielding circuits which are inherently insensitive to the major technological limitations plaguing linear IC designers, namely; nominal and statistical parameter variations, passive and active component matching, temperature variations, aging and parasitics. These structures are termed Digitally Controlled Analog Signal Processors (DCASP). Major emphasis this year has been placed upon designing and testing circuit structures serve as subcomponents in the overall DCASP architecture.

One major accomplishment this year was in the design and fabrication of a controlled signal processor. A preliminary version of this circuit was designed and reported on last year. In addition to minor design errors which rendered this circuit only partially functional, neither the resolution nor the adjustment range of this circuit were considered acceptable. The new structure, termed DCASP-2, was designed to have over three decades of center frequency adjustment and over three decades of bandwidth adjustment. The frequency and bandwidth adjustment range goes from approximately 2Khz to 2M hz. Resolution in the center frequency over this range is to 0.5% or better and bandwidth resolution is to 1% or better. The circuit is totally electrically reconfigurable and programmable and is capable of realizing any transfer function within the specified parameter adjustment range up to 6th order. The circuit was designed in a standard 3u double polysilicon CMOS process and fabricated in industry. The basic functionality, reconfigurability, wide adjustment range and fine resolution have been experimentally verified. Detailed dynamic testing of this structure is ongoing.

Significant advances in the design of operational transconductance amplifiers (OTAs) was also made. These circuits are used as the active elements in the controlled signal processor because of their inherent wide bandwidth and practical programmability. Structures which have over two decade adjustment range in gain (g_m) with resolution to 1% were designed, fabricated and tested. These structures achieve fine resolution through programmability of the tail voltage on the differential input stage and wide adjustment range through switch selection of output current mirror gain. Fabrication of these structures was also in a standard 3u CMOS process.

Progress was also made on the design of the performance detector. Three different performance detector architectures were investigated. These are all based upon a high speed sample and hold structure followed by a slower precision A/D converter. This approach was selected because of the performance advantages which can be achieved with slower A/D converter design. Major emphasis was placed on the design of the sample and hold architecture since design methodologies for precision slow speed A/D converters are well developed. Different sample and hold structures have been designed and fabricated

in a 3u CMOS process. Results of preliminary testing of these structures are presented in Section 5 of this report. More extensive dynamic testing is ongoing.

The tuning algorithm was also investigated. The tuning problem has been divided into two parts. The first part involves measuring the performance of an existing filter structure and the second is the actual tuning itself. Several different parameter measurement algorithms were investigated. Both transfer function magnitude measurements and performance parameter extraction from these measurements were addressed. Consideration of the effects of noise, measurement errors (e.g. nonlinearities, rounding and quantization) and the number of functional evaluations needed were made. One magnitude measurement method requiring only three A/D conversions per sample magnitude measurement was introduced. This simple algorithm is very fast but is sensitive to errors in the data converter and noise. A curve fitting algorithm based upon a large number of A/D conversions was also investigated which proves to be more tolerant to inaccurate converter outputs. Several methods of extracting relevant characterization parameters from the magnitude measurements have been investigated. One which is discussed in this report which performs quite well is based upon using a spline function to fit to the measured transfer function magnitudes. In the absence of measurement errors this algorithm performs very well although the number of required functional evaluations is a little larger than desired. Another method which has fewer functional evaluations and which is more robust is currently under evaluation.

Twenty circuit test structures were also designed and fabricated in a 3u CMOS process. These test structures serve as subcomponents in the basic building blocks used in the DCASP architecture. These test structures include D/A converters, operational transconductance amplifiers, sample and hold circuits, operational amplifiers, digital logic test structures as well as the controlled signal processor block. Details about the design and testing of these structures appear in earlier sections of this report.

7.0 CONCLUSIONS

Preliminary theoretical and experimental results support the contention that the DCASP approach offers potential for practical precision monolithic signal processing over a wide range of frequencies. The flexibility and reconfigurability of the present DCASP architecture has been experimentally verified. The preliminary CSP circuit itself, in addition to being reconfigurable and programmable over three decades in frequency, offers experimentally verified performance specifications in the higher portions of the frequency spectrum that are near to or beyond the best results reported in the technical literature.

8.0 RECOMMENDATIONS

Additional investigation of DCASP architectures are needed to determine the ultimate practical precision and frequency range attainable with this design methodology. This investigation needs to be made at both theoretical and experimental levels.

Architectures which offer increased flexibility for serving as generic system blocks should be investigated. These generic structures should positively impact the cost of developing precision military systems.

Architectures which offer significant reductions in area with only modest reductions in flexibility should also be investigated. These structures will be less costly in high volume applications. Control and tuning algorithms need additional investigation. The bidirectional functional on-chip tuning potential offered by the DCASP architecture has received minimal attention in the literature.

Subcomponents needed for the DCASP system must be investigated from a theoretical and experimental basis. The ultimate performance potential of DCASP systems is strongly dependent upon the system subcomponents, namely the CSP and the Performance Detector.

Very high frequency circuit structures which can be digitally controlled should be investigated. Emphasis should be placed upon flexibility, extension of the frequency range of operation, and improving linearity.

Extension of this approach into the Gallium Arsenide technology to take advantages of both improvements in speed and radiation hardness should also be made. To make this transition, practical access to a generic GaAs process is needed. Two possibilities are the Rockwell and the MacDonald Douglas pilot lines which were supported by DARPA. We have established contacts with both groups and currently have processing information about both processes. Both processes have been focused entirely on digital applications and consequently good device models for analog applications have not been developed. This model development must be addressed initially. Test structures for verifying models and test structures which will be used in the design of basic functional blocks in the DCASP architecture must also be designed, fabricated and tested.

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APPENDIX A

SPICE Model Parameters

The following is a list of the level 2 SPICE model parameters^[A-1] as recommended by MOSIS for analog design. These parameters were used with versions 2g6 and 3a7 of SPICE as distributed by Berkeley.

Table A-1. Level 2 SPICE model parameters.

Parameter	Value		Units
	NMOS	PMOS	
<i>LD</i>	0.28 μ	0.28 μ	<i>m</i>
<i>TOX</i>	500.0 $E - 10$	500.0 $E - 10$	<i>m</i>
<i>NSUB</i>	1.0 $E + 16$	1.121088 $E + 14$	1/ cm^3
<i>VTO</i>	0.827125	-0.894654	<i>V</i>
<i>KP</i>	3.286649 $E - 05$	1.526452 $E - 05$	A/V^2
<i>GAMMA</i>	1.35960	0.879003	$V^{1/2}$
<i>PHI</i>	0.6	0.6	<i>V</i>
<i>UO</i>	200.0	100.0	cm^2/Vs
<i>UEXP</i>	1.001 $E - 03$	0.153441	
<i>UCRIT</i>	999000.	16376.5	V/cm
<i>DELTA</i>	1.24050	1.93831	
<i>VMAX</i>	100000.	100000.	<i>m/s</i>
<i>XJ</i>	0.40 μ	0.40 μ	<i>m</i>
<i>LAMBDA</i>	1.604983 $E - 02$	4.708659 $E - 02$	1/ <i>V</i>
<i>NFS</i>	1.234795 $E + 12$	8.788617 $E + 11$	1/ cm^2
<i>NEFF</i>	1.001 $E - 02$	1.001 $E - 02$	
<i>NSS</i>	0.0 $E + 00$	0.0 $E + 00$	1/ cm^2
<i>TPG</i>	1.0	-1.0	
<i>RSH</i>	17	42	$Ohm/sq.$
<i>CGSO</i>	5.2 $E - 10$	4 $E - 10$	F/m
<i>CGDO</i>	5.2 $E - 10$	4 $E - 10$	F/m
<i>CJ</i>	4.5 $E - 4$	3.6 $E - 4$	$Ohm/sq.$
<i>MJ</i>	0.5	0.5	
<i>CJSW</i>	6.0 $E - 10$	6.0 $E - 10$	F/m
<i>MJSW</i>	0.33	0.33	

APPENDIX B

Reprints of Papers

HIGH-FREQUENCY VOLTAGE-CONTROLLED CONTINUOUS-TIME LOWPASS FILTER USING LINEARISED CMOS INTEGRATORS

Indexing term: Filters

The design and implementation of a continuous-time lowpass filter with voltage-controlled cutoff frequency and passband ripple is presented. The circuit uses a linearised CMOS transconductor as a basic integrating building block. A voltage-controlled phase-adjusting scheme is employed in the integrator to compensate for excess phase in the transconductance at high frequencies. The fabricated filter is capable of realising cutoff frequencies as high as 2 MHz and handles single-ended input signals up to 4 V p-p with less than 1% distortion.

Introduction: Recently several techniques for realising continuous-time filters in MOS technology have been proposed. Most of these techniques realise filters in the audio frequency range,¹ where switched-capacitor (SC) circuits have already been established as a viable approach. However, as operating frequencies are raised by an order of magnitude or more, the advantages of continuous-time processing become increasingly apparent.² To date, only a few fully MOS realisations of high-frequency continuous-time filters have been reported. The technique proposed in Reference 2 realises a 300 kHz bandpass filter but has limited signal swing capability due to nonlinearities in the MOSFETs used. Recently, a low-frequency linearising scheme has been extended to high frequencies,³ but only simulated results using operational amplifiers with 200 MHz gain-bandwidth products are available. This letter discusses the implementation of a 1 MHz lowpass filter using linearised CMOS transconductance integrators with improved signal-handling capability. Experimental results obtained from a fabricated test chip are reported.

Filter realisation: Fig. 1 shows the basic transconductance circuit used in the proposed filter. It employs a linearised input stage consisting of a simple source-coupled pair M_1, M_2 biased dynamically by a current component proportional to the square of the input voltage $V = V_1 - V_2$. This square-law current is generated by the crosscoupled configuration M_3-M_4 and coupled through a level-shifting device M_5 . By properly scaling the W/L ratios of the source-coupled pair and the crosscoupled devices, the nonlinearities of the input stage can be largely cancelled out over a wide input voltage range.⁴ The remaining devices M_6-M_{11} are used to bias the input stage and to sum device currents to obtain the final output current I_o . Assuming unity-gain current mirrors and a square-law model⁵ for the input devices gives the following linear i/v characteristic for the complete transconductor:

$$I_o = g_m V = K(V_C - V_T)V \quad (1)$$

where K is a constant dependent on process parameters and the geometries of M_1-M_4 and M_6-M_{11} , and V_C is the n-channel threshold voltage. Note that the transconductance $g_m = K(V_C - V_T)$ is adjustable by control voltage V_C . The range of V over which eqn. 1 is valid and further design

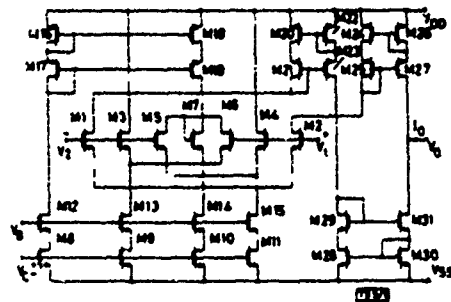


Fig. 1 Linearised CMOS transconductance circuit

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details for the basic input stage are discussed elsewhere⁴ and are not repeated here.

The complete transconductance circuit of Fig. 1 was fabricated using a standard 3 μ m double-poly p-well CMOS process.⁶ M_1, M_2 and M_3-M_4 had $W/L = 10 \mu\text{m}/5 \mu\text{m}$ while M_5, M_6 had $W/L = 20 \mu\text{m}/5 \mu\text{m}$. The substrates of these devices were connected to their respective sources. The remaining n-channel devices were in a common p-well connected to V_{DD} . All p-channel devices shared a common substrate connected to V_{SS} . The circuit occupies a total area of $220 \times 700 \mu\text{m}^2$. Fig. 2 depicts the nonlinearity in the measured i/v characteristic of the fabricated circuit as a percentage of a 2 V (peak) full-scale value, using the nominal supply and bias voltage values indicated. The results are comparable to those for recently reported transconductor schemes.^{7,8}

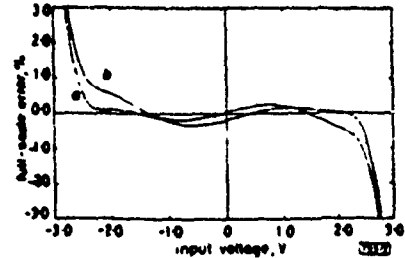


Fig. 2 Measured nonlinear error of transconductor for $V_{DD} = -V_{SS} = 5 \text{ V}$, $V_C = -2.5 \text{ V}$, $V_T = 1.75 \text{ V}$, $V_{SS} = 0$

a Input $V_1, V_2 = 0$

b Input $V_1, V_2 = 0$

However, the present circuit has the advantage of not requiring an accurately balanced input drive or a complicated output common-mode biasing circuit.⁹ The circuit consumes 10 mW with the nominal bias values, and exhibits a short-circuit 3 dB bandwidth of 15 MHz.

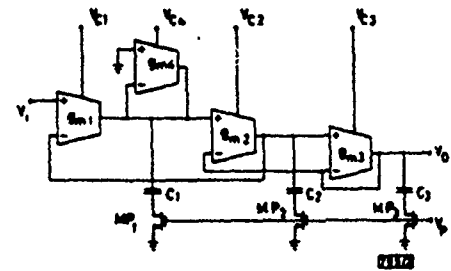


Fig. 3 3rd-order Chebyshev lowpass filter using phase-compensated transconductance integrators

$$C_{M1} = C_{M2} = C_{M3} = C_{M4} = C_{M5} = C_1 = C_2 = 9.2 \text{ pF}, C_3 = 4.5 \text{ pF}$$

Fig. 3 shows a 3rd-order Chebyshev lowpass ladder filter realised using the transconductor of Fig. 1 as a basic integrating building block. MOS capacitors C_1-C_3 perform the required integration. The drain resistances of devices $M_{P1}-M_{P3}$ in series with the capacitors introduce a high-frequency zero in the transfer function of each integrator. This zero is used to compensate for excess phase shift within the transconductor at high frequencies. The location of this zero is controllable using V_C , resulting in a voltage-variable phase-compensation scheme. If the initial phase errors are not large, the zero frequency is much higher than the unity-gain bandwidth of the integrator. Therefore, at frequencies within the passband of the filter, the signal voltages across the compensating MOSFETs are very small, resulting in negligible distortion due to nonlinearities of these devices. It can be shown that, for a single integrator with input $V = V_i \sin \omega t$, the distortion caused by the nonlinear phase-compensating device is mainly due to the second-harmonic component and is approximately given by

$$HD \approx \frac{g_{m2} r_d^2 V_i}{(V_C - V_T) \sqrt{4g_{m2} r_d^2 + (g_{m2} r_d)^2}} \quad (2)$$

where g_m is the integrator transconductance, C the integrating capacitance and r_o the small-signal resistance of the compensating transistor. Eqn. 2 has been derived assuming a first-order model of the compensating MOSFET operating in the ohmic region of its i_D characteristic.³ For typical values $g_m/r_o = 0.62$, $V_{ds} = V_p - V_{th} = 2$ V and $\alpha = g_m/C$, eqn. 2 gives $ND < 0.65\%$.

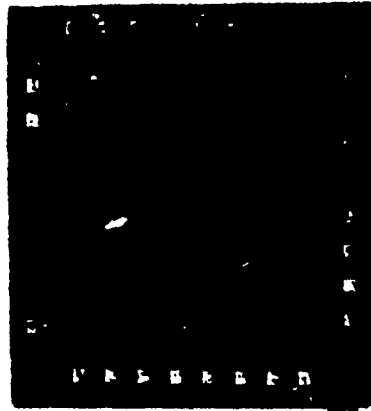


Fig. 4 Photomicrograph of experimental chip

The complete filter of Fig. 3 was designed to have a nominal cutoff frequency $f_c = 1$ MHz with a passband ripple of 1 dB and was fabricated using the process already mentioned.⁶ MP₁-MP₂ had $W/L = 25$ and their substrates were short-circuited to their sources. The entire filter, including the capacitance, phase-compensating devices and on-chip output buffers, occupies an area of $1500 \times 700 \mu\text{m}^2$. A photomicrograph of an experimental chip including the proposed filter as well as single transconductor and buffer test cells is shown in Fig. 4. All measurements were made using ± 5 V supplies with $V_{cs} = -2.5$ V. Fig. 5a shows the measured frequency response of the 1 MHz filter after adjusting $V_{c1} = V_{c2} = V_{c3} = V_{c4} =$

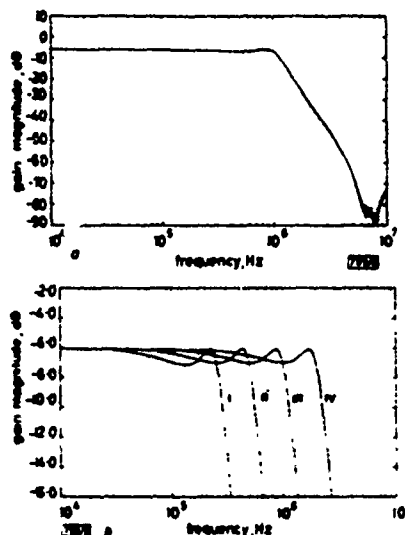


Fig. 5 Measured frequency response of filter

- a Cutoff frequency $f_c = 1$ MHz, $V_{c1} = 1.554$ V, $V_p = 1.845$ V
 b Expanded passband characteristics:
 (i) $f_c = 250$ kHz, $V_{c1} = 1.155$ V, $V_p = 1.065$ V
 (ii) $f_c = 500$ kHz, $V_{c1} = 1.208$ V, $V_p = 1.270$ V
 (iii) $f_c = 1$ MHz, $V_{c1} = 1.554$ V, $V_p = 1.845$ V
 (iv) $f_c = 2$ MHz, $V_{c1} = 2.562$ V, $V_p = 4.320$ V

730

V_{c1} and V_p to obtain the specified cutoff frequency and passband ripple. Expanded passband characteristics are given in Fig. 6b for four different values of (V_{c1}, V_p) corresponding to f_c ranging from 250 kHz to 2 MHz. In each case the control voltages were adjusted to make the measured passband response within ± 1 dB of the ideal Butterworth response. For f_c as high as 1.5 MHz, the variation in cutoff frequency is essentially linear with respect to V_{c1} , as expected from the linear dependence of g_m in eqn. 1. Above this frequency, the increased value of V_{c1} required drives M_1 - M_{12} into their ohmic region of operation, resulting in a nonlinear dependence of f_c on V_{c1} . This also limits the maximum obtainable value of f_c to approximately 2.2 MHz. To test the effectiveness of the phase control scheme, the drain resistances of MP₁-MP₂ were made very small by applying a large V_p ($+10$ V). This effectively disabled the phase compensation and resulted in a 2 dB peaking at the edge of the passband due to excess phase shifts in the integrators. The distortion characteristics of the filter were investigated. Fig. 6 shows the output spectrum obtained for the 1 MHz filter with a 4 V p-p input signal at 250 kHz. The total harmonic distortion in this case is within 1%. The distortion is reduced to 0.2% for a 2 V p-p input. The measured output noise spectral density above 10 kHz in the passband of the 1 MHz filter is fairly constant at $\pm 1 \mu\text{V}/\sqrt{\text{Hz}}$. This value increases slightly at lower frequencies due to $1/f$ noise, rising to $1 \mu\text{V}/\sqrt{\text{Hz}}$ at 100 Hz.

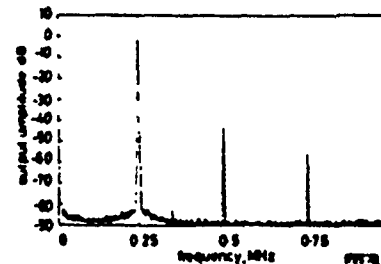


Fig. 6 1 MHz filter output distortion spectrum for $V_p = 4$ V p-p at 250 kHz

Conclusion: The design and implementation of a novel continuous-time filter technique using linearised high-frequency CMOS transconductors has been presented. A fabricated Chubbuck lowpass prototype exhibits a 1 MHz nominal cutoff frequency and is capable of handling input signals as high as 4 V p-p with less than 1% distortion using ± 5 V supplies. Using a voltage-controlled phase-compensation scheme, accurate response can be obtained for cutoff frequencies as high as 2 MHz. The voltage-control feature allows the filter to be tuned on-chip against process and temperature variations using known tuning schemes. Extension of this technique to higher frequencies is currently being investigated.

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12th May 1986

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A Fully Balanced CMOS OTA for High Frequency Monolithic Filters

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ABSTRACT

A fully balanced CMOS OTA (operational transconductance amplifier) designed for high frequency continuous-time filters is described. Computer simulations show the OTA has less than .6% nonlinearity over a ± 1 V range. The transconductance is adjusted using a novel CMOS voltage source with an output resistance that is less than 180 Ω . A fully balanced monolithic filter biquad with lowpass and bandpass outputs at 400 kHz shows THD of .30% and .70% respectively.

INTRODUCTION

The continuous-time filter presented in this paper utilizes fully balanced OTA's in a fully balanced filter structure. The benefits of fully differential (balanced) designs have recently been exploited in several switched capacitor filters [1],[2]. Reported advantages of fully balanced structures include improved power supply rejection ratio (PSRR), simpler gain block design, higher signal-to-noise ratio, improved linearity [3], and less gain-bandwidth induced filter characteristic shifts. These benefits are obtained at the expense of increased silicon area. The tradeoff has proven justifiable in many switched capacitor applications, and should be justifiable in corresponding continuous-time applications as well.

Transconductance based gain blocks provide post-fabrication tunability, a superior frequency response, and possibly an area advantage over the conventional op amp RC integrator. The traditional gain block for low-medium frequency discrete active filters has been the operational amplifier (op amp). For high frequency filter gain blocks, transconductors (OTA's) offer advantages over the traditional op amp, which suffers from excess phase. The improved performance of the OTA at high frequencies can be attributed to the fact that the OTA has no internal high impedance nodes. Any excess phase in the OTA is primarily due to the internal current mirrors [5]. In the 100 kHz - 1 MHz range the OTA integrator excess phase is adequately modeled by a single parasitic pole ($\gg f_o$). A

traditional op amp integrator model with comparable accuracy includes 2 high frequency poles. The higher order op amp model contributes more excess phase.

Recent op amp designs (cascode and folded-cascode op amps) offer significant improvements in high frequency performance, since they have no internal high impedance nodes and thus require no separate compensation capacitor. However, these recent high frequency op amps are actually transconductance amplifiers with very large output resistances [5]. As such, these devices are not general purpose op amps, but are rather designed specifically to drive capacitive loads. In particular, the capacitive load itself is used for frequency compensation. These new high speed op amps are superior choices for applications with low current drive requirements, like switched capacitor circuits. Traditional op amp RC active filter designs, however, can not use these new op amps (even with their superior frequency performance) because of their large output resistance. Monolithic high frequency active filters based upon conventional op amps are recognized as impractical due to both the high frequency op amp limitations and the inability to practically and accurately control the passive component values.

It is our intent to exploit the improved high frequency performance of the OTA in the design of high frequency monolithic filters. Emphasis will be placed upon the design of a high performance general purpose OTA. A block diagram of a basic fully balanced OTA is shown in Fig. 1. The design problem can be decomposed into the design of a differential input stage followed by the design of the appropriate current mirrors.

INPUT STAGE

OTA's in active filter structures typically experience input/output size signals across the OTA inputs [6]. For low distortion and good dynamic range the OTA input must remain linear over a wide input voltage range. This is a problem not encountered in op amp design since the differential input is ideally zero.

The circuit of Fig. 2 is a fully balanced OTA input circuit. It differs from a conventional source coupled pair differential amplifier in that the high impedance tail current

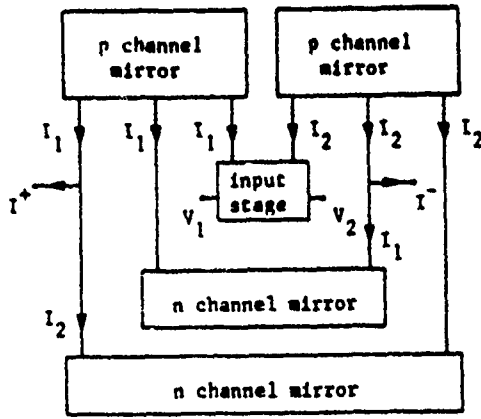


Fig. 1. Fully Balanced OTA Block Diagram.

source has been replaced by a voltage source. Both devices are assumed operating in the saturation region and modeled by Sah's equation :

$$I_1 = \beta(V_1 - V_{ee} - V_T)^2 \quad (2)$$

$$I_2 = \beta(V_2 - V_{ee} - V_T)^2 \quad (3)$$

where $\beta \equiv \frac{1}{2}\mu C_{ox} \frac{W}{L}$ and V_T is the threshold voltage. The differential output is defined as:

$$I_{out} = I_2 - I_1 = \beta[(V_2^2 - V_1^2) - 2(V_T + V_{ee})(V_2 - V_1)] \quad (4)$$

If the devices see purely differential input signals ($V_1 = -V_2$), the output expression simplifies to :

$$I_{out} = 4\beta(V_T + V_{ee})V_2 \quad (5)$$

and the transconductance gain is given by the expression:

$$g_m = \frac{I_{out}}{V_2 - V_1} = 2\beta(V_T + V_{ee}) \quad (6)$$

With differential inputs, the output current is a purely linear function of the difference mode input voltage, given that Sah's equation is an accurate model of MOSFET large signal behavior. Extensive SPICE2G.6 simulations using the full MOSIS 3μ CMOS models (25 Level 2 parameters) and device sizes listed in Table 1 have validated the excellent linearity.

OTA STRUCTURE

One of the largely unexplored advantages of OTA's is their topological and structural simplicity. The previous section has shown a very simple input stage that produces a linear output current given balanced (purely differential

mode) inputs. A method of obtaining the difference in drain currents, I_{out} , is shown in Fig. 1. The OTA does not require internal compensation like a conventional op amp, because there are no internal high impedance nodes.

Specification of current mirrors almost completes the OTA design. Consideration is given to the desired output resistance, current matching, frequency response and to the common mode output. The fully balanced input stage of Fig. 2 is combined with Wilson p-channel mirrors and cascode n-channel mirrors to form the OTA of Fig. 3. The p-channel mirrors were chosen for their superior frequency response. Very strict 1:1 current gain (and good frequency response) motivated the choice of the n-channel mirrors.

Fig. 4 shows the % full scale deviation from linear for both balanced output currents (I^+ and I^- on Fig. 3). The OTA is designed for a nominal g_m of $12.3\mu\text{mhos}$ and shows a maximum nonlinearity of .57% over ± 1 V full scale. Global parameter shifts and statistical (individual) parameter variations will cause the fabricated OTA's behavior to deviate slightly from the simulations. Nonlinearity degradation caused by global parameter shifts has been investigated by repeating the initial simulations with $\pm 25\%$ variations in each model parameter. The worst case nonlinearity was for a 25% decrease in K'_n , when the maximum full scale linear deviation became .94%. This large K'_n variation is outside the range of acceptable MOSIS fabrication parameters, so global parameter shifts should cause less severe nonlinearity. Statistical deviations were investigated for worst case β mismatches of $\pm 5\%$ and V_T mismatches of $\pm 20\text{mV}$. The maximum nonlinearity occurred for a 5% β mismatch in the input devices and was .77%. These simulated values appear a bit pessimistic based on measurements of a recently fabricated OTA with a similar topology.

Modest device mismatches can lead to large common-mode offsets unless common-mode feedback is used for Q-point stabilization [1]. The common-mode feedback is provided by the ME devices on the V_{ee} rail.

CMOS VOLTAGE SOURCE

The OTA transconductance is controlled by adjustment of V_{ee} as shown by Eq. 6. The final filter structure is designed to be readily adaptable to either Master-Slave tuning [7] or digital sensing/control [8]. An adjustable CMOS voltage source is used to buffer the tuning struc-

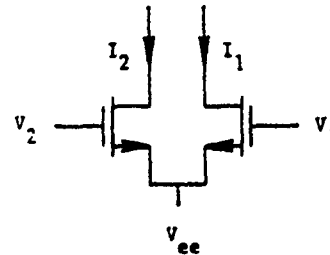


Fig. 2. Fully Balanced OTA Input Stage.

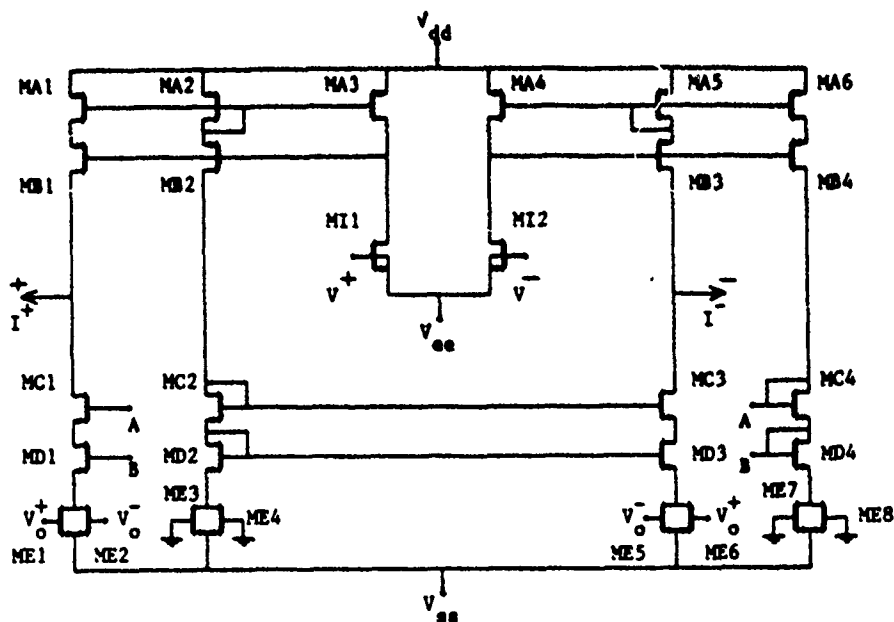


Fig. 3. Complete OTA Schematic.

ture control lines from the OTA V_{ss} current requirements. Fig. 5 shows an adjustable CMOS voltage source. A current mirror feedback loop senses V_{ss} and adjusts V_{GS} of a wide output device. A small (.36 pf) compensation capacitor is used to keep the output resistance low over a reasonable frequency range and to insure stability. The output resistance is nominally 180Ω . As V_{dd} varies from -4.0 V to -2.4 V the voltage source output V_{ss} varies from -4.15 V to -2.85 V, giving an OTA g_m adjustment range from $15.4\mu\text{mhos}$ to $8.85\mu\text{mhos}$.

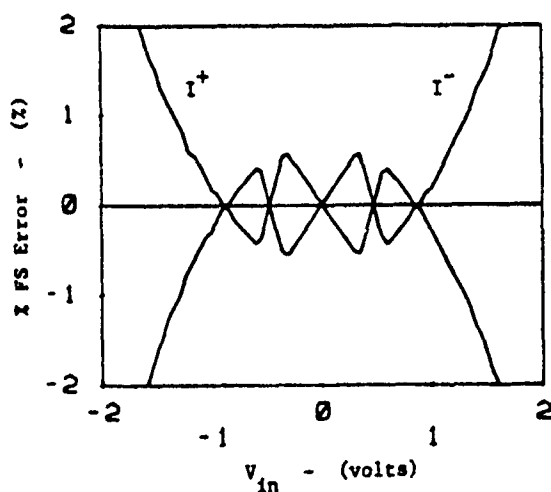


Fig. 4. Nonlinearity in balanced output currents.

INTEGRATOR

The integrator is the fundamental circuit element in many filter structures. An OTA integrator is shown in Fig. 6. For high frequency filter applications the deviations from ideal phase (90°) are critical. A parasitic pole 2 decades above the filter critical frequency (40 MHz for this filter) will contribute $.57^\circ$ excess phase. This modest amount of excess phase can cause substantial deviations from the nominal Q and critical frequency gain.

A simple phase compensation scheme obtained by the addition of a small "resistor" below the OTA integrator capacitor is shown in Fig. 6. This "resistor" introduces a phase-lead zero. An external voltage (V_x) sets the gate voltage of a grounded n-channel transistor operating in the ohmic region. The gate voltage can be used to adjust the resistance value and the zero location which offsets the excess phase due to a parasitic pole(s). Since the compensation zero is at a high frequency, the required equivalent

Devices	W/L (microns)
MAx	100/6
MBx	10/8
MIx	8/60
MCx	10/8
MDx	50/8
MEx	14/7

Table 1. OTA Device Sizes.

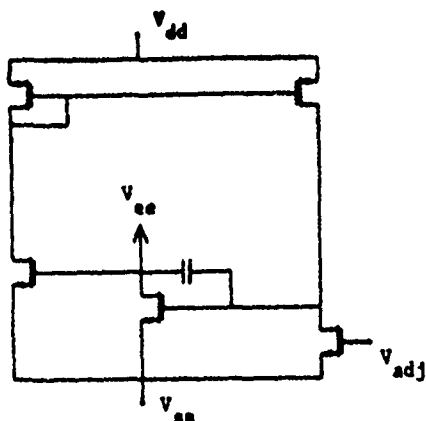


Fig. 5. CMOS Voltage Source Schematic.

resistance is low, and consequently the portion of the signal voltage appearing across the ohmic device is small. Therefore, distortion caused by the ohmic device is negligible. The integrator phase response simulation with $C = 16.96\text{pf}$ shows negligible phase error at $f_o = 400\text{ kHz}$, and less than $.25^\circ$ within an octave of f_o for $V_z = 1.25\text{ V}$.

FILTER TOPOLOGY

A fully balanced OTA based biquad is shown in Fig. 7. The topology is similar to that used by the op amp Tow-Thomas filter. In the conversion of the Tow-Thomas structure the op amp integrator(s) were replaced with OTA integrators, and the other resistors with OTA's.

This filter topology has been simulated with the OTA of Fig. 3, $C_1 = 16.96\text{pf}$ and $C_2 = 1.06\text{pf}$. Because the C_2 's are fairly small, calculation of the filter critical frequency and Q must include an estimate of the capacitive loading of C_2 by the gate (input) of OTA 3. For $V_{adj} = -3.8\text{ V}$, $\pm 5\text{ V}$ supplies, and a 2 V_{pp} input signal; the filter exhibits a 400 kHz center frequency, $Q = 3.8$, and THD of .30% and .70% for the lowpass and bandpass outputs respectively.

Silicon is currently being fabricated to verify this design and to test design feasibility at higher frequencies. The OTA appears well suited to higher frequency applications,

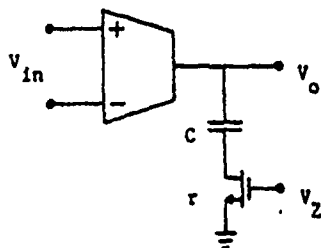


Fig. 6. (Compensated) OTA Integrator.

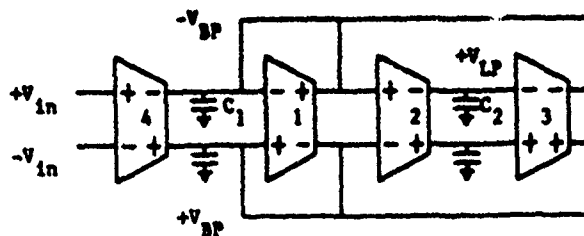


Fig. 7. OTA Filter Topology.

the input devices are fairly long ($W/L = 8\mu/60\mu$) for operation at 400 kHz . Simulations show that decreasing the input device length (L) to achieve larger OTA transconductances provides working designs above 1 MHz .

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Digitally Controlled Analog Signal Processing

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Introduction

Many signal processing applications involving continuous-time input and/or output signals exist. These applications are both linear and nonlinear, vary from low to high frequencies, and have specifications ranging from very lax to very stringent. Monolithic continuous-time signal processors have largely eluded IC designers for the past decade. This can be attributed primarily to the inability of researchers to solve many of the numerous technological challenges associated with analog signal processing.

Digital signal processing techniques have been successfully applied in a very useful but limited class of analog signal processing applications. The digital signal processing techniques have offered flexibility and simplicity but have been accompanied by high system costs and restricted to relatively low frequency and/or non-real-time applications. Aliasing, quantisation, warping, and algorithmic performance and sensitivity limitations pose continual challenges.

It is well known that monolithic continuous-time analog integrated circuits can ideally provide sophisticated signal processing capabilities in an area efficient manner over a very wide frequency range. This extends from the low audio range to frequencies well beyond 100 MHz where conventional circuits such as a simple digital inverter behave much as a lowpass filter.

Initially, the major practical limitations which have limited the development of monolithic analog integrated circuits are identified and quantified in this paper. Existing approaches and their fundamental limitations are discussed.

An architecture for a system which inherently compensates for the major factors which have limited the development of monolithic continuous-time integrated circuits is introduced. The architecture utilizes a precisely controllable analog signal path and a sophisticated digital controller in a control loop and is termed a Digitally Controlled Analog Signal Processor (DCASP). Within a predetermined range, both the functional characteristics

and specifications of the analog signal processor can be established via software input after silicon processing and packaging are complete. The structure is amenable for self-checking/self-correcting requirements as well as adaptive applications. Self testing features are also practical. The structure is applicable from low frequencies to very high frequencies. The DCASP is compatible with and scales with existing VLSI technologies.

The major emphasis in this paper is placed upon the DCASP architecture itself and on how this architecture can be used to simultaneously overcome the major technological limitations currently impeding the development of monolithic real-time continuous-time signal processing circuits.

Technological Challenges Facing the IC Designer

Numerous practical limitations are responsible for seriously limiting the evolution of monolithic analog integrated circuits. The major passive factors limiting the performance of these circuits are listed in Table 1. In addition to the passive factors, electrical noise of the passive and active devices and device nonlinearities further deteriorate performance.

- | |
|--|
| 1. Nominal Process Parameter Variations |
| 2. Statistical Process Parameter Spreads |
| 3. Large Temperature Coefficients |
| 4. Parasitic Resistors and Capacitors |
| 5. Passive Component Matching |
| 6. Active Component Matching |

Table 1. Major Passive Factors Limiting Performance of Monolithic Analog Circuits

The magnitude of the problem associated with the limitations of Table 1 can be best appreciated by considering the typical magnitude of these factors and their combined effects on typical system performance. For comparative purposes, emphasis will be placed on silicon MOS processes although similar phenomenon are observed in other technologies.

Parameter variations from the design target associated with processing are quite large. $\pm 50\%$ variations in sheet resistance, $\pm 100\text{mV}$ variations in oxide capacitor values of MOSFETs and $\pm 10\%$ variations in oxide capacitor values are typical. Variations in the transconductance parameter $K'(K' = \mu C_{ox})$ or less of percent are also common.

Chip level statistical parameter variations are somewhat smaller than the process parameter variations but are still significant. These variations are due to both local and global differences in the characteristics of silicon wafers across the die. Variations (mean standard deviation) of threshold voltages are in the 1mV to 30mV range and variations in K' range from 0.5% to 5% .

Temperature coefficients of passive and process parameters are significant. For example, the TCR of the sheet resistance of polysilicon is typically in the $0.1\%/^{\circ}\text{C}$ range.

Parasitic capacitors from plate to substrate associated with poly-poly capacitors are in the 1% to 30% range of the capacitor itself. Inherent parasitic resistors associated with poly strings, contacts and drain and source diffusions range upward from tens of ohms. Layout parasitics associated with interconnections are often somewhat larger. The parasitic capacitances associated with resistor strings are typically both distributed and voltage dependent.

With consideration in layout, ratio matching of capacitors to $\pm 0.1\%$ is possible. Practical resistor ratio matching is in the $\pm 3\%$ range (5micron feature size). Accurate ratio matching of parasitic components is more difficult.

Active component matching is poorer than passive component matching. For example, for a PNT resistor random variations in the 0.5% to 6% range are common.

The seriousness of the limitations of the factors in Table 1 can be appreciated only when one considers the specifications required in typical practical applications. Suffice it to say that many applications exist in all frequency ranges from low audio to many GHz. Effective RC products or component ratios can be practically controlled to between 0.1% and 1% accuracy.

The DCASP approach that is presented here has inherent compensation for all of the factors listed in Table 1, is applicable over a very wide frequency range, and can be used in medium precision as well as in some high precision applications.

DCASP Approach

A block diagram of the architecture of a simplified version of the Digitally Controlled Analog Signal Processor (DCASP) is shown in Fig. 1. Although this simplified

structure may not be optimal, it suffices to introduce the DCASP techniques and demonstrate the performance potential of this approach. The block diagram contains four basic components, the Controlled Signal Processor (CSP), the Performance Detector, the Exciter, and the Digital Controller. The first three components enclosed in the dashed curves represent analog circuitry that will appear on a single substrate. The Digital Controller may also be on the same substrate or may be external. The switch, S_1 , allows either the input signal or the output of the Exciter to be applied to the Controlled Signal Processor itself.

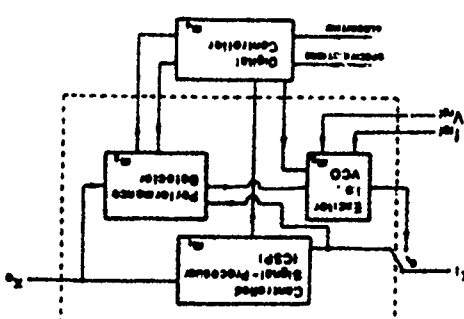


Fig. 1. DCASP Block Diagram

The basic operation of the system is very simple. S_1 is initially connected to the Exciter output. In this mode the Digital Controller "identifies" the Controlled Signal Processor by simultaneously identifying the three analog blocks: The Exciter, the Performance Detector, and the Controlled Signal Processor. Once the CSP is identified, the controllable components in the CSP are adjusted and latched to optimize performance of the CSP relative to the given specifications. Following optimization, S_1 changes states allowing the input signal to be applied to the CSP. All signal processing then takes place in the optimized analog CSP. Comments about the operation of each of the blocks and the overall system follow.

The Controlled Signal Processor should be designed to allow for adjustment of a large number of key parameters and functions. Large adjustment range and fine resolution for all components is important. For example, if the CSP is designed to act as a filter, a group of multiple input lossy integrators in which the loss and the unity gain frequency associated with each input are all independently adjustable over a wide range might serve as the basis for the CSP. By appropriately interconnecting these devices via the Digital Controller and adjusting the components to optimize performance, a universal precision filter structure is possible. For audio frequency applications, the adjustable components might be binarily weighted resistors and capacitors or switched capacitors or higher-level programmable structures such as Operational Transconductance Amplifiers (OTAs). Continuously adjustable rather than quantized components are also possible. A typical grid (in the s-plane) depicting by intersection of grid lines the possible pole locations of a filter constructed using this technique

unique with quantised component values is shown in Fig. 2. Methods of selecting the adjustable quantised components to obtain maximal resolution for specific applications are discussed in the literature⁶.

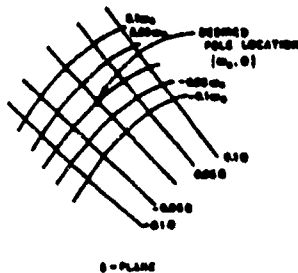


Fig. 2. Possible pole locations in a DCASP based active filter

The Exciter provides an excitation or sequentially, multiple excitations for the CSP during the identification state. Depending on the application, typically only f_{ref} or V_{ref} will be required. The exact value of these references is not critical but they must be known and stable. The identification and optimisation problem simplifies if multiple inputs (but a fixed single reference) are sequentially applied by the Exciter. Considering again the filter example, the Exciter may consist only of a non-precision voltage-controlled oscillator (VCO). The Digital Controller is used to sequentially set the Exciter (i.e., VCO) operating frequency. The "exact" frequency of oscillation for each step in the VCO sequence is not critical but can be precisely determined with a modest amount of circuitry if f_{ref} is known.

The Performance Detector is used to measure the performance of the CSP itself. If one were to attempt to identify only the CSP, the required specifications for the design of the Performance Detector would typically be quite challenging. By also identifying the Performance Detector and Exciter, the specifications required for these devices will be modest. For algorithmic simplicity, the Performance Detector may also be made to be tunable by the Digital Controller. Considering again the filter example, the Performance Detector may be no more than a voltage comparator or a generic analog to digital converter. Nonideal characteristics of the Performance Detector, such as offset voltages (as a function of common mode input) may be identified and/or adjusted by the Digital Controller. Slew rate and hysteresis effects may also be identified or, in some applications, ignored.

The Digital Controller is used to monitor the performance of the system during the identification or pretune state. Based upon the output of the Performance Detector for each excitation supplied by the Exciter, the system is adjusted to optimally meet the specifications established for the CSP. The desired specifications must be stored in nonvolatile memory. For high-volume applications, tuning algorithms may be fixed in hardware. Once tuned, the Digital Controller may either power-down or enter a standby state in which it monitors portions of the system. Since the

Digital Controller is not in the signal path, it is not needed for real-time operation. Since the pretune speed is typically not critical, the size and capabilities of the controller can be quite modest. Tradeoffs between algorithmic tuning complexity and capabilities of the Digital Controller can be made.

Referring back to the technological limitations of Table 1 which plague the continuous-time IC designer, it should be apparent that if an acceptable tuning strategy can be developed, and if the CSP has sufficient range and resolution so that the domain of realizable specifications (henceforth termed the tuning domain) intersects with the desired specifications (henceforth termed the specification domain), then the DCASP structure will be inherently unaffected by nominal process parameter variations, statistical process parameter spreads, parasitic resistors and capacitors as well as passive and active component matching.

If temperature changes after the initial trimming, several alternatives exist for temperature compensation. In those applications where the signal path can be periodically interrupted, the CSP structure can be re-calibrated. The Digital Controller can also monitor die temperature and make on-line corrections based upon nominal temperature characteristics of the devices. A dual signal path architecture in which the input signal is alternately applied to the two paths and in which the un-excited path is off-line calibrated is also possible.

High Frequency Applications

At high frequencies (10MHz to 200MHz) few techniques exist for signal processing on silicon. This can be attributed primarily to the relative significance of parasitic capacitances associated with both the passive and active devices as well as with the layout at these frequencies. As a consequence, at high frequencies drastic and non-controllable deterioration in the characteristics of amplifier structures is experienced rendering them impractical. This precludes the practical application of either SC or continuous-time active filters in this frequency range.

It has been demonstrated⁶ that continuous-time circuits can "operate" at much higher frequencies than their digital counterparts. The main limitation of high frequency monolithic continuous-time circuits is the inability of designers to precisely control the characteristics of the analog circuits. To demonstrate the high frequency performance capabilities of continuous-time circuits, consider the high frequency bandpass filter of Fig. 3. This circuit is basically the cascade of three "digital" inverters configured in a feedback structure.

The frequency response of this circuit as obtained from a SPICE simulation for several different values of I and V is shown in Fig. 4. In the simulation of this simplified circuit, the multiple-output current mirror and buffer amplifiers were assumed ideal, loading capacitors of 0.1pf

were connected to signal nodes, and the MOSFETs were characterized by parameters of a typical 5μ CMOS process. A dc level control was used to keep the quiescent output voltage constant. Potential for adjusting the characteristics of very high frequency circuits via dc control variables should be apparent from this example. If a good control structure to automatically adjust the characteristics of this circuit is developed, such as using the DCASP architecture of Fig. 1, precision high frequency performance is possible.

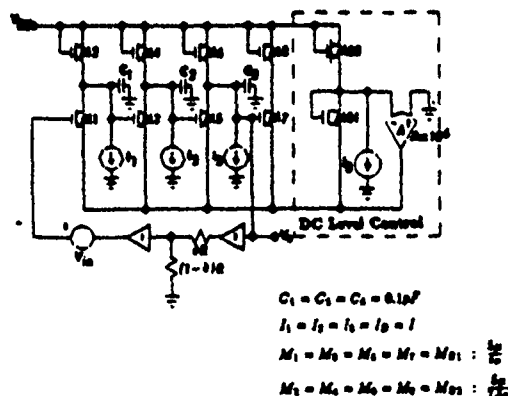


Fig. 3. Simplified High Frequency ω_o and Q Controllable Bandpass Filter

Conclusions

A new architecture for monolithic continuous-time precision signal processing has been introduced. The architecture employs a tunable non-precision signal processing path and a digital controller for precisely electronically tuning the signal path in the field. The DCASP structures are inherently insensitive to the major technological limitations plaguing other monolithic continuous-time approaches; namely, process variations, process parameter spreads, temperature variations, aging, parasitic resistor and capacitors as well as resistor and capacitor matching.

The DCASP architecture is amenable to a host of linear and non-linear signal processing applications over a wide range of frequencies. It is versatile in that it allows for post fabrication tailoring of circuit functions and specifications. It can be used in adaptive applications. It is microprocessor compatible and can be configured for self-testing and self-correcting operation.

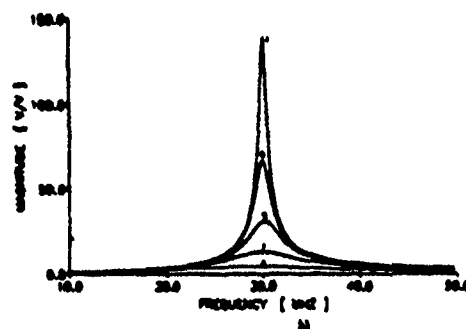
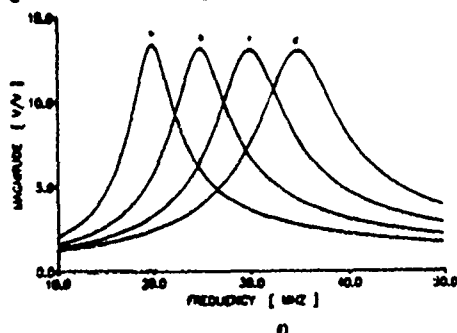


Fig. 4. Simulated Frequency Response for Circuit of Fig. 3 for various values of I and ν (Curve designations are in Table 3). a) Constant BW, Variable f_o , b) Constant f_o , variable BW

Plot	μA	ν/V	Plot	μA	ν/V
a	48.80	0.0571	e	25.80	0.310
b	38.34	0.1875	f	31.75	0.2671
c & f	30.17	0.2000	g	26.67	0.2671
d	31.25	0.613	h	34.65	0.343

Table 2. Parameters for Plots of Fig. 4

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A 1-MHZ VOLTAGE-CONTROLLED CONTINUOUS-TIME BANDPASS/LOWPASS FILTER USING LINEARIZED CMOS OTAs

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ABSTRACT

The design and implementation of a continuous-time bandpass/lowpass filter with voltage-controlled center frequency and Q is presented. The circuit uses a linearized CMOS transconductance element as the basic integrating block. A voltage-controlled phase-adjusting scheme is employed in the integrator to compensate for excess phase in the transconductance at high frequencies. The fabricated filter readily achieves the nominal design-center frequency of 1 MHz with $Q = 10$, and provides output signal swings up to $4V_{p-p}$ with 1 % distortion.

INTRODUCTION

Recently, there has been considerable interest in the design and implementation of fully monolithic continuous-time analog signal-processing circuits [1-3]. Such circuits overcome certain inherent limitations of switched-capacitor networks arising due to their sampled-data nature [4]. In particular, the advantages of continuous-time processing become increasingly apparent as operating frequencies are raised well beyond the audio range. A basic requirement for realizing accurate and stable continuous-time filters is a filter block having time-constants that are controllable using a voltage or current, thereby allowing the realized filter to be tuned on chip against process and temperature variations. This paper describes the design and implementation of a voltage-tunable filter block capable of realizing cut-off frequencies in excess of 1 MHz. The circuit is a second-order bandpass/lowpass structure using a CMOS operational transconductance amplifier (OTA) as the basic active element. The OTA employs a linearized input stage which dynamically adjusts the bias current of a differential pair to cancel out nonlinearities of the MOSFETs over a wide input voltage range. A voltage-controlled phase adjusting scheme is employed in the OTA integrators to compensate for the excess phase of the OTAs at high frequencies.

PHASE COMPENSATED OTA INTEGRATOR

Fig. 1 shows the schematic diagram of a phase-compensated integrator using an OTA whose transconductance g_m is adjustable by a control voltage V_C . It is as-

sumed that, at frequencies of interest, the high-frequency behavior of the OTA can be modelled by a single-pole frequency dependent transconductance of the form

$$g_m(s) = \frac{g_{m0}}{1 + s\tau} \quad (1)$$

where g_{m0} is the transconductance value at low frequencies and τ is a high-frequency time constant. This model is fairly accurate at normal operating frequencies where $|s| \ll \tau$. The resulting transfer function of the integrator is obtained as

$$A_I(s) = \frac{g_{m0}}{sC} \left(\frac{1 + sCr_d}{1 + s\tau} \right) \quad (2)$$

where

$$r_d \approx \frac{\mu_n C_{ox} W}{L} (V_P - V_T) \quad (3)$$

is the small-signal drain resistance of MP in Fig. 1. In the above equation, W and L are, respectively, the channel width and length of device MP , while the parameters μ_n , C_{ox} and V_T have their usual significance [5]. Note that transistor MP introduces a high-frequency zero in the transfer function of the integrator. Since r_d depends on the gate-source voltage V_P , the location of this zero is voltage-adjustable. The phase lead due to this zero can then be used to compensate for the excess phase lag within the OTA itself. That is, if V_P is adjusted to make $Cr_d = \tau$, exact phase compensation is achieved. Assuming that the initial phase error is not large, the zero frequency required for compensation is much higher than the unity-gain bandwidth of the compensated integrator. Therefore, at frequencies of interest, the signal voltage across the compen-

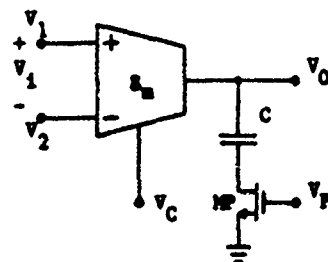


Fig. 1 Phase compensated OTA integrator

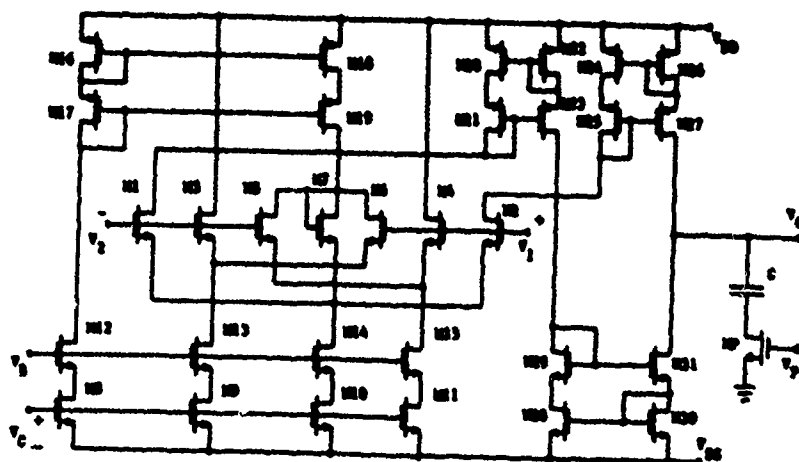


Fig. 2 Integrator using linearised CMOS OTA

sating device MP is very small, resulting in negligible distortion due to the nonlinearity of this device [6].

Fig. 2 shows a CMOS realization of the complete integrator. It employs a linearised transconductance circuit ($M_1 - M_{17}$) which provides a voltage-controlled low-frequency transconductance given by the relation

$$g_{mo} = K(V_C - V_T) \quad (4)$$

where K is a constant dependent on process parameters and the geometries of the input and biasing devices [6]. The quantity V_B is a constant bias voltage. Details of circuit design and the linearization scheme employed are discussed elsewhere [6,7] and are not repeated here. The integrator in Fig. 2 was fabricated using a standard 3μ double-poly p -well CMOS process [8]. Fig. 3 depicts the nonlinearity in the measured $i - v$ characteristics of the OTA as a percentage of a 2 V (peak) full-scale value. The observed nonlinearity is less than 1% for input voltages in the range between -2.4 V and +2.4 V. The circuit consumes 10 mW with the nominal bias values, and exhibits a short-circuit 3-dB bandwidth of 15 MHz.

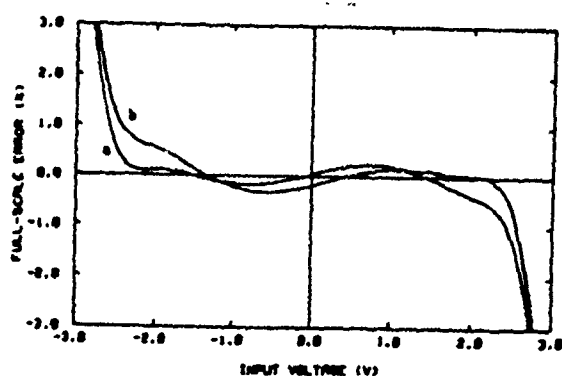


Fig. 3 Measured nonlinearity in OTA $i - v$ characteristics for $V_{DD} = -V_{SS} = 5V$, $V_B = -2.5V$, $V_C = 1.75V$, $V_o = 0$; Curve (a) Input V_1 , $V_2 = 0$; Curve (b) Input V_2 , $V_1 = 0$

FILTER REALIZATION

The schematic diagram in Fig. 4 shows the proposed test filter structure. It is simply a version of the well known two-integrator loop using the OTA integrator of Fig. 2 as a basic building block. OTAs g_{m1} and g_{m2} along with capacitors C_1 and C_2 form the integrators, while an additional OTA g_{m3} provides the required loss to obtain finite Q . With an input signal V_i the outputs V_{BPF} and V_{OLP} provide second-order band-pass and low-pass responses respectively. Assuming that $|s| \ll \omega_c$ and $|s| \ll C\omega_c$ in the frequency range of interest, a straightforward analysis using (1) and (2) gives the following relations for the bandpass center frequency ω_o and quality factor Q of the filter

$$\omega_o \approx \omega_c \quad (5)$$

$$Q \approx \frac{\hat{Q}}{1 - \hat{Q}(\tau_1 + \tau_2 - C_1\tau_{d1} - C_2\tau_{d2})} \quad (6)$$

where

$$\hat{\omega}_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (7)$$

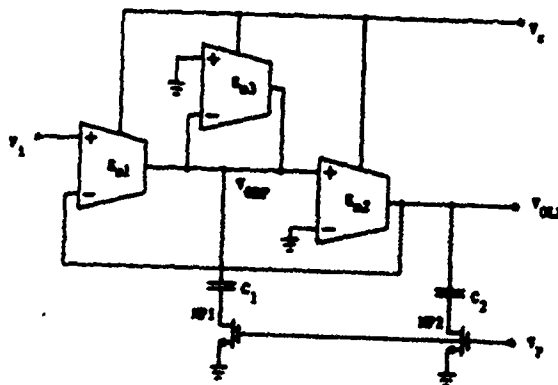


Fig. 4 Second-order bandpass/lowpass filter

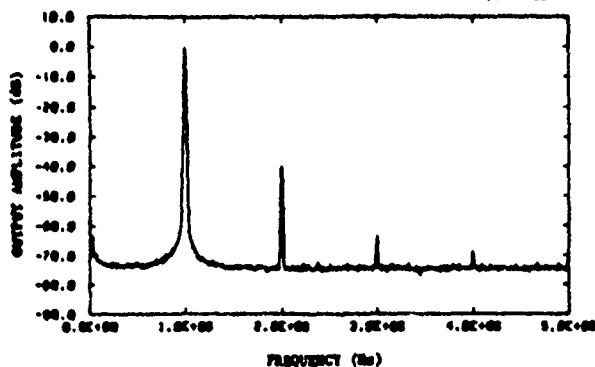


Fig. 7 Distortion spectrum of 1MHz bandpass filter for a $4V_{DD}$ output at 1MHz

CONCLUSION

The design and implementation of a second-order continuous-time filter with voltage-controlled center frequency and Q has been presented. Experimental results demonstrate the viability of continuous-time processing in the MHz range using a standard 3μ CMOS technology. The voltage-control feature allows this filter to be tuned on-chip against process and temperature variations using known tuning schemes [3, 9]. The implementation of higher-order filters obtained by cascading the proposed second-order block is presently under investigation.

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March 31, 1988

APPENDIX C

Instrumentation/Measurement Equipment Specifications

The following is a set of manufactured published equipment specifications for those pieces of equipment or instrumentation that were required in testing the overall DCASP architecture and its components. Specifically, the following equipment specifications are contained in this Appendix.

- Hewlett Packard Spectrum Analyzer, Model 3585A
- Hewlett Packard *pA* Meter/DC Voltage Source, Model 4140B
- Hewlett Packard LF Impedance Analyzer, Model 4192A
- Tektronix Digital Storage Oscilloscope, Model 468
- Tektronix Oscilloscope, Model 2465
- Hewlett Packard Synthesizer/Function Generator, Model 3325A
- Hewlett Packard Pulse Generator, Model 8082A
- Hewlett Packard 100MHz Universal Counter, Model 5316A
- Hewlett Packard Waveform Recorder, Model 5180A
- Tektronix Digital Multimeter, Model DM 501A
- Tektronix 40MHz Function Generator, Model FG 504

Hewlett Packard Spectrum Analyzer, Model 3585A

The following is an excerpt of *Service Manual — Model 3585A Spectrum Analyzer*, Vol. 1. Colorado: Hewlett-Packard Company, Aug. 1981, pp. 1-5 through 1-10.



**HEWLETT
PACKARD**

SERVICE MANUAL

MODEL 3585A

SPECTRUM ANALYZER

Serial Numbers: 1750A00716 and greater

WARNING

*To help minimize the possibility of electrical fire
or shock hazards, do not expose this instrument
to rain or excessive moisture.*

VOLUME I

Manual Part No. 03585-90006

Microfiche Part No. 03585-90056

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Printed: August 1981

1-8. Recommended Test Equipment

Equipment required to maintain the Model 3585A is listed in Table 1-2. Other equipment may be substituted if it meets the requirements listed in the table.

Table 1-1. Specifications

NOTE

Specifications are guaranteed only when the Auto Calibration is on, the OVEN REF OUT is connected to the EXT REF IN and the instrument has warmed up at least 20 minutes at the ambient temperature.

FREQUENCY:

Measurement Range:

20 Hz to 40.1 MHz

Displayed Range:

Frequency Span:

0 Hz to 40.1 MHz Settable with 0.1 Hz resolution
10 Hz to 40 MHz in 1, 2, 5 steps

Accuracy:

-0% +0.2% of Frequency Span setting

Marker:

Readout Accuracy:

$\pm 0.2\%$ of Frequency Span \pm Resolution Bandwidth

Counter Accuracy:

$\pm 0.3 \text{ Hz} \pm 1 \times 10^{-7}/\text{month}$ of counted frequency for a signal 20 dB greater than other signals and noise in the resolution bandwidth setting.

Manual Frequency Accuracy:

$\pm 0.1 \text{ Hz} \pm 1 \times 10^{-7}/\text{month}$ using the internal reference.

Resolution:

Resolution Bandwidths

3 dB bandwidths of 3 Hz to 30 kHz in a 1, 3, 10 sequence

Accuracy

$\pm 20\%$ at the 3 dB points

Selectivity (Shape Factor)

60 dB/3dB < 11:1

AMPLITUDE:

Measurement Range:

Terminated (50/75 Ω) input

-137 dBm to +30 dBm or equivalent level in dBV or volts

High Impedance (1 M Ω) input

31 nV to 22V

Table 1-1. Specifications (Cont'd)

Displayed Range:**Vertical Scale:**

10 division CRT settable to 10, 5, 2 and 1 dB/division relative to the Reference Level (which is represented by the top graticule line)

Input Range:

-25 dBm to +30 dBm in 5 dB steps

Reference Level (relative to Input Range):**Settability**

-100 dB to +10 dB; 0.1 dB resolution

Accuracy (at Center Frequency, for Sweep Time \geq 2 steps above auto setting at Manual Frequency, 1 or 2 dB/Div.)

Add 0.1 dB for auto sweep setting

Add 0.1 dB for 5 or 10 dB/Div.

Terminated (50/75 Ω) input

+10 dB -50 dB -70 dB -90 dB

± 0.4 dB	± 0.7 dB	± 1.5 dB
--------------	--------------	--------------

High Impedance (1 M Ω) input—add to above

20 Hz 10 MHz 40.1 MHz

± 0.7 dB	± 1.5 dB
--------------	--------------

Amplitude Linearity (referred to Reference Level):

0 dB -20 dB -50 dB -80 dB -95 dB

± 0.3 dB	± 0.6 dB	± 1.0 dB	± 2.0 dB
--------------	--------------	--------------	--------------

Frequency Response (referred to center of span):

Terminated (50/75 Ω) input $\pm .5$ dB

High Impedance (1 M Ω) input

20 Hz 10 MHz 40.1 MHz

± 0.7 dB	± 1.5 dB
--------------	--------------

Marker:**Amplitude Accuracy:**

Center Frequency or Manual frequency at the Reference Level: Use Reference Level accuracy from +30 dBm to -115 dBm, add Amplitude Linearity below -115 dBm.

To Calculate Marker Accuracy:**Terminated (50/75 Ω) input**

At the Center or Manual Frequency and at the Reference Level - use Reference Level Accuracy.

At the Center or Manual Frequency and NOT at the Reference Level - add Reference Level Accuracy and Amplitude Linearity.

NOT at the Center or Manual Frequency and NOT at the Reference Level - add Reference Level Accuracy, Amplitude Linearity and Frequency Response.

High Impedance (1 M Ω) input

Calculate the Marker Accuracy according to the Terminated Input rules above, then add 1 M Ω Reference Level Accuracy.

Table 1-1. Specifications (Cont'd)

INPUT:**Signal Inputs:**

Terminated (50/75 Ω) input; > 26 dB return loss, DC coupled, BNC connector. Applied dc voltage must be \leq ten times the RANGE setting in volts for full specification compliance.

High Impedance (1 M Ω) input; $\pm 3\%$ shunted by < 30 pF, BNC connector

Maximum Input Level:

Terminated (50/75 Ω) input; 13 V peak ac plus dc, relay protected against overloads to 42 V peak.

High Impedance (1 M Ω) input; 42 V peak ac plus dc (derate ac by a factor of two for each octave above 5 MHz).

External Reference Input:

10 MHz (or subharmonic to 1 MHz), 0 dBm to +15 dBm/50 Ω

Required frequency accuracy, $\pm 5 \times 10^{-6}$. When an external reference is used the $\pm 1 \times 10^{-7}$ /month specification on the Counter and Manual frequency accuracy is replaced by the accuracy of the external reference.

OUTPUT:**Tracking Generator:****Level**

0 dBm to -11 dBm/50 Ω with a single turn knob, continuously variable

Frequency Accuracy

± 1 Hz relative to analyzer tuning

Frequency Response

± 0.7 dB

Impedance

50 Ω ; > 14 dB return loss

Probe Power:

+15 Vdc, -12.6 Vdc; 150 ma max.

Suitable for powering HP 1120A Active Probe

External Display

X, Y: 1 volt full deflection;

Z: < 0V to > 2.4 V.

Recorder:

X Axis: minimum of +10 Vdc full scale

Y Axis: +10 Vdc full scale

Z—penlift output (TTL levels)

IF:

350 kHz, -11 dBV to -15 dBV at the reference level

Video:

+10 Vdc at the reference level

Frequency Reference:

10.000 MHz $\pm 1 \times 10^{-7}$ /mo., > +5 dBm into 50 Ω

Table 1-1. Specifications (Cont'd)

DYNAMIC RANGE:

Spurious Responses: (which includes image, out of band and harmonic distortion) referred to a single signal whose amplitude is \leq RANGE setting and whose frequency is \geq ten times the Resolution Bandwidth.

Terminated (50/75 Ω) input

< -80 dB

High Impedance (1 M Ω) input

< -80 dB; except second harmonic distortion, < -70 dB

Intermodulation Distortion: for two signals, each at least 6 dB below the RANGE setting and separated in frequency by at least 100 Hz, referred to the larger of the two signals.

Terminated (50/75 Ω) input

< -80 dB; except 2nd order IM with one or both of the input signals within the range of 10 MHz to 40 MHz, < -70 dB

High Impedance (1 M Ω) input

< -70 dB

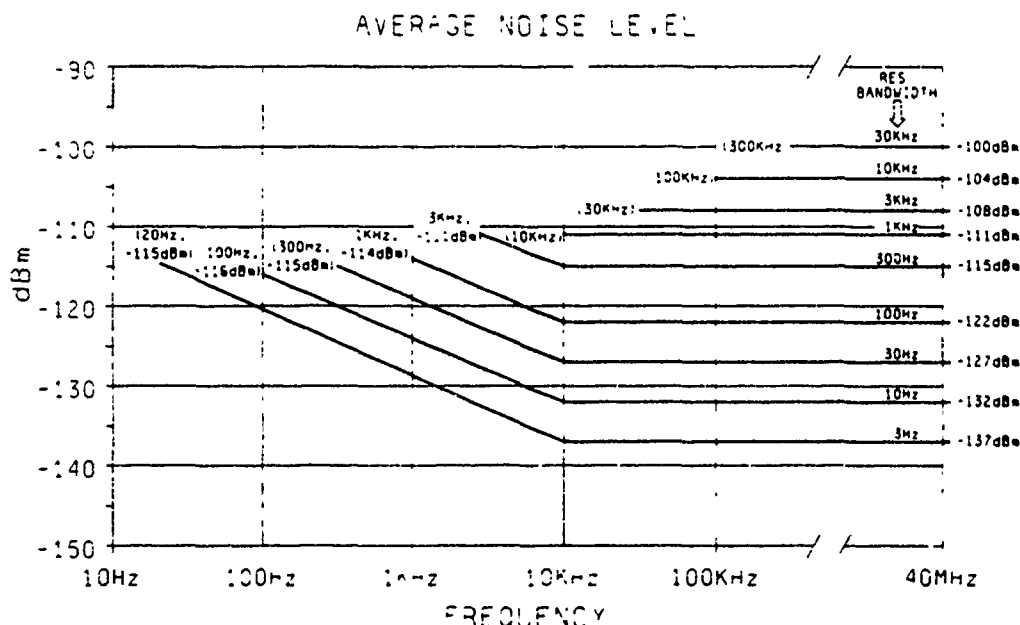
Residual Responses (no signal at input, -25 dBm Range)

< -120 dBm

Lo Feed Through:

< -15 dB with respect to Range

Average Noise Level (-25 dBm Range), 50/75 Ω input)



1 M Ω input: Below 500 kHz add 12 dB to above.

Average Noise Level at 40 Hz (3 Hz Res. BW) using the Noise Level Key
-123 dBm (1 Hz)

Table 1-1. Specifications (Cont'd)

DISPLAY:**Traces:**

Two memories, A and B, each 1001 data points horizontally by 1024 data points vertically are displayed on the CRT at a flicker free rate.

Memory A - updated at the rate of the analyzer sweep time.

Memory B - updated by transfer from A (Store A-B).

Max Hold - retains in Memory A the largest signal level at each horizontal point over successive sweeps.

A-B - updates Memory A with sweep data minus Memory B data at each corresponding horizontal point.

Trace Detection:

A linear envelope detector is used to obtain video information from the IF signal. Peak signal excursions between horizontal sweep data points are retained and displayed at the left-hand data point. This assures that no signal responses are missed.

SWEEP:**Modes:**

Continuous, Single or Manual

Trigger:

Free Run, Line, or External

Time:

Resolution: 0.2 sec

Minimum: 0.2 sec

Maximum: Frequency Span/minimum sweep rate limit

The minimum sweep rate limit is:

≥ 10 kHz Res BW - 10 sec/Hz of Frequency Span or 0.1 Hz/sec

≤ 3 kHz Res BW - 200 sec/Hz of Frequency Span or 0.005 Hz/sec

GENERAL:**Environmental:****Temperature:**

Operating 0°C to 55°C

Humidity:

< 95% RH except 300 Hz Res. BW, < 40% RH

Warm-up Time:

20 minutes at ambient temperature

Power Requirements:

115 V (+11% - 25%), 48-440 Hz

230 V (+11% - 18%), 48-66Hz

< 180 watts, 3A max.

Weight:

39.9 kg (88 lb)

Dimensions:

22.9 cm (9 in) H x 42.6 cm (16.75 in) W x 63.5 cm (25 in) D

Remote Operation:

Compatible with IEEE Standard 488-1975 "Standard Digital Interface for Programmable Instrumentation"

Table 1-2. Recommended Test Equipment

Instrument	Required Characteristics	Usage		Recommended Model
		Semi Automatic Performance Test	Operational Verification Tests	
Audio Oscillator	Frequency 1 kHz Distortion \leq 90dB Amplitude 0.1Vrms	x	x	hp-339 or hp-239
Attenuator Variable 10dB/Step Variable 1dB/Step See Note 1	Range: 0 - 120dB Range 0 - 12dB	x x	x x	hp-355D hp-355C
Bridge, Directional 50 Ω 75 Ω See Note 2, 3	Frequency 0.1 - 40 MHz Return Loss $>$ 30dB Directivity $>$ 40dB	x x	x x	hp-8721A hp-8721A Option 008
Calculator	Compatible with hp-9825A Software and I/O	x		hp-9825
Calculator ROM's	HP-IB* and hp-9825A Compatible	x		hp-98210A and hp-98213A
Filter 9MHz Low Pass	See Figure 4-14	x	x	
Frequency Counter	Range 5 to 10 MHz Resolution 0.1 Hz Accuracy \pm 1 count, \pm 5x10 ⁻¹⁰ /day	x	x	hp-5328A Option 010
Frequency Synthesizer	Freq. Range 200 Hz to 40.1 MHz Amp. Range -10 to 85 dBm Amplitude Accuracy \pm 0.25 dBm	x	x	hp-3335A
Frequency Synthesizer	Freq. Range 1 kHz to 33 MHz Amplitude Range 25 dBm Amplitude Accuracy \pm 0.4 dB	x	x	hp-3330B
Function Generator See Note 3	Frequency 1 - 2 kHz Square Wave 100ns rise time dc Offset \pm 1V	x		hp-3311A
HP-IB* Interconnection Cables		x		hp-10631
HP-IB* Interface Cable	hp-9825A Compatible	x		hp-98034A
Impedance Matching Network (50 Ω to 75 Ω Minimum Loss Pad)	Frequency 0.1 to 40 MHz VSWR $<$ 1.05	x	x	hp-8542B
Mixer Double Balanced See Note 3	Frequency 0.1 - 40 MHz	x		hp-10534
Oscilloscope See Note 2	Vertical Scale \geq 5 mV/Div Horizontal Scale \geq 50 nsec/Div		x	hp-1740A
Power Supply DC See Note 4	Voltage range 0 - 10 V DC	x		hp-6213A
Printer Impact Summer	Plotter Capability See Figure 4-15	x x	x	hp-9871A
Termination Feedthrough 50 Ω 75 Ω	\pm 0.1 ohm 1 Watt	x x	x x	hp-11048C hp-11094C
Thermal Voltage Converter 50 Ω , 0.5 V See Note 4	Frequency 0.1 - 60 MHz Calibration Data	x		hp-11051A Option 01
Voltage Divider 10 to 1 Terminated in 50 Ω See Note 4	See Figure 4-7	x		
Voltmeter Digital See Note 4	Full Scale Range 1Vdc Accuracy \pm 0.004% Resolution 6 Digits Input Resistance $>$ 1 M Ω	x		hp-3455A

NOTES

- 1 Attenuator must be calibrated by standards lab. Correction factors are required for the Operational Verification Tests
- 2 Required for the Operational Verification Return Loss Test
- 3 Required for the Semi Automatic Performance Test Return Loss procedure
- 4 Required to run the calibrator accuracy program

*Hewlett Packard Interface Bus

Hewlett Packard pA Meter/DC Voltage Source, Model 4140B

The following is an excerpt of *Hewlett Packard pA Meter/DC Voltage Source, Model 4140B*, Yokogawa-Hewlett-Packard, Ltd. Sept. 1983.



**HEWLETT
PACKARD**

OPERATION AND SERVICE MANUAL

MODEL 4140B
pA METER/DC VOLTAGE SOURCE

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed 2034J.

With changes described in Section VI, this manual also applies to instruments with serial numbers prefixed 2129J.

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9-1, TAKAKURA-CHO, HACHIOJI-SHI, TOKYO, JAPAN

Manual Part No. 04140-90021
Microfiche Part No. 04140-90071

Printed: SEP. 1983

Table 1-1. Specifications(Sheet 1 of 7).

Measurement Functions: I-V, C-V and I

I: For independent operations as universal pA Meter/Programmable Voltage Source













I-V: I-V characteristic measurement using staircase/ramp wave

C-V: Quasi-Static C-V characteristic measurement using ramp wave

Voltage Source: Two separate sources (VA and VB)

: $\pm 100V$, function generator/programmable source

: $\pm 100V$, programmable DC voltage source

Function	VA	VB
I-V	 ,  ,  , 	
C-V	 , 	
I	 ,  ,  ,  , 	

Voltage Sweep: Auto (pause available)/Manual

Warm-up Time: ≥ 1 hour

GENERAL

Operating Temperature: $0^{\circ}C$ to $40^{\circ}C$

Relative Humidity: $\leq 70\%$ at $40^{\circ}C$

Power: $100/120/220V \pm 10\%$, $240V - 10\% + 5\%$, $48Hz \sim 66Hz$, max. $135VA$ with any option.

Dimensions: $426mmW \times 177mmH \times 498mmD$

Weight: Approx. $14.4kg$

Accessory Furnished: 16053A Test Leads (1 set), 16055A Test Fixture.

Table 1-1. Specifications(Sheet 2 of 7).

CURRENT MEASUREMENT

Display: 3-1/2 digit, 99.9% overrange.

Measurement Range: $\pm 0.001 \times 10^{-12} \text{ A} \sim \pm 1.999 \times 10^{-2} \text{ A}$, 11 ranges, auto/manual range selection.

Measurement Accuracy/Integration Time:

Range(A)	Measurement Accuracy*	Integration Time(ms)**		
		SHORT	MED	LONG
$10^{-2} \sim 10^{-9}$	$\pm (0.5 + 2)$	20	80	320
10^{-10}	$\pm (2 + 2)$			
10^{-11}	$\pm (5 + 3)$	80	320	1280
10^{-12} ***	$\pm (5 + 8)$	160	640	2560

* \pm (% of rdg + counts), $23^\circ\text{C} \pm 5^\circ\text{C}$, $\leq 70\%$ humidity, integration time...LONG, filter...ON.

** at 50Hz line frequency (x 5/6 at 60Hz operation).

*** Zero offset is performed.

Voltage Burden: $\leq 10\mu\text{V}$ at full scale.

Internal Electromotive Force: $\leq 100\mu\text{V}$ at $23^\circ\text{C} \pm 5^\circ\text{C}$.

Maximum Input:

Hi-Lo (peak value): $\pm 2\text{V}$ at $10^{-2} \sim 10^{-3} \text{ A}$ range.
 $\pm 30\text{V}$ at $10^{-4} \sim 10^{-5} \text{ A}$ range.
 $\pm 120\text{V}$ at $10^{-6} \sim 10^{-12} \text{ A}$ range.

Lo-Guard: $\pm 200\text{V}$.

Zero Offset: Cancels leakage current of test leads/fixtures.

Offset Ranges: $0 \sim \pm 100\text{fA}$.

Trigger: INT/EXT or MAN.





High Speed I Data Output: Outputs current measurement data with max. 4ms intervals. (Refer to reference data for accuracy).

Input Terminal: Triaxial BNC (HP Part No.: 1250-0687).

Table 1-1. Specifications(Sheet 3 of 7).

DC VOLTAGE SOURCE (V_A AND V_B)

Output Mode:

V_A: , , , , ==, OFF
V_B: ==, OFF

Voltage Range: 0 ~ ±10.00V, 0 ~ ±100.0V, 2 ranges (autoranging only).

Max. Current Capacity: 10mA.

Sweep Control: Auto (pause available)/man., up/down manually available in hold.

Operating Parameters Setting Ranges:

Start/Stop/DC Voltage: 0 ~ ±10.00V in 0.01V steps, 0 ~ ±100.0V in 0.1V steps



Step Voltage: ±0.01V ~ ±10.00V in 0.01V steps (0.1V step at 10V of absolute value of output voltage)

Hold Time: 0 ~ 199.9s in 0.1s steps, 0 ~ 1999s in 1s steps.

Step Delay Time: 0 ~ 10.00s in 0.01s steps, 0 ~ 100.0s in 0.1s steps.

Ramp Rate (dV/dt): 0.001V/s ~ 1.000V/s in 0.001V/s steps.

Accuracy: at (23°C ± 5°C)

Output Voltage (, , ==):

±10V: ±(0.07% + 11mV).

±100V: ±(0.09% + 110mV).

Accuracy of Ramp Voltage* :

Ramp Rate: ±(0.2% + 10_μV/s) - $\frac{10^{-4} \times \text{START Voltage (V)}}{\text{HOLD TIME (s)} + 2\text{s}}$

±(0.2% + 80_μV/s) - $\frac{10^{-4} \times \text{START Voltage (V)}}{\text{HOLD TIME (s)} + 2\text{s}}$

- - if absolute setting value for START or STOP Voltage > 10V.

Linearity:

±{0.1% + $\frac{0.0003\text{V/s}}{\text{RAMP RATE (V/s)}}$ } - $\frac{0.01 \times \text{START Voltage (V)}}{\text{RAMP RATE (V/s)} \times (\text{HOLD TIME (s)} + 2\text{s})}$ %

±{0.2% + $\frac{0.003\text{V/s}}{\text{RAMP RATE (V/s)}}$ } - $\frac{0.01 \times \text{START Voltage (V)}}{\text{RAMP RATE (V/s)} \times (\text{HOLD TIME (s)} + 2\text{s})}$ %

- - if absolute setting value for START or STOP voltage > 10V.

- * : 1. Temperature Change: ≤ 3.6°C/hour.
2. Time after start of ramp ≥ 2s.

Table 1-1. Specifications (Sheet 4 of 7).

Start Stop Voltage (only for \nearrow , \searrow): $\pm 20\text{mV}$
($\pm 200\text{mV} \dots \geq 10\text{V}$ of absolute setting value for START or STOP voltage).

Display of Output Voltage (only for \nearrow , \searrow): $\pm(0.07\% + 16\text{mV})$
($\pm 0.09\% + 160\text{mV}$) $\geq 10\text{V}$ of absolute setting value for START or STOP voltage).

Step Delay/Hold Time: Accuracy is dependent on accuracy of line frequency
(50Hz or 60Hz).

Current Limit: 10^{-4}A , 10^{-3}A or $10^{-2}\text{A} \pm 10\%$.

Output Terminals: BNC, L-GND.

C-V MEASUREMENT

Calculation Equation $C(F) = \text{measured current value (A)} / \text{ramp rate (V/s)}$

Measurement Range: $0.0\text{pF} \sim 199.9\text{pF}$, $200\text{pF} \sim 1999\text{pF}$, 2 ranges of Auto range.

% change Display: Capacitance change is displayed as a % of the initial setting value of C_{ox} (100%).

% Display Range: $0.0\% \sim 199.9\%$.

C_{ox} Setting Range: $0.1\text{pF} \sim 199.9\text{pF}$, $200\text{pF} \sim 1999\text{pF}$.

Capacitance Calculation Accuracy: Depends on accuracies of both current measurement and linearity of ramp wave
(refer to paragraph 3-53).

Zero Offset: Cancels stray capacitances of test leads/fixtures.

Offset range: $0 \sim 100\text{pF}$.

Table 1-1. Specifications(Sheet 5 of 7).

OTHER

Analog Output:

Output Data: V_A , I and C

Output Voltage:

Output Data	Output Voltage (Resolution)
V_A $\pm 10V$ $\pm 10.1V \sim \pm 100V$	$0 \sim \pm 1.000V$ (1mV/count) $\pm 1.01 \sim \pm 10.00V$ (10mV/count)
I Full Scale	$\pm 5V$ (5mV/count)
C Full Scale 100pF 1000pF 100% (% Display)	0.5V (0.5mV/count) 5V (5mV/count) 5V (5mV/count)

Accuracy: $\pm(0.5\% + 20mV)$

Low Pass Filter: OFF, 0.22s $\pm 20\%$ and 1s $\pm 20\%$ applied to both V_A and I/C Data Output

Pen Lift Output: TTL low level ($\leq 0.8V$) during sweep period in I-V/C-V function

Recorder Scale Output: Upper right/lower left scale output for location adjustment of recorder

Key	V_A output	I/C output
U.R. (Upper Right)	Either maximum voltage value of START or STOP voltages.	Full scale value of (+) plus sign.
L.L. (Lower Left)	Either minimum voltage value of START or STOP voltages.	Full scale value of (-) minus sign. 0V (0pF) for C-V measurement.
ZERO	0V	0V

HP-IB Interface: IEEE 488-1975, ANSI. STANDARD MC 1.1

Interface Functions: SH? AH? T5 L4 SR? RL? DC? DT?

Remotely Controllable Functions: Measurement Function, Current Range, Lower Limit of Auto Mode, Integration Time, I Trig, Filter, Voltage Sweep Control, Current Limit, Voltage of V_A/V_B , Setting Times and Self Test.

Data Output: Measured Data (I, C and V_A),
Voltage Settings (V_A , V_B),
Setting Times,
Setting Value of C_{ox} and,
Front Panel Key Status.

Table 1-1. Specifications(Sheet 6 of 7).

OPTIONS

- Option 907: Front Handle Kit (5061-0090).
Option 908: Rack Flange Kit (5061-0078).
Option 909: Rack and Handle Kit (5061-0084).
Option 910: Extra Manual.

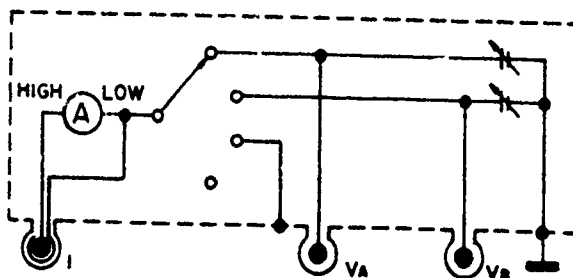
ACCESSORIES AVAILABLE

16053A: Test Leads (furnished with the 4140B)

One triaxial (male) - triaxial (male) cable, two BNC (male) - BNC (male) cables, and connection plate with female connectors (one triaxial and two BNC) are furnished. Each cable is 1 meter long. Useful for connecting user designed probe station/measurement fixture.

16054A: Connection Selectors

Selects connection of low lead for pA Meter section as in following figure. Used in conjunction with the 16053A.



16055A: Test Fixture for General Device Measurements (furnished with the 4140B)

For stable pA current measurements with electrostatic/light shielded hood. Alligator clips/T0-5 socket with connection plates for easy connection to actual devices.

16056A: Current Divider (10:1)

Extends 10^{-2} A range to 10^{-1} A (use only on 10^{-2} A range).

Table 1-1. Specifications(Sheet 7 of 7).

Other Accessories/Recommended Stock Parts:

Descriptions		HP Model/Part Number
HP-IB Cable	0.5m	10833D
	1m	10833A
	2m	10833B
	4m	10833C
Triaxial Connector Female		1250-0687
Male	CONNECTOR-RF	1250-1413
	ROD, BRASS	16053-24001
	ROD, BRASS	16053-24002
BNC Connector Female	CONNECTOR-RF	1250-0083
	NUT	2950-0001
	WASHER	2190-0016
	SOLDER LUG	0360-1190
Male		1250-0408
16055A Accessories		
Connection Plate with Alligator Clip		16055-65001
Connection Plate with TO-5 Socket (10pins)		16055-65002
Alligator Clips (10ea)		16055-65003
Connection Leads for TO-5 Socket (10ea)		16055-65004
TO-5 Socket (8pins)		1200-0238
TO-5 Socket (10pins)		1200-0239
TO-5 Socket (12pins)		1200-0240
Triaxial Cable (approx 1m)		16053-61002
BNC-BNC Cable (approx 1m)		16053-61003
Connection Plate for the 16053A		16053-61001

Hewlett Packard LF Impedance Analyzer, Model 4192A

The following is an excerpt of *Hewlett Packard LF Impedance Analyzer, Model 4192A*, Yokogawa-Hewlett-Packard, Ltd., Nov. 1981.



OPERATION AND SERVICE MANUAL

MODEL 4192A
LF IMPEDANCE ANALYZER

SERIAL NUMBERS

This manual applies directly to instruments with
serial numbers prefixed 2045J- and above.

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9-1, TAKAKURA-CHO, HACHIOJI-SHI, TOKYO, JAPAN

Manual Part No. 04192-90001
Microfiche Part No. 04192-90051

Printed : NOV. 1981

improves efficiency in production applications where repetitive measurements are made. This feature can also be used to measure the same parameter on one component under (five) different sets of test conditions. The standard memory of the 4192A preserves stored data even when the instrument is off.

1-10. The 4192A provides HP-IB interface capability for complete remote control of all front-panel control key settings and test parameter settings. This feature makes it possible to integrate the 4192A into a measurement system which reduces cost by improving DUT throughput, improving circuit design efficiency, and shortening the component development period. The 4192A is also equipped with X-Y recorder outputs and pen lift control. Clear and accurate copies of characteristics curves resulting from swept measurements can be obtained easily with this capability, without an external HP-IB controller.

1-11. The versatility and operability of the 4192A are maximized by the availability of versatile test fixtures. Because components and networks are not of uniform shape and size, the 4192A has several test fixtures that can be used to best meet different measurement requirements.

1-12. SPECIFICATIONS

1-13. Complete specifications of the Model 4192A LF Impedance Analyzer are given in Table 1-1. These specifications are the performance standards or limits against which the instrument is tested. The test procedures for the specifications are covered in Section IV, Performance Tests. Table 1-2 lists supplemental performance characteristics. Supplemental performance characteristics are not specifications but are typical characteristics included as additional information for the operator. When the 4192A LF Impedance Analyzer is shipped from the factory, it meets the specifications listed in Table 1-1.

1-14. SAFETY CONSIDERATIONS

1-15. The Model 4192A LF Impedance Analyzer has been designed to conform to the safety requirements of an IEC (International Electromechanical Committee) Safety Class I instrument and is shipped from the factory in a safe condition.

1-16. This operating and service manual contains information, cautions, and warnings which must be followed by the user to ensure safe operation and to maintain the instrument in a safe condition.

1-17. INSTRUMENTS COVERED BY MANUAL

1-18. Hewlett-Packard uses a two-section nine character serial number which is stamped on the serial number plate (Figure 1-2) attached to the instrument's rear-panel. The first four digits and the letter are the serial prefix and the last five digits are the suffix. The letter placed between the two sections identifies the country where the instrument was manufactured. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-19. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this new instrument may be accompanied by a yellow Manual Changes supplement or have a different manual part number. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-20. In addition to change information, the supplement may contain information for correcting errors (called Errata) in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with this manual's print date and part number, both of which appear on the manual's title page. Complimentary copies of the supplement are available from Hewlett-Packard. If the serial prefix or number of an instrument is lower than that on the title page of this manual, see Section VII, Manual Changes.

1-21. For information concerning a serial number prefix that is not listed on the title page or in the Manual Change supplement, contact the nearest Hewlett-Packard office.

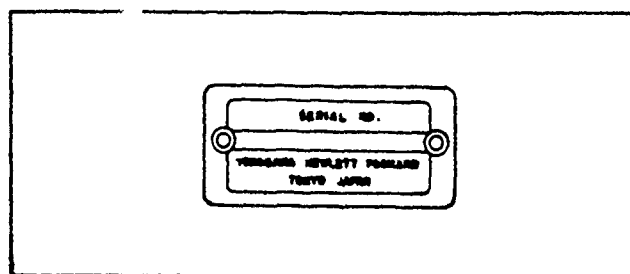


Figure 1-2. Serial Number Plate

Table 1-1. Specifications (Sheet 1 of 12)

COMMON SPECIFICATIONS

(Amplitude-Phase and Impedance Measurements)

INTERNAL SYNTHESIZER : Output from OSC OUTPUT (H_{CUR}) terminal

Frequency Range : 5.000Hz to 13.000000MHz

Frequency Resolution : 1mHz (5Hz to 10kHz), 10mHz (10kHz to 100kHz), 100mHz (100kHz to 1MHz), 1Hz (1MHz to 13MHz)

Frequency Accuracy : ± 50 ppm ($23^{\circ}\text{C} \pm 5^{\circ}\text{C}$)

OSC Level Range : Variable from 5mVrms to 1.1Vrms (when terminated by 50Ω in amplitude-phase measurements or UNKNOWN terminals are open in impedance measurements).

OSC Level Resolution : 1mV (5mV to 100mV), 5mV (100mV to 1.1V)

OSC Level Accuracy :

Measuring Frequency	OSC Level	
	$\leq 100\text{mV}$	$> 100\text{mV}$
5Hz ~ 1MHz	$(5 + 10/f) \pm 2\text{mV}$	$(5 + 10/f) \pm 10\text{mV}$
1MHz ~ 13MHz	$(4 + 1.5F) \pm 2\text{mV}$	$(4 + 1.5F) \pm 10\text{mV}$

f : measuring frequency (Hz). F : measuring frequency (MHz).

Output Resistance : 50Ω (amplitude/phase measurements), 100Ω (impedance measurements, $\geq 38\text{kHz}$), 100Ω to $10\text{k}\Omega$ (impedance measurements, $< 38\text{kHz}$, depends on measuring range).

Level Monitor (impedance measurement) Measures and displays the voltage across- or current through the device under test.

Frequency and Level Control : Set via the front-panel numeric keys or HP-IB: auto sweep (except for level) or manual sweep.

EXTERNAL SYNTHESIZER : Connected to the VCO INPUT connector on the rear-panel (HP3325A Synthesizer or equivalent is recommended).

Frequency Range : 40.000005MHz to 53MHz (measuring frequency is equal to the frequency of the external synthesizer minus 40MHz [5Hz to 13MHz]).

Required Signal Level : 0dBm to 3dBm

Note. Frequency of the 4192A internal synthesizer should be set to the frequency of the external synthesizer minus 40MHz, and the internal and external synthesizers should be phase-locked.

Table 1-1. Specifications (Sheet 2 of 12)

EXT REFERENCE INPUT CONNECTOR : Can be connected to a 1MHz/10MHz high stability reference signal (-1dBm to +5dBm) to improve the stability of the internal synthesizer.	
Input Resistance .	Approximately 50 Ω
MEASURING MODE :	
Spot Measurement .	At specific frequency (or dc bias*)
Swept Measurement .	Between START and STOP frequencies (or dc bias*). Sweep can be automatic or manual.
Sweep Mode :	Linear sweep mode (sweeps at specified step) and logarithmic sweep mode (20 measurement points per frequency decade).
X10 STEP :	Multiplies the specified frequency/dc bias* step by 10 in linear manual sweeps.
PAUSE Key .	Temporarily stops swept measurements.
SWEEP ABORT Key	Makes sweep cancellation.
* : DC bias sweeps can be made for impedance measurements only.	
RECORDER OUTPUT : DC outputs proportional to measured values of DISPLAY A, DISPLAY B, and measuring frequency or dc bias. PEN LIFT output and X-Y recorder scaling outputs are provided.	
Maximum Output :	$\pm 1V$
Output Voltage Accuracy :	$\pm (0.5\% \text{ of output voltage} + 20mV)$.
FIVE NONVOLATILE STORAGE REGISTERS . Memorize five complete instrument measurement configurations. Measurement configurations can be set from the front-panel from the HP-IB, or both.	
HP-IB INTERFACE : Data output and remote control via the HP-IB (based on IEEE-Std-488 and ANSI-MC1-1.	
Interface Capability .	SH1, AH1, T5, L4, SR1, RL1, DC1, DT1, E1.
Remote Control Function :	All front-panel functions except LINE ON/OFF switch and X10 STEP key.
Data Output :	Measured values of DISPLAY A, DISPLAY B, and measuring frequency or dc bias.
SELF TEST : Performs the 4192A basic operation checks and displays the test results when power is turned on or when the SELF TEST mode is set by the SELF TEST key or via HP-IB.	
TRIGGER : Internal, External, Hold/Manual, or HP-IB remote control.	

Table 1-1. Specifications (Sheet 3 of 12)

AMPLITUDE/PHASE MEASUREMENTS

PARAMETERS MEASURED : Measures DISPLAY A parameters and DISPLAY B parameters simultaneously in the parameter combination listed below. Deviation measurement (Δ) and percent deviation measurement ($\Delta\%$) can be performed for all measurement parameters.

DISPLAY A Function	DISPLAY B Function
B - A (dB) : Amplitude ratio	Group delay (s)
	θ (deg/rad) : Phase Difference
A (dBm/dBV) : Absolute amplitude of Reference Input	
B (dBm/dBV) : Absolute amplitude of Test Input	

REFERENCE AMPLITUDE : 0dBv = 1 Vrms. 0dBm = 1 mV (into 50 Ω)

OSC OUTPUT CONNECTOR OUTPUT IMPEDANCE : 50 Ω + 5% - 8% (at 50 Hz to 5 MHz), 50 Ω \pm 10% (at 5 Hz to 13 MHz).

CHANNEL A AND B :

Input Impedance : 1 M Ω \pm 2%, shunt capacitance 25 pF \pm 5 pF

Maximum Input Voltage : 2 Vrms/ \pm 35 V DC Max.

DISPLAY RANGE AND RESOLUTION : In NORMAL or AVERAGE measurement mode (Measuring resolution decreases one digit in HIGH SPEED measurement mode.

B - A : 0 to \pm 100 dB, 0.001 dB ($<$ 20 dB), 0.01 dB (\geq 20 dB) resolution

θ : 0 to \pm 180 $^\circ$ (0 to $\pm \pi$ radian), 0.01 $^\circ$ resolution

Group Delay (τ_g) : 0.1 ns to 19.999 s, 0.1 ns maximum resolution

A, B : +0.8 dBV to -100 dBV, +13.8 dBm to -87 dBm, 0.001 dB ($>$ -20 dB), 0.01 dB (\leq -20 dB) resolution

Table 1-1. Specifications (Sheet 4 of 12)

MEASURING ACCURACY Specified at measuring terminals when the following conditions are satisfied:

- (1) Warmup Time : > 30 minutes
- (2) Ambient Temperature : $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$ (error limits double for 0°C to 55°C temperature range).
- (3) Measuring Speed : NORMAL or AVERAGE mode.

Note: Additional errors due to the power splitter, feedthrough termination, etc., are to be added to specifications given here.

The measurement accuracy of each parameter is given below. The accuracy depends on input absolute level of each channel and the measuring frequency.

B-A and θ Measurements Accuracies : Accuracies are the sum of each channel accuracy given in the table below. For example, when the frequency is 1 kHz, A channel is -15 dBV and B channel is -25 dBV; the uncertainty contributed by each channel to the B-A error is 0.01 dB/0.05° and 0.05 dB/0.15°, respectively. Therefore, the final accuracy of 0.06 dB/0.2° is given by the accuracy of both channels.

Group Delay Measurements Accuracy : Accuracy is derived from the following equation (phase accuracy $\Delta\theta_A$ and $\Delta\theta_B$ are read from the table below):

$$\text{group delay accuracy} = \frac{\Delta\theta_A + \Delta\theta_B}{720 \times \Delta F} \text{ (s)}$$

where. $\Delta\theta_A$: Channel A phase accuracy (degree)

$\Delta\theta_B$: Channel B phase accuracy (degree)

ΔF : Step Frequency (Hz)

+0.8				
-10	$(0.008+0.2/f)\text{dB}$ $(0.04+1/f)^{\circ}$	0.01dB 0.05°	0.045dB 0.08°	$(0.025+0.02F)\text{dB}$ 0.08F°
-20	$(0.047+0.2/f)\text{dB}$ $(0.13+2/f)^{\circ}$	0.05dB 0.15°	0.08dB 0.25	$(0.04+0.04F)\text{dB}$ $(0.05+0.2F)^{\circ}$
-30	$(0.05+1/f)\text{dB}$ $(0.14+6/f)^{\circ}$	0.06dB 0.2°	0.12dB 0.3°	$(0.06+0.06F)\text{dB}$ $(0.05+0.25F)^{\circ}$
-40	$(0.05+3/f)\text{dB}$ $(0.15+15/f)^{\circ}$	0.08dB 0.3°	0.14dB 0.6°	$(0.07+0.07F)\text{dB}$ $(0.3+0.3F)^{\circ}$
-50	$(0.1+10/f)\text{dB}$ $(1+50/f)^{\circ}$	0.2dB 1.5°		$(0.1+0.1F)\text{dB}$ $(1+0.5F)^{\circ}$
-60	$(0.45+25/f)\text{dB}$ $(4+100/f)^{\circ}$	0.7dB 5°		$(0.4+0.3F)\text{dB}$ $(4+F)^{\circ}$
-70	$(1.5+50/f)\text{dB}$ $(12+300/f)^{\circ}$	2dB 15°		$(1+F)\text{dB}$ $(13+2F)^{\circ}$
-80				
-90	Unspecified			
-100				
	5	100	10k	1M
	13M			
	Measuring Frequency (Hz)			

f : measuring frequency (Hz)

F : measuring frequency (MHz)

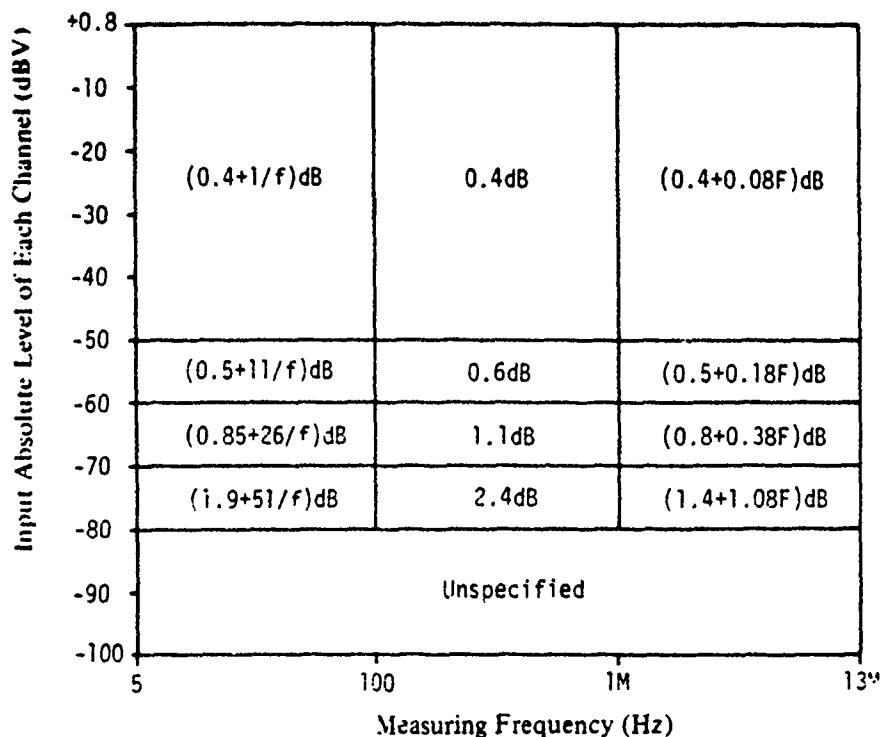
Equations in table represent:

A, B accuracy

θ accuracy

Table 1-1. Specifications (Sheet 5 of 12)

Absolute Amplitude (A, B) Accuracy : Accuracy is given in the table below.



f : measuring frequency (Hz)





F : measuring frequency (MHz)

Table 1-1. Specifications (Sheet 6 of 12)

IMPEDANCE MEASUREMENTS

PARAMETERS MEASURED : Measures DISPLAY A parameters and DISPLAY B parameters simultaneously in the parameter combinations listed below. Deviation measurement (Δ) and percent deviation measurement ($\Delta\%$) can be performed for all measurement parameters.

DISPLAY A Function	DISPLAY B Function
$ Z $: Absolute Value of Impedance	θ (deg/rad) : Phase Angle
$ Y $: Absolute Value of Admittance	
R : Resistance	X : Reactance
G : Conductance	B : Susceptance
L : Inductance	Q : Quality Factor
C : Capacitance	D : Dissipation Factor
	R : Resistance
	G : Conductance

EQUIVALENT CIRCUIT MODE : Auto,  (Series), and  (Parallel). $|Z|$, R, and X are measured in  mode; and $|Y|$, G, and B in  mode.

DISPLAY Maximum $4\frac{1}{2}$ digits in NORMAL or AVERAGE measurement mode, maximum 3 $\frac{1}{2}$ digits in HIGH SPEED measurement mode. Number of display digits depends on OSC level, measuring range, and measuring frequency.

RANGING : AUTO or MANUAL for impedance ($|Z|$) admittance ($|Y|$) measured value.

MEASUREMENT TERMINAL : 4-terminal pair configuration

AUTOMATIC ZERO ADJUSTMENT : Residual impedance ($R + jX$) and stray admittance ($G + jB$) of the test fixture are measured at a frequency selected by the operator. These values are then stored and used as offset data for subsequent measurements. The stored offset values are converted and applied to other measurement frequencies (refer to paragraph 3-79).

Table 1-1. Specifications (Sheet 7 of 12)

MEASURING RANGE AND RESOLUTION : Accuracy is specified at UNKNOWN terminals under the following conditions:

- (1) Warmup Time : ≥ 30 minutes
- (2) In Floating Measurements : (see Table 1-2 for specifics on low-grounded measurements)
- (3) Measuring Frequency : At the frequency of the zero offset adjustment
- (4) Ambient Temperature : $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$ (error limits double for temperature range of 0°C to 55°C)
- (5) CABLE LENGTH : At 0 position
- (6) Measuring Speed : NORMAL or AVERAGE mode
- (7) In the tables, area : Accuracy is not guaranteed.
 area : Accuracy cannot be specified.

$$B = 1 + \frac{0.02}{\gamma} : \text{use the left graph (below)}$$

$$C = \frac{1}{\gamma} : \text{use the right graph (below)}$$

where γ : OSC LEVEL (V)

f : Measuring frequency (Hz)

F : Measuring frequency (MHz)

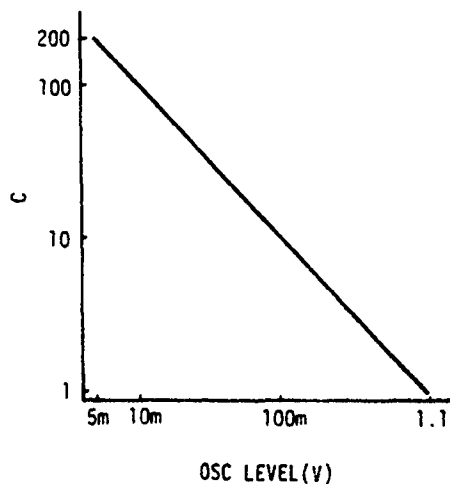
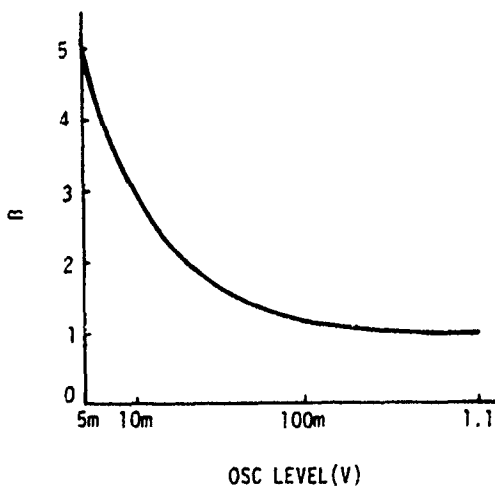


Table 1-1. Specifications (Sheet 8 of 12)

|Z| - θ and R-X Measurements :**Measuring Range :**

Parameter	Measuring Range	Maximum Resolution
Z · R · X	0.0001 Ω to 12.999 M Ω	100 $\mu\Omega$
θ	-180.00° to +180.00°	0.01°

Measurement Accuracy : Refer to the table below (specified by ZY RANGE). However, R and X accuracy depends on the value of D as follows:

	D < 1	1 ≤ D < 10	10 ≤ D
R	Accuracy of R is equal to the accuracy of X, in number of counts, as calculated from the table below.	Two times % error given in the table below.	Table below
X	Table below.	Accuracy of X is equal to the accuracy of R, in number of counts, as calculated from the table below.	

Z Range (Ω)	5	400	1M	2M	13M
	$\left[0.12 + \frac{A}{B} + \frac{5}{2} \left(1 + \frac{2.4A}{C}\right)\right] \cdot 1$ $\left[0.05 + \frac{0.1A}{B} + \frac{3}{2} \left(1 + \frac{0.2A}{C}\right)\right] \cdot 1$	$0.2 + \frac{A}{B} \cdot 1$ $0.1 + \frac{0.5A}{B} \cdot 1$	$0.2 + \frac{A}{B} \cdot 1$ $0.1 + \frac{0.5A}{B} \cdot 1$		
	$\left[0.1 + \frac{0.2A}{B} + \frac{5}{2} \left(1 + \frac{0.2A}{C}\right) + \frac{10A}{C}\right] \cdot 1$ $\left[0.05 + \frac{0.1A}{B} + \frac{3}{2} \left(1 + \frac{0.2A}{C}\right) + \frac{5A}{C}\right] \cdot 1$		$0.2 + \frac{0.2A}{B} \cdot 1$ $(0.05 + \frac{0.1A}{B}) \cdot 1$	$0.2 + \frac{0.2A}{B} \cdot 1$ $0.1 + \frac{0.1A}{B} \cdot 1$	
	$\left[0.1 + \frac{0.2A}{B} + \frac{5}{2} \left(1 + \frac{0.2A}{C}\right) + \frac{10A}{C}\right] \cdot 1$ $\left[0.05 + \frac{0.1A}{B} + \frac{3}{2} \left(1 + \frac{0.2A}{C}\right) + \frac{5A}{C}\right] \cdot 1$		$0.2 + \frac{0.2A}{B} \cdot 1$ $(0.05 + \frac{0.1A}{B}) \cdot 1$	$0.2 + \frac{0.2A}{B} \cdot 1$ $0.1 + \frac{0.1A}{B} \cdot 1$	
	$\left[0.18 + \frac{5}{2} \left(1 + \frac{0.04}{C} \left(1 + \frac{2.2}{A}\right)\right)\right] \cdot 3$ $\left[0.05 + \frac{0.01}{A} \cdot B + \frac{3}{2} \left(1 + \frac{0.04}{C} \left(1 + \frac{2.2}{A}\right)\right)\right] \cdot 1$	$0.18 \cdot 3$ $0.05 + \frac{0.01}{A} \cdot B \cdot 1$	$0.1 + \frac{0.01}{A} \cdot B \cdot 1$ $0.05 + \frac{0.01}{A} \cdot B \cdot 1$	$0.1 + \frac{0.01}{A} \cdot B \cdot 1$ $0.05 + \frac{0.01}{A} \cdot B \cdot 1$	
	$\left[0.28 + \frac{5}{2} \left(1 + \frac{0.04}{C} \left(1 + \frac{2.2}{A}\right)\right)\right] \cdot 5$ $\left[0.1 + \frac{0.02}{A} \cdot B + \frac{3}{2} \left(1 + \frac{0.04}{C} \left(1 + \frac{2.2}{A}\right)\right)\right] \cdot 1$	$0.28 \cdot 5$ $(0.1 + \frac{0.02}{A} \cdot B) \cdot 1$	$0.1 + \frac{0.02}{A} \cdot B \cdot 1$ $(0.1 + \frac{0.02}{A} \cdot B) \cdot 1$	$0.1 + \frac{0.02}{A} \cdot B \cdot 1$ $(0.1 + \frac{0.02}{A} \cdot B) \cdot 1$	
	$\left[0.58 + \frac{5}{2} \left(1 + \frac{0.04}{C} \left(1 + \frac{2.2}{A}\right)\right)\right] \cdot 5$ $\left[(0.3 + \frac{0.1}{A} \cdot B) + \frac{3}{2} \left(1 + \frac{0.04}{C} \left(1 + \frac{2.2}{A}\right)\right)\right] \cdot 1$	$0.58 \cdot 5$ $0.3 + \frac{0.1}{A} \cdot B \cdot 1$			

(1) $A = \frac{\text{Displayed } |Z|, R \text{ or } X (\Omega)}{|Z| \text{ Range full scale } (\Omega)}$ in the table.

(2) Equations in table represent :

|Z|, R, X accuracy [± (% of reading + number of counts)]
 θ accuracy [± (absolute value)]

Table 1-1. Specifications (Sheet 9 of 12)

$|Y| - \theta$ and G-B Measurements :

Measuring Range :

Parameter	Measuring Range	Maximum Resolution
$ Y , G, B$	$0.001 \mu S \sim 129.99 S$	$1 nS$
θ	$-180.00^\circ \sim +180.00^\circ$	0.01°

Measurement Accuracy : Refer to the table below (specified by ZY RANGE). However, G and B accuracy depends on the value of D as follows:

	$D \leq 0.1$	$0.1 < D \leq 1$	$1 < D$
G	Accuracy of G is equal to the accuracy of B, in number of counts, as calculated from the table below.		Table below
B	Table below	Two times % error given in the table below.	Accuracy of B is equal to the accuracy of G, in number of counts, as calculated from the table below.

$ Y $ Range (S)	5	100	$1m$	$10m$	$100m$	1	10
	$\{0.25 + \frac{5}{2} \{1 + \frac{0.24C}{A}\}\} \cdot 3$ $\{0.1 + \frac{0.05}{A} B + \frac{5}{2} \{1 + \frac{0.24C}{A}\}\} \cdot 3$	$0.25 + 3$ $0.1 + \frac{0.05}{A} B$	$0.2F B + 3$ $0.12F + \frac{0.05}{A} B$	$0.2F B + 3$ $0.12F + \frac{0.05}{A} B$	$0.15F B + 3$ $0.09F + \frac{0.01}{A} B$	$\{0.1 + 0.02F + 0.024F^2\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$
	$\{0.1B + \frac{5}{2} \{1 + 0.03 \{1 + \frac{1}{A} C\}\} \} \cdot 3$ $\{0.05 + \frac{0.01}{A} B + \frac{5}{2} \{1 + 0.03 \{1 + \frac{1}{A} C\}\} \} \cdot 3$	$0.1B + 3$ $0.05 + \frac{0.01}{A} B$	$0.15F B + 3$ $0.09F + \frac{0.01}{A} B$	$\{0.1 + 0.02F + 0.024F^2\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$
	$\{0.1B + \frac{5}{2} \{1 + 0.02 \{1 + \frac{1}{A} C\}\} \} \cdot 3$ $\{0.05 + \frac{0.01}{A} B + \frac{5}{2} \{1 + 0.02 \{1 + \frac{1}{A} C\}\} \} \cdot 3$	$0.1B + 3$ $0.05 + \frac{0.01}{A} B$	$0.15F B + 3$ $0.09F + \frac{0.01}{A} B$	$\{0.1 + 0.02F + 0.024F^2\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$
	$\{0.1B + \frac{5}{2} \{1 + 0.04 \{1 + \frac{1}{A} C\}\} \} \cdot 3$ $\{0.05 + \frac{0.01}{A} B + \frac{5}{2} \{1 + 0.04 \{1 + \frac{1}{A} C\}\} \} \cdot 3$	$0.1B + 3$ $0.05 + \frac{0.01}{A} B$	$0.15F B + 3$ $0.09F + \frac{0.01}{A} B$	$\{0.1 + 0.02F + 0.024F^2\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$
	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$
	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$
	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$	$\{0.1 + 0.2A\} B + 3$ $\{0.35 + \frac{0.01}{A}\} \cdot 0.01F + 0.014F^2 B$

(1) $A = \frac{\text{Displayed } |Y|, G \text{ or } B (S)}{|Y| \text{ Range full scale } (S)}$ in the table.

(2) Equations in table represent :

$|Y|, G, B$ accuracy $[\pm (\% \text{ of reading} + \text{number of counts})]$
 θ accuracy $[\pm (\text{absolute value})]$

Table 1-1. Specifications (Sheet 10 of 12)






L-Q, D, R, G Measurements : Refer to R/X or G/B measurements for R and G accuracy.

Measuring Range :

Parameter	Measuring Range	Maximum Resolution
L*	0.01 nH ~ 1.0000 kH	10 pH
D	0.0001 ~ 19.999	0.0001
Q	0.1 ~ 1999.9	0.1

* : Depends on ZY RANGE and measuring frequency (refer to paragraph 3-71).

Measuring Accuracy : Refer to the table below (specified by ZY RANGE).

Z Range (Ω)	1M	100k	10k	1k	100	10	1
	$\left\{ (1 + 2A)B + \frac{2}{3} \left(1 + \frac{1.44}{A} \right) \right\} \times 1$ $(0.01 + 0.002A)B + \frac{2.25}{A} \left(1 + \frac{1.44}{A} \right)$	$1 + 0.04/B + 1$ $0.01 + 0.002A/B$					
	$\left\{ 0.2 + 0.3A/B + \frac{5}{3} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right) \right\} \times 1$ $0.002 + 0.003A/B + \frac{2.25}{A} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$
	$\left\{ 0.2 + 0.3A/B + \frac{5}{3} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right) \right\} \times 1$ $0.002 + 0.003A/B + \frac{2.25}{A} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$
	$\left\{ 0.2 + 0.3A/B + \frac{5}{3} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right) \right\} \times 1$ $0.002 + 0.003A/B + \frac{2.25}{A} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$
	$\left\{ 0.2 + 0.3A/B + \frac{5}{3} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right) \right\} \times 1$ $0.002 + 0.003A/B + \frac{2.25}{A} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$
	$\left\{ 0.2 + 0.3A/B + \frac{5}{3} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right) \right\} \times 1$ $0.002 + 0.003A/B + \frac{2.25}{A} \left(1 + \frac{1.44}{A} \right) + 0.03 \left(1 + \frac{1.44}{A} \right)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$	$0.02F + 0.003A/B + 1$ $(0.0002F + 0.003A/B)$

$$(1) A = \frac{2\pi \times \text{Measuring frequency (Hz)} \times \text{Displayed L (H)}}{\text{Z: Range full scale } (\Omega)} \text{ in the table.}$$

(2) Equations in table represent (at $D \leq 0.1$) :

L accuracy $[\pm (\% \text{ of reading} + \text{number of counts})]$
 D accuracy $[\pm (\text{absolute value})]$

(3) If $0.1 < D \leq 1$, double the % error for all values of L.(4) If $D > 0.1$, multiply error of D by $(1 + D)^2$.

Table 1-1. Specifications (Sheet 11 of 12)

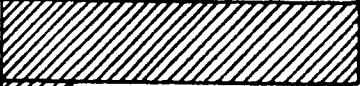

C-Q, D, R, G Measurements: Refer to R/X or G/B measurements for R and G accuracy.

Measuring Range:

Parameter	Measurement Range	Maximum Resolution
C*	0.0001nF ~ 100.00mF	0.1pF
D	0.0001 ~ 19.999	0.0001
Q	0.1 ~ 1999.9	0.1

* : Depends on ZY RANGE and measuring frequency (refer to paragraph 3-71).

Measurement Accuracy: Refer to the table below (specified by ZY RANGE).

Y Range (S)	10L	$\left\{0.2B + \frac{5}{F} \left(1 + \frac{0.24C}{A}\right)\right\} \pm 3$ $\left(0.002 + \frac{0.001}{A}\right)B + \frac{0.05}{F} \left(1 + \frac{0.24C}{A}\right)$	$0.2B \pm 3$ $\left(0.002 + \frac{0.001}{A}\right)B$	$0.2F B \pm 3$ $\left(0.002F + \frac{0.001}{A}\right)B$
	100L	$\left\{0.1B + \frac{5}{F} \left(1 + 0.03 \left(1 + \frac{1}{A}\right)C\right)\right\} \pm 3$ $\left(0.0009 + \frac{0.0002}{A}\right)B + \frac{0.05}{F} \left(1 + 0.03 \left(1 + \frac{1}{A}\right)C\right)$	$0.1B \pm 3$ $\left(0.0009 + \frac{0.0002}{A}\right)B$	$0.2F B \pm 3$ $\left(0.002F + \frac{0.0002}{A}\right)B$
	1m	$\left\{0.1B + \frac{5}{F} \left\{1 + 0.02 \left(1 + \frac{1}{A}\right)C\right\}\right\} \pm 3$ $\left(0.0009 + \frac{0.0002}{A}\right)B + \frac{0.05}{F} \left\{1 + 0.04 \left(1 + \frac{0.6}{A}\right)C\right\}$		$0.15F B \pm 3$ $\left(0.0015F + \frac{0.0002}{A}\right)B$
	10m	$\left\{0.1B + \frac{5}{F} \left\{1 + 0.04 \left(1 + \frac{0.6}{A}\right)C\right\}\right\} \pm 3$ $\left(0.0009 + \frac{0.0002}{A}\right)B + \frac{0.05}{F} \left\{1 + 0.04 \left(1 + 2A\right)C\right\}$		$0.1 + 0.02F + 0.024F^2 B \pm 3$ $0.0009 + \frac{0.0002}{A} + 0.0002F + 0.0003F^2 B$
	100m	$\left\{0.1 + 0.2A\right\}B + \frac{5}{F} \left\{1 + 0.04 \left(1 + 2A\right)C\right\} \pm 1$ $\left(0.0009 + \frac{0.0002}{A}\right)B + \frac{0.05}{F} \left\{1 + 0.04 \left(1 + 2A\right)C\right\}$	$\left\{0.1 + 0.2A\right\}B \pm 1$ $\left(0.0009 + \frac{0.0002}{A}\right)B$	$\left\{0.1 + 0.2A + 0.32F + 0.024F^2\right\}B \pm 1$ $\left(0.0009 + \frac{0.0002}{A} + 0.0002F + 0.0003F^2\right)B$
	1	$\left\{0.2 + 0.5A\right\}B + \frac{5}{F} \left\{1 + 0.04 \left(1 + 20A\right)C\right\} \pm 1$ $0.002 + 0.004A B + \frac{0.05}{F} \left\{1 + 0.04 \left(1 + 20A\right)C\right\}$	$\left\{0.2 + 0.5A\right\}B \pm 1$ $\left(0.002 + 0.004A\right)B$	
10		$\left\{0.5 + 2A\right\}B \pm 1$ $\left(0.005 + 0.02A\right)B$		

5

$$(1) A = \frac{2\pi \times \text{Measuring frequency (Hz)} \times \text{Displayed C (F)}}{|Y| \text{ Range full scale}}$$

(2) Equations in table represent (at $D \leq 0.1$) :

C accuracy [\pm (% of reading + number of counts)]
D accuracy [\pm (absolute value)]

(3) If $0.1 < D \leq 1$, double the % error for all values of C.

(4) If $D > 0.1$, multiply error of D by $(1 + D)^2$.

Table 1-1. Specifications (Sheet 12 of 12)

DC BIAS .	Valid for impedance measurements only.
Voltage Range .	-35 V to +35 V, 10 mV steps
Setting Accuracy (at 23°C ± 5°C) :	± (0.5% of setting + 5 mV)
Output Resistance :	110 Ω to 11 kΩ ± 10% (depends on measuring range)
Maximum Output Current :	Varies with measuring frequency and range.
Floating measurements	- 20 mA max.
Low-grounded measurements	- 5 mA max.
Control :	Front-panel numeric keys or HP-IB remote control
GENERAL	
OPERATING TEMPERATURE :	0°C to 55°C
RELATIVE HUMIDITY :	≤ 95% at 40°C
POWER :	100, 120, 220 V ± 10%, 240 V + 5 V - 10%, 48 Hz to 66 Hz, power consumption 100 VA maximum.
DIMENSIONS :	425.5 mm (W) × 230 mm (H) × 574 mm (D)
WEIGHT :	Approximately 19 kg
FURNISHED ACCESSORIES AND PARTS :	16047A Test Fixture, 11048C 50 Ω Feedthrough Termination (2 ea.), Splitter (HP Part No.: 11652-60009, Nominal 50 Ω), Power Cord (HP Part No.: 8120-1378).
OPTIONS	
OPTION 907 :	Front Handle Kit (HP Part No.: 5061-0091)
OPTION 908 :	Rack Flange Kit (HP Part No.: 5061-0079)
OPTION 909 :	Rack and Handle Kit (HP Part No.: 5061-0085)
OPTION 910 :	Extra Manual

Table 1-2. General Information (Sheet 1 of 2)

GENERAL INFORMATION

(The following information is reference data and not guaranteed specifications.)

TYPICAL MEASUREMENT ACCURACY :

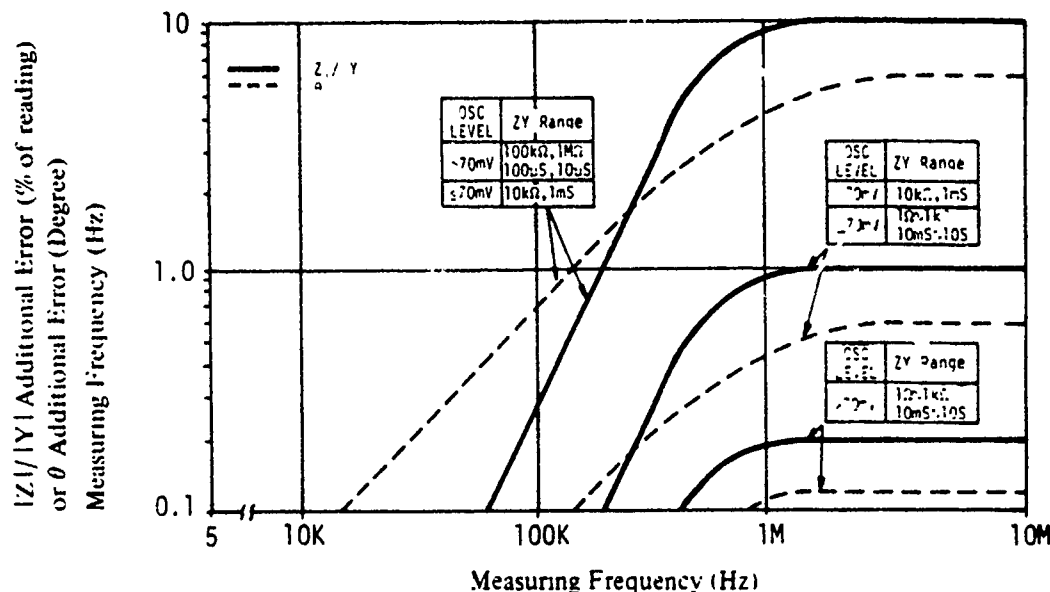
Impedance Measurement (Floating) :

Accuracy when CABLE LENGTH is 1 m : 2.5 times percent error for frequencies above 1 MHz.

L : C accuracy for $D > 1$: $(1 + D^2)$ times accuracy specifications

Low Grounded Impedance Measurement Accuracy :

To obtain low grounded measurement accuracy, add the accuracy for floating impedance measurements, given in the preceding tables, to the additional error given in the figure below. Compensation for residual impedance ($\leq 9\text{pF}$ at $\leq 600\text{kHz}$ or approximately $20\text{k}\Omega$ at $\geq 600\text{kHz}$) must also be made using the 4192A's zero offset adjustment function.



MEASURING SPEED :

Refer to the figure below (at fixed measuring frequency, measurement range and OSC level for impedance measurement). Specific information is provided in paragraph 3-55 for amplitude/phase measurements and in paragraph 3-89 for impedance measurements. Speed in AVERAGE mode is approximately 7 times that for NORMAL mode.

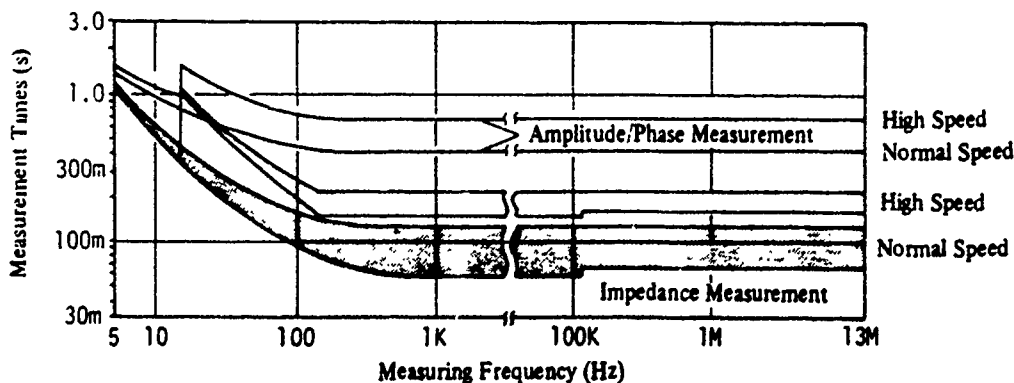


Table 1-2. General Information (Sheet 2 of 2)

FREQUENCY SWITCHING TIME : Approximately 50ms to 65ms

ZY RANGE SWITCHING TIME : Approximately 35ms to 50ms per range (at $> 400\text{ Hz}$)

OSC LEVEL SWITCHING TIME : Approximately 65ms

DC BIAS VOLTAGE SETTling TIME : Approximately $(0.4 \times \Delta V + 10)$ ms where ΔV is the voltage change (V).

LEVEL MONITOR RANGE AND ACCURACY : At $23^\circ\text{C} \pm 5^\circ\text{C}$

	Range	Accuracy (% of reading + count)
Voltage	5mV ~ 1.1V	$\leq 100\text{ Hz} : (4 + 10/f) \% + 1$
Current	1 μA ~ 11mA	100Hz to 1MHz : 4% + 1
		$\geq 1\text{ MHz} : (4 + 0.8F) \% + 1$
where f : measuring frequency (Hz). F . measuring frequency (MHz).		

TIME REQUIRED FOR LEVEL MONITOR : Approximately 120ms

1MHz REFERENCE OUTPUT : Square wave, $\geq 1.6\text{ Vp-p}$

Output Resistance : Approximately 50Ω

1-22. OPTIONS

1-23. Options are modifications to the standard instrument that implement the user's special requirements for minor functional changes. The 4192A has four options as listed in Table 1-3.

Table 1-3. Available Options

Option Number	Description
907	Front Handle Kit.
908	Rack Flange Kit.
909	Rack Flange and Front Handle Kit.
910	Extra Manual

1-24. The following options provide the mechanical parts necessary for rack mounting and hand carrying:

Option 907: Front Handle Kit. Furnishes carrying handles for both ends of front-panel.

Option 908: Rack Flange Kit. Furnishes flanges for rack mounting for both ends of front-panel.

Option 909: Rack Flange and Front Handle Kit. Furnishes both front handles and rack flanges for instrument.

Installation procedures for these options are detailed in Section II.

1-25. Option 910 adds an extra copy of the Operation and Service Manual.

1-26. ACCESSORIES SUPPLIED

1-27. The HP Model 4192A LF Impedance Analyzer, along with its furnished accessories, is shown in Figure 1-1. The furnished accessories are also listed below.

16047A Test Fixture
11048C 50 Ω Feedthrough (2 ea.)
Power Splitter (HP Part No.: 11652-60009)
BNC Adapter (HP Part No.: 1250-0216)
11170A BNC Cable (2 ea.)
Power Cable (HP Part No.: 8120-1378)

1-28. ACCESSORIES AVAILABLE

1-29. For certain measurements and for convenience in connecting samples, ten types of accessories are available. Each accessory is designed to meet the various measurement requirements and types of DUT. All accessories were developed with careful consideration to accuracy, reliability, and ease of measurement. A brief description and photo of each available accessory is given in Table 1-4.

Tektronix 468 Digital Storage Oscilloscope

The following is an excerpt of *Tektronix Digital Storage Oscilloscope, Model 468*, Instruction Manual, Service Vol. 1, June 1982.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS
ARE FOR USE BY QUALIFIED PERSONNEL ONLY.
TO AVOID PERSONAL INJURY, DO NOT
PERFORM ANY SERVICING OTHER THAN THAT
CONTAINED IN OPERATING INSTRUCTIONS
UNLESS YOU ARE QUALIFIED TO DO SO.

**PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL.**

468 DIGITAL STORAGE OSCILLOSCOPE

**SERVICE
VOLUME I**

INSTRUCTION MANUAL

**Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077**

**070-3515-00
Product Group 40**

Serial Number _____

**First Printing AUG 1980
Revised JUN 1982**

SPECIFICATION

INTRODUCTION

The TEKTRONIX 468 Oscilloscope is a portable digital storage oscilloscope with a four-trace, dc-to-100 MHz, vertical deflection system. The 468 combines an easy-to-use storage function with cursor measurement of time and voltage. Measurement values are indicated on a four-digit, seven-segment LED display.

NON STORE MODE

In the NON STORE mode, the 468 operates as a conventional oscilloscope that can display CH 1, CH 2, ADD, and A TRIG VIEW (external trigger only) simultaneously. The vertical deflection system has calibrated deflection factors ranging from 5 mV to 5 V per division. The horizontal deflection system has calibrated A Sweep rates from 0.5 s to 0.02 μ s per division and is capable of operating in the following sweep modes: A, A intensified by B, A alternated with delayed B, and B delayed. The calibrated B Sweep rates are from 50 ms to 0.02 μ s per division.

The horizontal magnifier circuit feature increases each sweep rate by a factor of 10. This provides a maximum sweep rate of 2 ns per division when the TIME/DIV switch is in the 0.02 μ s per division position.

STORAGE MODE

The 468 digital storage circuitry has a 10 MHz Useful Storage Bandwidth for the acquisition of signals, and will display the acquired waveform with a bright, flicker-free trace. With the digital storage feature, low-frequency signal analysis and waveform measurements—previously difficult or impossible to make—are easily performed. A choice of two standard and one optional signal acquisition modes are available: NORM and ENVELOPE (standard) and AVG (optional). Two storage functions are available to hold a display indefinitely for measurement and comparison: SAVE Storage Mode (stops acquisition) and SAVE REF (holds a reference display and continues acquisition in the selected Storage Mode). Using the PRE TRIG or POST TRIG Storage Window, waveform data may be acquired prior to or after the trigger. Time and voltage measurements on the acquired waveform are easily made using the VOLTS and TIME Cursor Functions, and the measurement values are indicated on a four-digit, seven-segment light-emitting diode (LED) display.

Digital storage adds three TIME/DIV switch positions, increasing the storage time base to 5 s per division (a total sweep time of 50 s). The waveshape of signals acquired at these low frequencies would be impossible to view on a conventional oscilloscope. Digital storage circuitry, however, constantly refreshes an acquired waveform to produce a directly viewable display for ease of analysis and measurement. Three added VOLTS/DIV switch positions increase the digital storage vertical deflection sensitivity up to 0.5 mV per division. Small-amplitude signals are acquired at 5 mV per division and are amplified to produce the added sensitivity.

The digital storage signal acquisition modes are NORM and ENVELOPE Storage Modes and an optional AVG Storage Mode. Selecting NORM Storage Mode causes acquisition and display of a new waveform with each trigger. The display in this mode most resembles conventional oscilloscope displays, and waveforms acquired will react to the oscilloscope front-panel controls with each trigger.

When ENVELOPE Storage Mode is chosen, the maximum and minimum waveform values for a selected number of sweeps are acquired, and the resultant waveform envelope is displayed. This mode is useful for detecting noise and spurious or erratic signals.

Choosing the optional AVG Storage Mode allows waveforms to be acquired for a selected number of sweeps and causes the averaged value of the acquired signals to be displayed. In this mode, signal-to-noise ratio is improved in direct proportion to the square root of the number of sweeps acquired, and noise accompanying the signal is either averaged out or reduced to a small level. The signal acquired in the AVG Storage Mode is processed to increase the vertical resolution of the displayed signal. This feature is very useful for displaying small-amplitude signals acquired in the 0.5, 1, and 2 mV per division positions of the VOLTS/DIV switch.

Once the desired signal is obtained in storage, the signal acquisition may be halted and the display frozen by selecting the SAVE Storage Mode. The waveform will remain displayed indefinitely for analysis and measurement purposes. In the SAVE mode, the next six faster positions of the TIME/DIV switch (if available) horizontally expand the display (up to 100 times). Additionally, signals acquired at sweep rates of 1 μ s per division or faster may be reduced back to the 2 μ s per division acquisition rate.

The SAVE display may also be expanded vertically (up to 10 times) with the next three higher deflection sensitivity positions of the VOLTS/DIV switch (if available) for the channel used to obtain the SAVE display. Signals obtained in the NORM or ENVELOPE Storage Mode at VOLTS/DIV switch settings 0.5, 1 or 2 mV per division may be reduced back to the 5 mV per division deflection sensitivity if desired. The SAVE display of a waveform acquired in the AVG Storage Mode may be expanded, but it may not be reduced below the deflection sensitivity at which the signal was acquired.

When the SAVE REF push button is pressed in, the waveform being displayed at that time will be stored and held on the display while the digital storage continues to acquire data. The SAVE REF display is then available for comparison with signals obtained from other circuits, or it can be used as a before-and-after check on circuit operation when changes or adjustments are made to the circuit under test. A new reference waveform is obtained each time the button is released and then pressed in again. Displaying the reference signal reduces the number of vertical mode possibilities that the 468 is capable of displaying simultaneously.

The time window used to obtain a stored waveform may be set to acquire either approximately 8.75 horizontal divisions of waveform data occurring before the triggering signal (in PRE TRIG Storage Window) or the same amount of waveform data occurring after the triggering signal (in POST TRIG Storage Window). The PRE TRIG feature is useful for analyzing events that might cause an error to occur. If the oscilloscope is set to trigger on the error, data immediately prior to the error is stored for analysis. POST TRIG Storage Window most resembles conventional triggering; but while conventional oscilloscope triggering usually starts the sweep, POST TRIG Storage Window triggering does not occur until approximately 1.25 horizontal divisions of waveform data are acquired.

Voltage and time measurements are made directly on the displayed waveform. Pressing in the VOLTS Cursor Function push button causes two horizontal lines (VOLTS Cursors) to be presented on the display. Only one cursor at a time is positionable using the CURSOR control knob. The active cursor is displayed as a dashed line, while the fixed cursor is a solid line. Voltage difference (as represented by the cursor positions) is directly read on the seven-segment LED display, and the appropriate measurement scale factor is shown on the three dual-color (red and green) LED indica-

tors to the right of the seven-segment LED display. Time measurements are made using two bright, positionable dots that appear on the trace when the TIME Cursor Function button is pressed in. The TIME cursor dots are positioned to the desired measurement points, and the time difference between the dots is directly read on the LED display.

A COUPLED V/T measurement mode is made available by pressing in both the VOLTS and TIME Cursor Function push buttons. In this mode, the TIME dots attach to the VOLTS cursors, and the VOLTS cursors will never be displayed beyond the limits of the waveform. The COUPLED V/T mode is useful for slope, peak-to-peak amplitude, and time duration measurements. While the cursors are coupled, the LED readout will display the voltage difference between the cursors.

In instruments factory equipped or converted to firmware version 2.0 or higher, the COUPLED V/T mode is also useful for making absolute dc-voltage measurements with respect to ground.

AVAILABLE OPTIONS

Option 02 is the General Purpose Interface Bus (GPIB), used to transmit the waveform data stored in the display memory. The waveform data transmitted will conform to the Waveform Transmission Standard as specified in the Tektronix Interface Standard—General Purpose Interface Bus (GPIB), Codes and Formats.

Option 12 is the AVE Storage Mode. This option will acquire data for a selected number of sweeps (from 2 to 256 in a binary sequence) and display the average waveform accumulated.

NOTE

The AVE Storage Mode is part of the standard instrument above SN B032430.

Option 04 (EMC) provides additional reduction of electromagnetic interference.

Option 05 provides the instrument with front-panel selection of additional trigger-signal processing capabilities to facilitate observation and measurement of composite video and related television waveforms.

Option 11 enables the 468 to convert the digital data stored in memory into analog X and Y outputs for driving an X-Y Plotter.

SPECIFICATION TABLES

The following electrical characteristics (Table 1-1) are valid only if the instrument has been calibrated at an ambient temperature between $+20^{\circ}\text{C}$ and $+30^{\circ}\text{C}$, the instrument is operating at an ambient temperature between -15°C and $+55^{\circ}\text{C}$ (unless otherwise noted), and the instrument has had a warmup period of about 20 minutes.

Environmental characteristics are given in Table 1-2. The 468 meets the requirements of MIL-T-28800B, Class 3, Style D equipment. Physical characteristics are listed in Table 1-3, and option electrical characteristics are presented in Table 1-4.

Table 1-1
Electrical Characteristics

Characteristics	Performance Requirements	Supplemental Information
VERTICAL SYSTEM		
Deflection Factor (Nonstorage Mode) Range		5 mV per division to 5 V per division in a 1-2-5 sequence of 10 steps.
DC Accuracy	Graticule indication is within 3% of true input voltage up to ± 12 divisions, referenced to instrument ground, for all calibrated VOLTS/DIV switch settings.	Gain set with VOLTS/DIV switch set to 5 mV per division.
Uncalibrated (VAR) Range (Nonstorage Mode)	Continuously variable between settings of VOLTS/DIV switch. Extends deflection factor to at least 12.5 V per division.	
Low-Frequency Linearity		0.1 division or less compression or expansion of a 2-division signal at center screen with waveform positioned to upper and lower extremes of graticule area.
Frequency Response		5-division reference signal from a $25\text{-}\Omega$ source; centered vertically, with VAR VOLTS/DIV control in calibrated detent.
Bandwidth (Channel 1 and Channel 2 Nonstorage Mode) -15°C to $+40^{\circ}\text{C}$	Dc to at least 100 MHz.	
$+40^{\circ}\text{C}$ to $+55^{\circ}\text{C}$	Dc to at least 85 MHz. ^a	
AC Coupled Lower -3 dB Point 1X Probe	10 Hz or less.	
10X Probe	1 Hz or less.	

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
VERTICAL SYSTEM (cont)		
Step Response (Non-Storage Mode)		5-division reference signal, dc coupled at all deflection factors, from a 25- Ω source; vertically centered with VAR VOLTS/DIV control in calibrated detent.
Rise Time 0°C to +40°C	3.5 ns or less (calculated). ^a	Rise Time = $\frac{0.35}{BW \text{ (in MHz)}}$
Positive-Going Step (Excluding ADD Mode) Aberrations 0°C to +40°C		+4%, -4%, 4% p-p or less. +6%, -6%, 6% p-p or less (5 V setting only).
Position Effect 0°C to +40°C		Total aberrations less than +6%, -6%, 6% p-p; checked at 5 mV per division.
Negative-Going Step		Add 2% to all positive-going specifications; checked at 5 mV per division.
ADD Mode Operation		Add 5% to all aberration specifications; checked at 5 mV per division.
Common Mode Rejection Ratio (ADD Mode With Channel 2 Inverted)		At least 10:1 at 20 MHz for common mode signals of 6 divisions or less with GAIN adjusted for best CMRR at 50 kHz. (10:1 at 10 MHz for storage mode.)
Trace Shift as VAR VOLTS/DIV Control Is Rotated		1 division or less. Digital Storage scale-factor LED will indicate voltage measurements are in divisions in a storage mode with the VAR control out of calibrated detent.
INVERT Trace Shift		Less than 2 divisions when switching from non-inverted to inverted.
Input Gate Current +20°C to +30°C		0.5 nA or less (0.1 division or less trace shift when switching input coupling between DC and GND with VOLTS/DIV switch set to 5 mV per division).
-15°C to +55°C		4 nA or less (0.8 division or less trace shift when switching input coupling between DC and GND with VOLTS/DIV switch set to 5 mV per division).

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
VERTICAL SYSTEM (cont)		
Channel Isolation		At least 100:1 at 25 MHz (10 MHz in storage).
Vertical POSITION Range		At least +12 and -12 divisions from graticule center.
Chopped Mode Repetition Rate (Nonstorage Mode)	Approximately 500 kHz.	Within 20%.
Input R and C		
Resistance	1 M Ω , within 2%. ^a	
Capacitance	Approximately 20 pF. ^a	
R and C Product (+20°C to +30°C)		Aberrations 2% or less using a P6105 probe.
Maximum Input Voltage		
DC Coupled	250 V (dc + peak ac). ^a 500 V (p-p ac at 1 kHz or less). ^a	
AC Coupled	250 V (dc + peak ac). ^a 500 V (p-p ac at 1 kHz or less). ^a	
Cascaded Operation		CH 1 VERT OUT SIGNAL OUT coupled into CH 2 input; ac coupled, using 50- Ω , 42-inch RG-58 C/U cable, terminated in 50 Ω at the CH 2 input connector.
Bandwidth (Nonstorage)	Dc to at least 50 MHz.	
Cascaded Sensitivity	At least 1 mV per division; terminated in 50 Ω at the CH 2 input connector.	
DIGITAL STORAGE VERTICAL ACQUISITION		
Resolution		8 bits, 25 levels per division. 10:24 divisions dynamic range.
DC Accuracy	Scaled binary value of stored digital word is within 3% of true input voltage up to ± 12 divisions, referenced to instrument ground, for all calibrated VOLTS/DIV switch settings.	Gain set with VOLTS/DIV set to 5 mV per division.
Range		0.5 mV to 5 V per division in a 1-2-5 sequence of 13 steps.
Digital Sample Rate		10 Hz to 25 MHz as determined by the TIME/DIV switch setting.

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements		Supplemental Information
DIGITAL STORAGE VERTICAL ACQUISITION (cont)			
Digital Chop Rate			5 Hz to 12.5 MHz (1/2 of the non-chopped sample rate at all TIME/DIV switch settings).
Analog Step Response	3% or less acquired overshoot on a 5-division pulse with Display Response set to PULSE.		Checked on a saved waveform display using horizontal expansion (X10 MAG off).
Analog Bandwidth	Dc to 10 MHz, within ± 1 dB, measured in ENVELOPE Storage Mode with the TIME/DIV switch set to 1 ms.		At exactly 10 MHz input signal frequency, it is possible for aliasing to occur and produce an envelope with variable amplitude. If aliasing occurs, shift the test frequency slightly to obtain an envelope with flat amplitude.
Useful Storage Bandwidth			For SINE Display Response, useful storage bandwidth is limited to that frequency where there are 2.5 samples per input cycle period at the maximum sampling rate (max sampling rate is 25 MHz in Single Trace or ALT and 12.5 MHz in CHOP). Accuracy at useful storage bandwidth limit is measured with respect to a 6 division, 50 kHz reference sine wave.
NORM Storage Mode	Single Trace or Alt	CHOP	
SINE Display Response	Dc to 10 MHz, within +1, -3 dB, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μ s (X10 MAG off).	Dc to 5 MHz, within +0.5, -1.5 db, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μ s (X10 MAG off).	
PULSE Display Response	Dc to 3.5 MHz, within +0.5, -1.5 dB, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μ s (X10 MAG off).	Dc to 1.75 MHz, within +0.5, -1.5 db, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μ s (X10 MAG off).	
Useful Storage Rise Time			Useful storage rise time is defined as 1.6 times the minimum sampling interval (40 ns in Single Trace or ALT and 80 ns in CHOP).
NORM Storage Mode			
PULSE Display Response	64 ns.	128 ns.	

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
TRIGGERING		
Sensitivity		In EXT/10, multiply requirements by 10.
AC Coupled Signal	0.3 division internal or 50 mV external from 30 Hz to 10 MHz; increasing to 1.5 divisions internal or 150 mV external up to 100 MHz.	
LF REJ Coupled Signal	0.5 division internal or 100 mV external from 50 kHz to 10 MHz; increasing to 1.5 divisions internal or 300 mV external up to 100 MHz.	Attenuates signals below approximately 50 kHz.
HF REJ Coupled Signal	0.5 division internal or 100 mV external from 30 Hz to 50 kHz.	Attenuates signals above approximately 50 kHz.
DC Coupled Signal	0.3 division internal or 50 mV external from dc to 10 MHz; increasing to 1.5 divisions internal or 150 mV external up to 100 MHz.	
Trigger Jitter		
Nonstorage Mode	0.5 ns or less at 100 MHz at 2 ns per division (X10 MAG on).	
Storage Mode	± 1 sample period for data transmitted on the GPIB. See Jitter Correction Performance Requirement. ^a	Inherent ± 1 sample jitter between sample clock and asynchronous trigger is partially compensated for by the jitter correction circuitry.
External Trigger Inputs		
Maximum Input Voltage	250 V (dc + peak ac). ^a 250 V (p-p ac at 1 kHz or less). ^a	
Input Resistance	1 M Ω within 10%. ^a	
Input Capacitance		Approximately 20 pF, within 30%.
LEVEL Control Range		
EXT	At least + and -2 V, 4 V p-p.	
EXT/10	At least + and -20 V, 40 V p-p.	
A External Trigger View (Nonstorage Mode Only)		
Deflection Factor		Dc trigger coupling only; checked with a 1 kHz signal.
EXT	100 mV per division $\pm 5\%$.	
EXT/10	1 V per division $\pm 5\%$.	

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
TRIGGERING (cont)		
A External Trigger View (Nonstorage Mode Only) (cont)		
Rise Time	5 ns or less. ^a	BW Limit at full (button out).
Delay Difference	$\leq \pm 0.20$ division ($\leq \pm 400$ ps at 2 ns per division).	5-div signal with 5 ns rise time or less from a 25- Ω source; centered vertically with equal 50- Ω cable length from signal source to vertical channel and external trigger input connectors; terminated in 50- Ω at each input.
Centering of Triggering Point		Within 1 division of center screen.
Flatness and Aberrations		+10%, -10%, 10% p-p.
HORIZONTAL DEFLECTION SYSTEM		
Sweep Rate (Nonstorage Mode)		
Calibrated Range		
A Sweep		0.5 s/div to 0.02 μ s/div in 23 steps in a 1-2-5 sequence. X10 MAG extends maximum sweep rate to 2 ns/div.
B Sweep		50 ms/div to 0.02 μ s/div in 20 steps in a 1-2-5 sequence. X10 MAG extends maximum sweep rate to 2 ns/div.
Accuracy	Within the given percentages of the indicated value.	Accuracy specification applies over the full 10 div of the unmagnified sweep.
+20°C to +30°C	Unmagnified	In X10 MAG, at TIME/DIV switch setting of .02 μ s, .1 μ s, and .2 μ s, exclude the first and last 50 ns of the sweep; and at a TIME/DIV switch setting of .5 μ s, exclude the first 100 ns of the sweep.
	Within 2%	
-15°C to +55°C	Within 3% ^a	Within 4% ^a
Two-Division Linearity Check		$\pm 5\%$ over any two-division portion (or less) of the full 10 div. When in X10 MAG exclude first and last magnified div when checking 2 ns, 5 ns, and 10 ns/div rates.
Alternate Sweep Trace Separation (Nonstorage Mode Only)		$\geq \pm 4$ divisions.
Variable Range (A Only) (Nonstorage Mode)	Continuously variable between calibrated settings of the A TIME/DIV switch. Extends slowest A sweep rate to at least 1.25 s/div.	At least 2.5:1.

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements		Supplemental Information
HORIZONTAL DEFLECTION SYSTEM (cont)			
A Sweep Length (Nonstorage Mode)			10.5 to 11.5 divisions.
A Trigger HOLDOFF (Variable)			Increases A sweep holdoff time by at least a factor of 10 (Nonstorage Mode). Storage holdoff time is a function of microprocessor operation.
Magnifier Registration			Within 0.2 division from graticule center (X10 MAG on to X10 MAG off).
POSITION Range (Horizontal)			Start of sweep must position to right of graticule center. End of sweep must position to left of graticule center.
Differential Time Measurement Accuracy (Nonstorage Mode)	Measurements of 1 or more major dial divisions	Measurements of less than 1 major dial division	With the A TIME/DIV switch at 0.5 μ s per division, or 0.2 μ s per division, the differential time measurement accuracy limit is valid only for DELAY TIME POSITION dial settings between 1.50 and 8.50.
+15°C to +35°C	Within 1% of indicated value.	\pm 0.01 major dial division.	
-15°C to +55°C	Within 2.5% of indicated value. ^a	\pm 0.03 major dial division. ^a	
Delay Time Jitter (Nonstorage Mode)	One part or less in 50,000 (0.002% of 10 times the A TIME/DIV switch setting) when operating on an ac-power-source frequency above 50 Hz. One part or less in 20,000 (0.005% of A TIME/DIV switch setting) when operating on a 50-Hz or lower ac-power source frequency. ^a		
Calibrated Delay Time (VAR Control in Calibrated Detent)	Continuous from 0.2 μ s to at least 5 s after the delaying (A) sweep.		
X-Y Operation (Nonstorage Mode Only)			
X-Axis Deflection Factor	Same as vertical system, with X10 MAG off.		
Variable Range	Same as vertical system.		
X-Axis Bandwidth	Dc to at least 4 MHz.		10-division reference signal.
Input Resistance	Same as vertical system. ^a		
Input Capacitance	Same as vertical system. ^a		

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
HORIZONTAL DEFLECTION SYSTEM (cont)		
X-Y Operation (Nonstorage Mode Only) (cont)		
Maximum Usable Input Voltage	Same as vertical system. ^a	
Phase Difference Between X and Y Amplifiers		Within 3° from dc to 50 kHz.
Deflection Accuracy	Graticule indication is within 4% of true input voltage.	
DIGITAL STORAGE HORIZONTAL ACQUISITION		
Horizontal Resolution		
Single Waveform Acquisition		9 bit, 512 data points (50 data points per division across the graticule area).
Chopped Acquisition (NORM Storage Mode Only)		8 bit, 256 data points per division (25 data points per division across the graticule area).
Range		5 s per division to 20 ns per division in a 1-2-5 sequence. At TIME/DIV switch settings of 5 s to 2 μ s, waveform sampling rate is determined by the switch setting. From 1 μ s to 0.02 μ s per division, sampling rate is at the 2 μ s per division rate. Interpolation and analog gain are used to expand the signal to the correct horizontal scale.
Accuracy (Sample Period)		Sample clock is within 0.01% of selected sample period, ± 50 ps ADC aperture uncertainty. Crystal oscillator: 0°C to +70°C $V_{cc} = +5$ V ± 0.5 V.
Dynamic Range	10.24 divisions.	
STORAGE DISPLAY		
Vertical		
Resolution		1 part in 1024 (10 bit). Calibrated for 100 points per division.
Differential Accuracy	Graticule indication of voltage cursor difference is within 2% of LED readout value, measured over center six divisions.	

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
STORAGE DISPLAY (cont)		
Vertical (cont) POSITION Range		Any portion of a stored waveform vertically magnified X10 can be positioned to the top and to the bottom of the graticule area.
Position Registration NON STORE to NORM		Within ± 0.5 division at graticule center at VOLTS/DIV settings from 5 mV to 5 V per division.
NORM, ENVELOPE, or AVG to SAVE		Within ± 0.2 divisions at VOLTS/DIV settings from 5 mV to 5 V per division.
SAVE Mode Gain Range (Vertical)		Up to X10 as determined by the setting of the VOLTS/DIV switch.
ENVELOPE Fill		90% or more of a six division ENVELOPE display.
Rise Time		≤ 0.3 horizontal graticule division for a five-division step, with horizontal X10 MAG on. Checked with no samples on the rising edge of the waveform.
Aberrations		+6%, -6%, 6% p-p or less on a five-division step (fast rise) input.
Horizontal Resolution		1 part in 1024 (10 bit). Calibrated for 100 points per division.
Differential Accuracy	Graticule indication of time cursor difference is within 2% of LED readout value, measured over center eight divisions.	
SAVE Mode Gain Range (Horizontal)		Up to X100 as determined by the setting of the TIME/DIV switch.
Position Registration		Sweep start between NON STORE and Storage within ± 0.2 division at TIME/DIV switch setting of 1 ms.
Display Response (Selectable) SINE		Microprocessor performs an interpolation between data points that is optimized to produce the best response for input signals that have no frequency components above $F_s/2$, when F_s is the sampling rate.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
STORAGE DISPLAY (cont)		
Display Response (Selectable) (cont) SINE (cont)		For a 6-division, sinusoidal input, digitized at 2.5 samples per input cycle and expanded 10X with the TIME, DIV switch, SINE Display Response envelope distortion produces a maximum amplitude error at any peak which is less than 5% of the ideally reconstructed reference p-p amplitude, assuming no distortion in the acquired input signal.
PULSE		Microprocessor performs linear interpolation between data points to optimize the display response for fast-rise and fast-fall waveforms (rise and fall times faster than 3 times the sampling interval). For a 6-division, sinusoidal input at seven samples per input cycle period, PULSE Display Response envelope distortion produces a maximum amplitude error at any peak which is less than 5% of the ideally reconstructed reference p-p amplitude.
Jitter Correction		Reduces effect of sample clock-to-trigger jitter.
Gain		0.4 division, $\pm 10\%$, X10 MAG on.
Resolution		± 0.1 sample period for TIME/DIV switch settings of 20 μ s to 5 s per division, ± 3 ns for switch settings of 0.02 μ s to 10 μ s per division. NOTE <i>Due to inherent uncertainty involved in the jitter correction, the resolution will occasionally, at random intervals, exceed the limits given above.</i>
READOUT DISPLAY		
Display Type		Four-digit, seven-segment LED indicators.
VOLTS Readout		Displays calculated voltage difference between horizontal cursors in VOLTS measurement mode. Scale factor is determined by VOLTS/DIV switch setting.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
READOUT DISPLAY (cont)		
Display Type (cont)		
VOLTS Readout (cont)		
Resolution		1 part in 1024 (10 bit).
TIME Readout		Displays calculated time difference between cursor dots in TIME measurement mode. Scale factor determined by setting of the appropriate TIME/DIV switch (A or B).
Resolution		1 part in 1024 (10 bit).
<p>NOTE</p> <p>Scale-factor LED indicates measurement is in DIV in the VOLTS measurement mode when vertical UNCAL LED is illuminated, or when different deflection factors are used in a dual-channel mode.</p>		
CRT DISPLAY		
Display Area		8 X 10 cm.
Geometry		0.1 division or less of tilt or bowing.
Trace Rotation Range		Adequate to align trace with horizontal graticule lines. At least $\pm 3^\circ$.
Standard Phosphor		P31 (green).
Nominal Accelerating Potential		18.5 kV.
Electrode Voltages to Ground		
Heater Voltage Between CRT Pins 1 and 14		6.3 Vrms, ± 3 V; elevated to -2450 V.
Cathode (Pin 2)		-2450 V, $\pm 2\%$.
Grid No. 1 (Pin 3)		≈ -2455 V to -2555 V.
Focus (Pin 4)		≈ -1780 V to -2000 V.
Astigmatism (Pin 5)		0 V to $\approx +95$ V.
Isolation Shield (Pin 7)		+35 V, ± 5 V.
First Anode (Pin 8)		$\approx +55$ V.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
CRT DISPLAY (cont)		
Electrode Voltages to Ground (cont)		
Geometry (Pin 10)		0 to $\approx +95$ V.
Mesh (Pin 12)		≈ -150 V.
CALIBRATOR		
Output Voltage		
0°C to +40°C	0.3 V, within 1.0%	Within 0.5% at 25°C, $\pm 5^\circ$ C.
-15°C to +55°C		0.3 V, within 1.5%.
Repetition Rate	Approximately 1 kHz.	Within 25%.
Output Resistance		Approximately 10.3 Ω .
Output Current		
+20°C to +30°C	30 mA, within 2%. ^a	
-15°C to +55°C		30 mA, within 2.5%.
Z-AXIS INPUT		
Sensitivity	5 V p-p signal causes noticeable modulation at normal intensity.	Positive-going signal decreases intensity.
Usable Frequency Range	Dc to 50 MHz. ^a	
Input Resistance		25 k Ω , within 10%. Decreases to approximately 200 Ω at 2 MHz and above.
Maximum Input Voltage		25 V (dc + peak ac).
SIGNAL OUTPUTS		
CH 1 VERT SIGNAL OUT		
Output Voltage	At least 50 mV per division of displayed signal into 1 M Ω . At least 25 mV per division of displayed signal into 50 Ω .	
Output Resistance		Approximately 50 Ω .
Bandwidth	Dc to at least 50 MHz into 50 Ω .	
DC Level	Approximately 0 V.	Within 100 mV.

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
SIGNAL OUTPUTS (cont)		
A and B + GATES Output Voltage	Approximately 5.5 V, positive-going rectangular pulse.	Starts at 0 V, within 500 mV.
Output Resistance		Approximately 500 Ω .
POWER SOURCE		
AC-Source Voltage Ranges		
115 V		
(High)	108 V to 132 V. ^a	
(Low)	90 V to 110 V. ^a	
230 V		
(High)	216 V to 250 V. ^a	
(Low)	198 V to 242 V. ^a	
AC-Source Frequency	48 Hz to 440 Hz. ^a	
Power Consumption		
Typical	115 watts (140 VA). ^a	
Maximum	150 watts (190 VA). ^a	48 Hz, 110 Vac, low regulating range.

Characteristics	Supplemental Information				
INTERNAL POWER SUPPLIES					
Main Supply Accuracy (+20°C to +30° C)	Initial Setting	Any 500-Hour Period After First 200 Hours	Maximum p-p Ripple	Accuracy From -15°C to 55°C	
	-8 V	±0.9%	±1.7%	2 mV	Within 0.5% of 25°C value
	+5 V	±0.9%	±1.7%	2 mV	Within 0.5% of 25°C value
	+15 V	±0.9%	±1.7%	2 mV	Within 0.5% of 25°C value
	+55 V	±0.3%	±0.7%	4 mV	Within 0.5% of 25°C value
	-2450 V	±1.2%	±2.2%		
	+110 V	±3%		100 mV	

^aPerformance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Supplemental Information			
INTERNAL POWER SUPPLIES (cont)				
Digital Storage Power Supplies (Not Adjustable)				
Voltage	-6 V	--12 V	+5 V	+12 V
Tolerance	±4%	±5%	±4%	±5%
Maximum p-p Ripple			150 mV	

Table 1-2
Environmental Characteristics

Characteristics	Description
<p>NOTE All of the environmental tests performed meet the requirements of MIL-T-28800B, Class 3, Style D equipment.</p>	
Temperature	
Nonoperating (Storage)	-62°C to +85°C.
Operating	-15°C to +55°C.
Altitude	
Nonoperating (Storage)	To 50,000 ft.
Operating	To 15,000 ft.
Humidity (Operating and Nonoperating)	5 cycles (120 hrs) referenced to MIL-T-28800B, Par 3.9.2.2. Class 3, 95% to 97% relative humidity.
Vibration (Operating)	15 minutes along each of 3 major axes at a total displacement of 0.025 inch p-p (4 g's at 55 Hz), with frequency varied from 10 Hz to 55 Hz to 10 Hz in 1-minute sweeps. Hold 10 minutes at each major resonance, or if no major resonance present, hold 10 minutes at 55 Hz.
Shock (Operating and Nonoperating)	30 g's, half-sine, 11-ms duration, 3 shocks per axis in each direction, for a total of 18 shocks.
EMI	
Option 04 Only	Meets TEKTRONIX Standard 062-2866-00 with exception of RE-02 specification being relaxed by 20 dB.

Table 1-3
Physical Characteristics

Characteristics	Description
Weight	
With Panel Cover, Accessories, and Accessory Pouch	33 pounds (15 kg).
Without Panel Cover, Accessories, and Accessory Pouch	30 pounds (13.6 kg).
Domestic Shipping Weight	47 pounds (21.4 kg).
Height	
With Feet and Pouch	7.5 inches (19.0 cm).
Without Pouch	7.2 inches (18.3 cm).
Width	
With Handle	12.9 inches (32.8 cm).
Without Handle	11.5 inches (29.2 cm).
Depth	
Including Panel Cover	21.7 inches (55.1 cm).
Handle Extended	23.7 inches (60.2 cm).

Table 1-4
Option Electrical Characteristics

Characteristics	Performance Requirement	Supplemental Information
GENERAL PURPOSE INTERFACE BUS (GPIB) OPTION 02		
Interface Function ^a	SH1 Source Handshake. AH1 Acceptor Handshake. T1 Basic talker, talk only mode, serial poll. L0 No Listener. SR1 Service Request. RL0 No Remote/Local. PP0 No Parallel Poll. DC2 Device Clear. DT0 No Device Trigger. C0 No Controller.	
Waveform Data Transmitted ^a	Conforms to Tektronix Interface Standard, GPIB Codes and Formats (Rev. C).	When no waveform has been acquired, only the ID portion of the waveform message will be transmitted.
SIGNAL AVERAGING OPTION 12		
Averaging Range	Two to 256 waveforms in a 2-4-8 binary sequence. Number of sweeps to be averaged set with CURSOR/NO. OF SWEEPS control knob when NO. OF SWEEPS push button (on side panel) is pressed in.	Uncorrelated noise, signal-to-noise ratio is improved by the square root of the number of waveforms averaged.

^aPerformance requirement not checked in manual.

Tektronix 2465 Oscilloscope

The following is an excerpt of *Tektronix Oscilloscope, Model 2465*,
Instruction Manual, March 1984.



WARNING

THE FOLLOWING SERVICING INSTRUCTIONS
ARE FOR USE BY QUALIFIED PERSONNEL ONLY.
TO AVOID PERSONAL INJURY, DO NOT
PERFORM ANY SERVICING OTHER THAN THAT
CONTAINED IN OPERATING INSTRUCTIONS
UNLESS YOU ARE QUALIFIED TO DO SO.

**PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL.**

2465 OSCILLOSCOPE SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

SPECIFICATION

INTRODUCTION

The TEKTRONIX 2465 Oscilloscope is a portable 300-MHz instrument having a four-channel vertical deflection system. Channel 1 and Channel 2 provide calibrated deflection factors from 2 mV per division to 5 V per division. For each of these channels, input impedance is selectable between two values: either 1 M Ω in parallel with 15 pF, or 50 Ω internal termination. Input-signal coupling with 1-M Ω impedance can be selected as either AC or DC. Channel 3 and Channel 4 have deflection factors of either 0.1 V or 0.5 V per division. Each of these channels has an input impedance of 1 M Ω in parallel with 15 pF, with DC input-signal coupling. Trigger circuits enable stable triggering over the full bandwidth of the vertical system.

The horizontal deflection system provides calibrated sweep speeds from 1.5 s per division to 500 ps per division. Drive for the horizontal deflection system is obtained from a choice of A, B delayed, A alternated with B delayed sweeps, or CH 1 (for the X-Y display mode).

The 2465 incorporates alphanumeric crt readouts of the vertical and horizontal scale factors, the trigger levels, time-difference measurement values, voltage-difference measurement values, and certain auxiliary information.

The 2465 Oscilloscope is shipped with the following standard accessories:

- 2 Probe packages
- 1 Snap-lock accessories pouch
- 1 Zip-lock accessories pouch
- 1 Operators manual
- 1 Service manual
- 1 Operators pocket reference card
- 1 Fuse
- 1 Power cord (installed)
- 1 Blue plastic crt filter (installed)
- 1 Clear plastic crt filter
- 1 Front-panel cover

For part numbers and further information about both standard and optional accessories, refer to either "Options and Accessories" (Section 7) in the Operators manual or the Accessories information at the rear of this manual. Your Tektronix representative or local Tektronix Field Office can also provide accessories information and ordering assistance.

PERFORMANCE CONDITIONS



The following electrical characteristics (Table 1-1) are valid for the 2465 when it has been adjusted at an ambient temperature between +20°C and +30°C, has had a warm-up period of at least 20 minutes, and is operating at an ambient temperature between -15°C and +55°C (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1-2. The 2465 Oscilloscope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style C equipment, with the humidity and temperature requirements defined in paragraphs 3.9.2.2, 3.9.2.3, and 3.9.2.4.

Mechanical characteristics of the 2465 are listed in Table 1-3.

Table 1-1 (cont)

Characteristics	Performance Requirements	
VERTICAL DEFLECTION SYSTEM—CHANNEL 1 AND CHANNEL 2 (cont)		
Common-mode Rejection Ratio (CMRR)	At least 20:1 at 50 MHz for common-mode signals of eight divisions or less, with VAR VOLTS/DIV control adjusted for best CMRR at 50 kHz at any VOLTS/DIV switch setting from 5 mV to 5 V per division; at least 20:1 at 20 MHz for the 2-mV-per-division switch setting.	
Channel Isolation	100:1 or greater attenuation of the deselected channel at 100 MHz; 50:1 or greater attenuation at 300 MHz, for an eight-division input signal from 2 mV per division to 500 mV per division, with equal VOLTS/DIV switch settings on both channels.	
Displayed Channel 2 Signal Delay with Respect to Channel 1 Signal	Adjustable through a range of at least -500 ps to +500 ps.	
Input R and C (1 MΩ)		
Resistance	1 MΩ ±0.5%. ^a	
Capacitance	15 pF ±2 pF. ^a	
Maximum Input Voltage 	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less. ^a	
Input R (50 Ω)		
Resistance	50 Ω ±1%. ^a	
VSWR (DC to 300 MHz)	1.3:1 or less. ^a	
Maximum Input Voltage 	5 V rms; 0.5 W-seconds during any 1-s interval for instantaneous voltage from 5 V to 50 V.	
Cascaded Operation		
Bandwidth	Dc to 50 MHz or greater.	
Deflection Factor	400 μV per division ±10%.	
VERTICAL DEFLECTION SYSTEM—CHANNEL 3 AND CHANNEL 4		
Deflection Factor		
Values	0.1 V per division and 0.5 V per division.	
Accuracy	Within ±10%.	
Frequency Response	Six-division reference signal, from a terminated 50-Ω system.	
	-3-dB bandwidth with standard-accessory probe	-4.7-dB bandwidth with external 50-Ω termination
-15°C to +35°C	DC to 300 MHz	DC to 300 MHz
+35°C to +55°C	DC to 250 MHz	DC to 250 MHz

^aPerformance Requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING (cont)	
Minimum P-P Signal Amplitude for Stable Triggering from Channel 3 or Channel 4 Source	Amplitudes are one-half of Channel 1 or Channel 2 source specification.
Minimum P-P Signal Amplitude for Stable Triggering from Composite, Multiple Channel Source in ALT Vertical Mode	Add 1 division to single-channel source specification.
Maximum P-P Signal Rejected by NOISE REJ COUPLING for Signals Within the Vertical Bandwidth	
Channel 1 or Channel 2 Source	0.4 division or greater for VOLTS/DIV switch settings of 10 mV and higher. Maximum noise amplitude rejected is reduced at 2 mV and 5 mV per division.
Channel 3 or Channel 4 Source	0.2 division or greater.
Jitter	Less than 50 ps at 300 MHz with A and B SEC/DIV switch set to 5 ns and X10 MAG on.
LEVEL Control Range	
Channel 1 or Channel 2 Source	± 18 times the VOLTS/DIV switch setting. ^a
Channel 3 or Channel 4 Source	± 9 times the VOLTS/DIV switch setting. ^a
LEVEL Control Readout Accuracy (for triggering signals with transition times greater than 20 ns)	
Channel 1 or Channel 2 Source	
DC Coupled	
+15°C to +30°C	Within $\pm [3\% \text{ of setting} + 3\% \text{ of p-p signal} + 0.2 \text{ division} + (0.5 \text{ mV} \times \text{probe attenuation factor})]$.
-15°C to +55°C (excluding +15°C to +30°C)	Add (1.5 mV \times probe attenuation factor) to the specification listed for +15°C to +30°C.
NOISE REJ Coupled	Add ± 0.6 division to the DC Coupled specification.
Channel 3 or Channel 4 Source (DC Coupled)	Within $\pm [3\% \text{ of setting} + 4\% \text{ of p-p signal} + 0.1 \text{ division} + (0.5 \text{ mV} \times \text{probe attenuation factor})]$.
NOISE REJ Coupled	Within $\pm [3\% \text{ of setting} - 4\% \text{ of p-p signal} + 0.4 \text{ division} - (0.5 \text{ mV} \times \text{probe attenuation factor})]$.
SLOPE Selection	Conforms to trigger-source waveform or ac power-source waveform.
AUTO LVL Mode Maximum Triggering Signal Period	
A SEC/DIV Switch Setting Less than 10 ms	At least 20 ms. ^a
A SEC/DIV Switch Setting from 10 ms to 50 ms	At least four times the A SEC/DIV switch setting. ^a
A SEC/DIV Switch Setting from 100 ms to 500 ms	At least 200 ms. ^a

^aPerformance Requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
HORIZONTAL DEFLECTION SYSTEM (cont)	
Timing Accuracy (SEC/DIV VAR control out of detent)	Add 2% of time interval to the A and B Sweep Accuracy specification.
Timing Accuracy (-15°C to $+15^{\circ}\text{C}$ and $+35^{\circ}\text{C}$ to $+55^{\circ}\text{C}$)	Add $\pm 0.2\%$ of time interval to all Δt and delay specifications. Add $\pm 0.5\%$ of time interval to A and B Sweep accuracy specifications. ^a
Δt Readout Resolution	Greater of either 10 ps or 0.025% of full scale. ^a
Δt Range	± 10 times the A SEC/DIV switch setting. ^a
Delay Pickoff Jitter	Within 0.004% (one part or less in 25,000) of the maximum available delay, plus 100 ps.
Delay Time Position Range	0 to 9.95 times the A SEC/DIV switch setting. Main sweep triggering event is observable on delayed sweep with zero delay setting. ^a
X-Y Operation	
X-Axis Deflection Factor	
Range	Same as Channel 1. ^a
Accuracy	Same as Channel 1.
Variable Range	Same as Channel 1. ^a
X-Axis Bandwidth	Dc to 3 MHz.
Input R and C	Same as Channel 1. ^a
Phase Difference Between X and Y with Normal Bandwidth	1° or less from dc to 1 MHz; 3° or less from 1 MHz to 2 MHz.
X-Axis Low-Frequency Linearity	0.2 division or less compression or expansion of a two-division, center-screen signal when positioned within the display area.
CURSOR AND FRONT-PANEL DISPLAY	
Cursor Position Range	
Delta Volts (ΔV)	At least the center 7.6 vertical divisions.
Delta Time (Δt)	At least the center 9.6 horizontal divisions.
Minimum Setup Time Required to Maintain Front-panel Settings at Power-down	10 seconds or less. ^a

^aPerformance Requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
AC POWER SOURCE	
Source Voltage	
Ranges	
115 V	90 V to 132 V. ^a
230 V	180 V to 250 V. ^a
Source Frequency	48 Hz to 440 Hz. ^a
Fuse Rating	2 A, 250 V, AGC/3AG, Fast blow; or 1.6 A, 250 V, 5 x 20 mm, Quick-acting (F). ^a
Power Consumption	
Typical	70 W (140 VA). ^a
Maximum	120 W (180 VA). ^a
Primary Circuit Dielectric Voltage Withstand Test	1500 V rms, 60 Hz for 10 s without breakdown. ^a
Primary Grounding	Type test to 0.1 Ω maximum. Routine test to check grounding continuity between chassis ground and protective earth ground. ^a

^aPerformance Requirement not checked in manual.

Table 1-3
Mechanical Characteristics

Characteristics	Description
Weight	
With Accessories and Pouch	10.2 kg (22.4 lb).
Without Accessories and Pouch	9.3 kg (20.5 lb).
Domestic Shipping Weight	12.8 kg (28.2 lb).
Height	
With Feet and Accessories Pouch	190 mm (7.5 in).
Without Accessories Pouch	160 mm (6.3 in).
Width (with handle)	330 mm (13.0 in).
Depth	
With Front-Panel Cover	434 mm (17.1 in).
With Handle Extended	505 mm (19.9 in).
Cooling	Forced-air circulation.
Finish	Tektronix Blue vinyl-clad material on aluminum cabinet.
Construction	Aluminum-alloy chassis (sheet metal). Plastic-laminate front panel. Glass-laminate circuit boards.

Hewlett Packard Synthesizer/Function Generator

The following is an excerpt of *Hewlett Packard Synthesizer/Function Generator, Model 3325A*, Manual Part No. 03325-90001, January 1981.



**HEWLETT
PACKARD**

OPERATING AND SERVICE MANUAL

MODEL 3325A SYNTHESIZER/FUNCTION GENERATOR

Serial Number 1748A04551

IMPORTANT NOTICE

This manual applies to instruments with the above serial number and greater. As changes are made in the instrument to improve performance and reliability, the appropriate pages will be revised to include this information.

WARNING

To prevent potential fire or shock hazard, do not expose equipment to rain or moisture.

Manual Part No. 03325-90001

Microfiche Part No. 03325-90051

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P.O. Box 301, Loveland, Colorado 80537 U.S.A.

Printed: January 1981

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. The Operating and Service Manual contains information required to install, operate, test, adjust, and service the Hewlett-Packard Model 3325A Synthesizer/Function Generator. The Operating Information Supplement is a copy of the first four sections of the Operating and Service Manual. It also includes the Operational Verification procedures from Section IV, which may be used for incoming inspection. The supplement should be kept with the instrument for use by the operator. The part numbers of both the Operating and Service Manual and the Operating Information Supplement are shown on the title pages.

1-3. Also shown on the title page of this manual is a Microfiche part number. This number can be used to order 4 × 6 inch transparencies of the Operating and Service Manual. Each Microfiche contains up to 96 photo-duplicates of the manual pages. The Microfiche package includes the latest Manual Changes supplement as well as pertinent Service Notes.

1-4. Additional copies of the Operating and Service Manual, Operating Information Supplement, or Service Notes can be ordered through your nearest Hewlett-Packard Sales and Service Office. (A list of these offices is provided at the end of this manual.)

1-5. INSTRUMENT DESCRIPTION.

1-6. The Model 3325A Synthesizer/Function Generator produces the following signals at a minimum frequency of 1 μ Hz and maximum frequency of:

Sine wave	20 MHz
Square wave	10 MHz
Triangle	10 kHz
Positive slope ramp	10 kHz
Negative slope ramp	10 kHz

Frequency may be selected with up to eleven digits of resolution. Output amplitude is 1 mV to 10 V peak-to-peak. The output level may also be selected or displayed in V rms or in dBm (50 ohms). Any function may be dc offset up to ± 4.5 V, or the output may be dc only up to ± 5 V. An optional high voltage output produces up to 40 V p-p into ≥ 500 ohms load.

1-7. Frequency sweep of all functions is provided in linear or log sweep, at sweep times of 10 milliseconds to 99.99 seconds for linear sweep. Maximum time for log sweep is 99.99 seconds and minimum time is 2 seconds for single log sweep and 0.1 second for continuous log sweep. Single linear sweep may be up or down, while continuous sweep is up/down/up, etc., in the linear mode and up/up, etc., in log mode.

1-8. The Model 3325A is fully programmable through the rear panel Hewlett-Packard Interface Bus (HP-IB) connector. A device such as a programmable calculator is capable of remotely controlling the 3325A. Interface information is given in Section II of this manual, and programming information is in Section III.

1-9. SPECIFICATIONS.

1-10. Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Any changes in specifications due to manufacturing, design or traceability to the U.S. National Bureau of Standards are included in Table 1-1 of this manual and/or the Manual Changes Supplement. Specifications listed in this manual supersede all previous specifications for the Model 3325A.

1-11. SUPPLEMENTAL OPERATING INFORMATION.

1-12. Table 1-2 contains information describing general operating characteristics of the 3325A. This information is supplemental operating information and is not to be considered as specifications.

1-13. REMOTE CONTROL.

1-14. Table 1-3 lists the HP-IB interface capabilities of the Model 3325A in conformity with IEEE Standard 488-1975, "Standard Digital Interface for Programmable Instrumentation". HP-IB response times are given in Table 1-4.

1-15. OPTIONS.

1-16. The following options extend the frequency stability and output amplitude capabilities of the Model 3325A:

Option 001	High Stability Frequency Reference
Option 002	High Voltage Output

The following options indicate the line voltage to which the instrument was set at the factory:

Option 100	Nominal 100 V ac
Option 120	Nominal 120 V ac
Option 220	Nominal 220 V ac
Option 240	Nominal 240 V ac

Table 1-1. Specifications (Cont'd.)

Accuracy of DC Offset (into 50 ohms):

DC Only (No AC Function): $\pm 0.4\%$ of full output for each range**Except lowest attenuator range where accuracy is $\pm 20 \mu\text{V}$.DC + AC, $\leq 1 \text{ MHz}$: $\pm 1.2\%$, Ramps $\pm 2.4\%$ DC + AC, $> 1 \text{ MHz}$: $\pm 3\%$

AMPLITUDE MODULATION (of Sine function only)

Modulation Envelope Distortion: -30 dB to 80% modulation at 1 kHz , 0 V dc Offset

PHASE OFFSET

Range: $\pm 719.9^\circ$ with respect to arbitrary starting phase, or assigned zero phaseResolution: 0.1° Stability: $\pm 1^\circ \text{ phase}/^\circ\text{C}$ Increment Accuracy: $\pm 0.2^\circ$

PHASE MODULATION

Linearity (Sine Function): $\pm 0.5\%$, best fit straight line

SYNC OUTPUT

Output Levels into 50 ohms :Square wave with $V_{\text{high}} > +1.2 \text{ V}$, $V_{\text{low}} < +0.2 \text{ V}$

X DRIVE OUTPUT

Amplitude: 0 to $+10 \text{ V}$ dc linear ramp proportional to sweep frequency (sweep up only)Linearity, 10% to 90% , best fit straight line: $\pm 0.1\%$ of final value. Specified for all linear sweep widths which are integral multiples of the minimum sweep width for each function and sweep time.

OPTION 001

HIGH STABILITY FREQUENCY REFERENCE

Ambient Stability: $\pm 5 \times 10^{-8}$ (0° to 55°C referenced to $+30^\circ\text{C}$)Aging Rate: $\pm 5 \times 10^{-8}$ per week (after 72 hours continuous operation)
 $\pm 1 \times 10^{-7}$ per month (after 15 days continuous operation)

OPTION 002

HIGH VOLTAGE OUTPUT

Frequency Range:

Sine and Square Wave: $1 \mu\text{Hz}$ to 1 MHz Triangle and Ramps: $1 \mu\text{Hz}$ to 10 kHz

Amplitude:

Range: 4 mV p-p to 40 V p-p ($\geq 500 \Omega$, $< 500 \text{ pF}$ load) maximum output current, 40 mA p-p Accuracy (at 2 kHz): $\pm 2\%$ of full output for each rangeFlatness: $\pm 10\%$ of programmed amplitude

DC Offset:

Range: 4 times the range of the standard instrument

Accuracy: $\pm (1\% + 25 \text{ mV})$ of full output for each range

Signal Characteristics:

Sine Wave Harmonic Distortion (relative to the fundamental frequency at full output into $\geq 500 \text{ ohms}$, $< 500 \text{ pF}$)

Fundamental Frequency	No Harmonic Greater Than
10 Hz to 50 kHz	-65 dB
50 kHz to 200 kHz	-60 dB
200 kHz to 1 MHz	-40 dB

Square Wave:

Rise/Fall Time: $< 100 \text{ nanoseconds}$, 10% to 90% at full output with $\geq 500 \text{ ohm}$, $< 500 \text{ pF}$ loadOvershoot: $< 10\%$ of peak amplitude with $\geq 500 \text{ ohm}$, $< 500 \text{ pF}$ load

Table 1-2 Supplemental Information

MAIN SIGNAL OUTPUT

 50Ω Impedance

BNC Connector, switchable to front or rear panel (not switchable with Option 002)

May be floated a maximum of $\pm 42 \text{ V}$ peak (ac + dc) from chassis (earth) ground

Amplitude Ranges:

All AC Functions (with no dc offset):

Range No.	Attenuation Factor	Amplitude (Peak-to-Peak)
1	1	10.00 V to 3.000 V
2	3	2.999 V to 1.000 V
3	10	999.9 mV to 300.0 mV

4	30	299.9 mV to 100.0 mV
5	100	99.99 mV to 30.00 mV
6	300	29.99 mV to 10.00 mV
7	1000	9.999 mV to 3.000 mV
8	3000	2.999 mV to 1.000 mV

DC Offset Only:

Range No.	Attenuation Factor	Amplitude (Peak-to-Peak)
1	1	5.000 V to 1.500 V
2	3	1.499 V to 500.0 mV
3	10	499.9 mV to 150.0 mV
4	30	149.9 mV to 50.00 mV
5	100	49.99 mV to 15.00 mV
6	300	14.99 mV to 5.000 mV
7	1000	4.999 mV to 1.500 mV
8	3000	1.499 mV to 1.000 mV

Table 1-2. Supplemental Information (Cont'd).

X Drive Output (Sweep up only):

Amplitude: 0 to + 10 V linear ramp proportional to sweep frequency

Connector: Rear panel BNC

Z Blank Output:

Levels (TTL compatible voltage levels):

Linear Sweep:

Single: Low at start of sweep, High at stop. Remains High until start of next sweep.

Continuous: Low during sweep up, High during sweep down.

Log Sweep:

Single: Low at start of sweep, High at stop. Remains High until start of next sweep.

Continuous: Low during sweep. Goes High momentarily at stop frequency.

10 MHz Oven Reference Output, Option 001, for phase locking the 3325A to the optional high stability frequency reference:

Amplitude: 0 dBm, 50 ohms

Connector: Rear panel BNC. Must be connected to the rear panel EXT REF IN connector.

REMOTE CONTROL

Hewlett-Packard Interface Bus (HP-IB) Control: (HP-IB is Hewlett-Packard Company's implementation of IEEE Standard 488-1975). Time shown is in addition to programming time.

Frequency Switching and Settling Time:*

< 10 ms to within 1 Hz of final value for 100 kHz span

< 25 ms to within 1 Hz of final value for 1 MHz span

< 70 ms to within 1 Hz of final value for 20 MHz span

Phase Switching and Settling Time:*

< 15 ms to within 90° of phase lock for 20 MHz frequency change

Amplitude Switching Time:*

< 30 ms to within amplitude specifications

*Times shown are in addition to programming time

GENERAL**Operating Environment:**

Temperature: 0° to 55°C

Relative Humidity: < 95%, 0° to 40°C

Altitude: ≤ 15,000 ft.

Storage Temperature: - 50° to + 75°C

Storage Altitude: ≤ 50,000 ft.

Power Requirements:

100/120/220/240V + 5%, - 10%, 48 to 66 Hz
60 VA, 100 VA with all options, 10 VA standby

Dimensions in millimeters and (inches):

132.6 (5%) high × 425.5 (16%) wide × 497.8 (19.5/8) deep

Weight in kilograms and (lbs):

Net weight: 9(20)

Shipping Weight: 14.5 (32)

The following accessory options are also available for the Model 3325A:

Option 907	Front Handle Assembly
Option 908	Rack Mount Flange Kit
Option 909	Rack Mount Flange Kit/Front Handle Assembly
Option 910	Additional Operating and Service Manual

1-17. ACCESSORIES SUPPLIED.

1-18. A special connector is supplied with the High Stability Frequency Reference Option 001 for connecting the rear panel Reference Output to the Reference Input. This connector is Part No. 1250-1499.

1-19. ACCESSORIES AVAILABLE.

1-20. The following accessories are available for use with the Model 3325A:

Number	Description
11048C	50 ohm Feedthru Termination
11356A	Ground Isolator
03325-80001	Oven Board Assy. (Converts 3325A to Option 001)
03325-80002	High Voltage Option (Converts 3325A to Option 002)
5061-0077	Rack Mount Flange Kit (Option 908)
5061-0083	Rack Mount Flange/Front Handle Kit (Option 909)
5061-0089	Front Handle Kit (Option 907)

Hewlett Packard 8082A Pulse Generator

The following is an excerpt of *Hewlett Packard Pulse Generator, Model 8082A*, Operating and Service Manual No. 08082-90003, Sept. 1983.

OPERATING AND SERVICE MANUAL

8082A

PULSE GENERATOR

SERIAL NUMBERS

This manual applies directly to instrument with serial number 1822G02846 and higher. Any change made in instruments having serial numbers higher than the above number will be found in a "Manual Changes" supplement supplied with this manual. Be sure to examine the supplement for changes which apply to your instrument and record these changes in the manual. Backdating information for instruments with lower serial numbers can be found in Section 7 (yellow pages).

**c HEWLETT-PACKARD GMBH 1983
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FEDERAL REPUBLIC OF GERMANY**

**MANUAL PART No. 08082-90003
MICROFICHE PART No. 08082-90503**

PRINTED: SEP 1983

Printed in the Federal Republic of Germany

1-1 INTRODUCTION

1-2 The 8082A is a 250 MHz dual channel pulse source with variable leading and trailing edge transition times as fast as 1ns. It also has variable pulse frequency, delay, width, offset and amplitude. The normal/complement relationship and the polarity of either output can be reversed. Single pulse, double pulse and square wave operation are available. There are also four trigger modes:

1-3 Normal Mode. In this mode the 8082A operates as a self-contained pulse source with full control of the pulse parameters from the front panel controls.

1-4 Ext Trig Mode. In this mode the pulse and trigger output frequencies are determined by the frequency of an externally applied signal. The other pulse parameters are varied from the front panel controls.

1-5 Gate Mode. In this mode a gating signal enables the pulse and trigger outputs.

1-6 External Width Mode. In this mode the pulse frequency and width are determined by the frequency and width of an externally applied signal. The delay between input and output is fixed. The trigger output is the shaped trigger input signal.

1-7 ECL OUTPUT

1-8 The 8082A has an ECL position on each of its amplitude range switches. When either or both of the switches are set to this position, both 8082A outputs automatically deliver a fixed voltage swing of $-0.9V$ to $-1.7V$ typical (into an open circuit) for driving ECL logic.

Table 1-1 Specifications

These specifications apply when:

1) both outputs are terminated by a 50- Ω load,

2) the internal 50- Ω source impedance is selected.

PULSE CHARACTERISTICS

(Source and load impedance 50 Ω)

Transition Times: ≤ 1 ns to 0.5 ms in 6 ranges. First range from ≤ 1 ns to 5 ns controls leading and trailing edges simultaneously. For all other ranges transition times variable independently up to 1:10.

Difference between risetime and fall-time is less than 25% of the faster transition time of the two.

Overshoot and Ringing: $\leq \pm 5\%$ of pulse amplitude may increase to $\pm 10\%$ with amplitude vernier CCW.

Preshoot: $\leq \pm 5\%$ of pulse amplitude.

Linearity: Linearity aberration for both slopes $\leq 5\%$ for transition times > 5 ns.

Output: Maximum amplitude is 5V from 50 Ω into 50 Ω . Maximum output voltage is ± 5 V (amplitude + offset)

Offset: $> \pm 2$ V, into 50 Ω

Baseline: 0V ± 150 mV with offset switched off and amplitude range set to maximum. Other amplitude ranges reduce baseline proportionately.

DC Source Impedance: 50 $\Omega \pm 5\%$

Reflection Coefficient: Reflection is 2% typical for steps with 1 ns rise time applied to output connector on all amplitude ranges except 5V range. On the 5V range, the reflection may be 15%.

Output protection: Cannot be damaged by open or short circuits or application of ext $\leq \pm 6$ volts or ± 200 mA independent of control settings.

Attenuator: Two separate three step-attenuators reduce the outputs to 1V. Vernier is common for both outputs and reduces the output to 0.4V minimum. A further position provides ECL-compatible outputs (-0.9 V to -1.7 V typ. open circuit).

TIMING

Repetition Rate: > 250 MHz to < 1 kHz in 6 ranges.

Period Jitter: $< 0.1\% + 50$ ps

Delay: < 2 ns to > 0.5 ms in 6 ranges plus typ. 18 ns fxd. with respect to trigger output.

Delay Jitter: $< 0.1\% + 50$ ps

Double Pulse: Up to 125 MHz max (simulates 250 MHz). Min pulse spacing ≥ 4 ns.

Delay Duty Cycle: $> 50\%$

Pulse Width: < 2 ns to > 0.5 ms in 6 ranges.

Width Jitter: $< 0.1\% + 50$ ps

Width Duty Cycle: $> 50\%$

Square Wave: A further position of the Pulse Width switch provides Square Wave output (Delay and double pulse are disabled, max. Rep. Rate 250 MHz) Duty cycle is 50% $\pm 10\%$ up to 100 MHz, 50% $\pm 15\%$ for > 100 MHz

Trigger Output: Negative going Square Wave (50% duty cycle typ.) > 500 mV from 50 Ω into 50 Ω . Internal 50 Ω load can be switched off by slide-switch on PC-board. Amplitude increases to ≥ 1 V into 50 Ω up to 200 MHz

Trigger Output Protection: Cannot be damaged by short circuit or application of external ± 200 mA.

EXTERNALLY CONTROLLED OPERATION

External Input

Input Impedance: 50 $\Omega \pm 10\%$. DC coupled.

Maximum Input: ± 6 V

Trigger Level: Adjustable -1.5 V to $+1.5$ V.

Slope Control: Positive, negative or manual selectable. In the MAN-position all ext. functions can be controlled by push button. Button pushed in simulates an "on-signal".

Sensitivity: Sine-wave > 200 mVpp, pulses > 200 mV.

Repetition Rate: 0 to > 250 MHz.

Ext.-Controlled Modes

Ext. Trigger: There are approximately 7 ns delay between the external input and the trigger output. Rep. Rate is ext. controlled (is triggered by external signal). Trigger output provides the pulse-shaped input signal. Square wave mode is disabled

Synchronous Gating: Gating signal turns rep. rate generator on. Last pulse is of normal width even if gate ends during the pulse.

External Width: Output pulse width determined by width of drive input. Rep. Rate and Delay are disabled. Trigger output provides shaped input signal.

OPTIONS

Option 907	Front Handle Kit
Option 908	Rack Flange Kit
Option 909	Rack Flange plus Front Handle Kit
Option 910	Additional Instrument Manual

GENERAL

Power Requirements: 100V, 120V, 220V, 240V (+5%, -10%) 48 - 440 Hz. Power consumption 85VA max.

Weight: Net 7.9 kg (17.44 lbs), shipping 8.9 kg (19.63 lbs).

Dimensions: 426 mm wide, 145 mm high, 380 mm deep (16 3/4 ins. x 5 11/16 ins. x 15 ins.).

Hewlett Packard 5316A 100MHz Universal Counter

The following is an excerpt of *Hewlett Packard 100MHz Universal Counter, Model 5316A*, Operating and Service Manual, May 1981.

OPERATING AND SERVICE MANUAL

5316A 100 MHz Universal Counter

SERIAL PREFIX: 2120A

This manual applies to Serial Prefix 2120A, unless accompanied by a Manual Change Sheet indicating otherwise.

First Edition — May 1981

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5301 Stevens Creek Boulevard
Santa Clara, California 95050

MANUAL PART NUMBER 05316-90001
Microfiche Part Number 05316-90002

 **HEWLETT
PACKARD**

Model 5316A
General Information

Table 1-1. Model 5316A Specifications

INPUT CHARACTERISTICS
(Channel A and Channel B)

Range:

DC coupled, 0 to 100 MHz.
AC coupled, 30 Hz to 100 MHz.

Sensitivity:

10 mV rms sine wave to 10 MHz.
25 mV rms sine wave to 100 MHz.
75 mV peak-to-peak pulse at minimum pulse width of 5 ns.
Sensitivity can be varied continuously up to 500 mV rms
NOMINAL by adjusting sensitivity control. In sensitivity
mode, trigger level is automatically set to 0V **NOMINAL**.

Dynamic Range:

30 mV to 5V peak-to-peak, 0 to 10 MHz.
75 mV to 5V peak-to-peak, 10 to 100 MHz.

Signal Operating Range: +2.5V dc to -2.5V dc.

Coupling: AC or DC, switchable.

Filter: Low pass, switchable in or out of Channel A.
3 dB point of **NOMINALLY** 100 kHz.

Impedance:

1 MΩ **NOMINAL** shunted by less than 40 pF.

Attenuator: X1 or X20 **NOMINAL**.

Trigger Level: Variable between +2.5V dc and -2.5V dc.

Slope: Independent selection of + or - slope.

Common Input: All specifications are the same for Common A
except the following:

Sensitivity: 20 mV rms sine wave to 10 MHz.
50 mV rms sine wave to 100 MHz, 150 mV peak-to-peak.
Dynamic Range: 60 mV to 5V peak-to-peak 0-10 MHz,
150 mV to 5V peak-to-peak 10-100 MHz.
Impedance: 500 kΩ **NOMINAL** shunted by less than 70 pF.

Damage Level:

AC & DC × 1:

DC to 2.4 kHz 250V (DC + AC rms)
2.4 kHz to 100 kHz (6 × 10⁵ V rms × Hz)/FREQ
>100 kHz 6V rms

AC & DC × 20:

DC to 28 kHz 500V (DC + AC peak)
28 kHz to 100 kHz (1 × 10⁷ V rms × Hz)/FREQ
>100 kHz 100V rms

FREQUENCY (Channel A)

Range: .1 Hz to 100 MHz.

LSD Displayed: 10 Hz to 1 nHz depending upon gate
time and input signal. At least 7 digits displayed per
second of gate time

Resolution:

For FREQ <10 MHz;

$$\pm \text{LSD} \pm 1.4 \times \frac{\text{Trigger Error}}{\text{Gate Time}} \times \text{FREQ.}$$

For FREQ ≥ 10 MHz; ±LSD††

Accuracy: ± Resolution ± (time base error) × FREQ.

Range: .1 Hz to 100 MHz, both channels.

LSD:

$$\frac{2.5 \times \text{Period}}{\text{Gate Time}} \times \text{Ratio (rounded to nearest decade).}$$

where "Period" is the period of the highest frequency
input signal.

Resolution:

FREQ A > FREQ B

$$\pm \text{LSD} \pm \frac{\text{B Trigger Error}}{\text{Gate Time}} \times \text{Ratio.}$$

FREQ B > FREQ A

$$A = \frac{2.5 \times \text{Period A}}{\text{Gate Time}} \times \text{Ratio} \quad (\text{Rounded to nearest decade})$$

$$\pm A \pm \frac{\text{B Trigger Error}}{\text{Gate Time}} \times \text{Ratio}$$

Accuracy: Same as resolution.

TOTALIZE

Manual:

Range: 0 to 100 MHz.

A Gated By B:

Totalizes input A between two events of B. Instrument must be
reset to make new measurement. Gate opens on A slope, closes
on B slope.

Range: 0 to 100 MHz.

Resolution: ±1 count.

Accuracy: ±1 count ± B Trigger Error × Frequency A.

PERIOD

Range: 10 ns to 10⁵ s.

LSD Displayed: 100 ns to 1 fs depending upon gate time and
input signal. At least 7 digits displayed per second of
gate time.

Resolution:

For PER > 100 ns;

$$\pm \text{LSD} \pm 1.4 \times \frac{\text{Trigger Error}}{\text{Gate Time}} \times \text{PER.}$$

For PER ≤ 100 ns; ±LSD††

Accuracy: ± Resolution ± (time base error) × PER.

†Best Case Resolution for 1 Second Gate

	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz	100 MHz
50 mV rms	±.0004 Hz	±.00048 Hz	±.0014 Hz	±.01 Hz	±.1 Hz	±1 Hz	±10 Hz
100 mV rms	±.0002 Hz	±.00029 Hz	±.0012 Hz	±.01 Hz	±.1 Hz	±1 Hz	±10 Hz
500 mV rms	±.00005 Hz	±.00014 Hz	±.0011 Hz	±.01 Hz	±.1 Hz	±1 Hz	±10 Hz
1V rms	±.00003 Hz	±.00012 Hz	±.0010 Hz	±.01 Hz	±.1 Hz	±1 Hz	±10 Hz

This chart shows best case frequency resolution versus input sine wave rms amplitude.
This is best case because noise from the signal source is assumed to be zero; the trigger
error is produced only by the counter's noise (i.e., 120 μV rms).

††Due to arithmetic truncation, quantization error will be ±1 or ±2 counts of the
LSD (Least Significant Digit) as follows:

$$\pm 2 \text{ counts of LSD if } \frac{\text{LSD}}{\text{FREQ or PER}} < 1 \times 10^{-7}, \text{ FREQ} < 10 \text{ MHz.}$$

$$\pm 2 \text{ counts of LSD if } \frac{\text{LSD}}{\text{FREQ or PER}} < \frac{1/(\text{Gate Time})}{\text{FREQ}}, \text{ FREQ} \geq 10 \text{ MHz.}$$

±1 count of LSD for all other cases.

Table 1-1. Model 5316A Specifications (Continued)

TIME INTERVAL

Range: 100 ns to 10⁶ s.
LSD Displayed: 100 ns.
Resolution: $\pm \text{LSD} \pm \text{Start Trigger Error} \pm \text{Stop Trigger Error}$.
Accuracy: $\pm \text{Resolution} \pm (\text{time base error}) \times \text{T.I.}$

TIME INTERVAL AVERAGE

Range: 0 ns to 10⁶ s.
LSD Displayed: 100 ns to 10 ps depending upon gate time and input signal. See table in Definitions section.
Resolution:

$$\pm \text{LSD} \pm \frac{\text{Start Trigger Error}}{\sqrt{N}} \pm \frac{\text{Stop Trigger Error}}{\sqrt{N}}$$

Accuracy: $\pm \text{Resolution} \pm (\text{time base error}) \times \text{T.I.} \pm 4 \text{ ns}$.
Number of Intervals Averaged (N): $N = \text{Gate Time} \times \text{FREQ}$
Minimum Dead Time (stop to start): 200 ns.

TIME INTERVAL DELAY (Holdoff)

Front panel gate time knob inserts a variable delay of NOMINALLY 500 μ s to 20 ms between START (Channel A) and enabling of STOP (Channel B). Electrical inputs during delay time are ignored. Delay time may be measured by simultaneously pressing T.I. Average, T.I. Delay, and Blue Shift key. Other specifications of T.I. Delay are identical to Time Interval.

TIME BASE

Frequency: 10 MHz.
Aging Rate: $< 3 \times 10^{-7}/\text{mo}$.
Temperature: $\leq 5 \times 10^{-6}$, 0 to 50°C.
Line Voltage: $\leq 1 \times 10^{-7}$ for $\pm 10\%$ variation.
Oscillator Output: 10 MHz, 50 mV p-p into 50 Ω .
External Frequency Standard Input: 1, 5, 10 MHz, 1V rms into 500 Ω . on rear panel; 6V rms maximum.

GENERAL

Trigger Level Output: $\pm 5\% \pm 15 \text{ mV}$, over $\pm 2.0\text{V}$ dc range at front panel test connectors.
Check: Counts internal 10 MHz reference frequency over gate time range NOMINALLY 500 μ s to 30 ms.
Error Light: LED warning light activated if logic error is found during instrument turn-on self-check.
Display: 8-digit LED display, with engineering units annunciator.
Overflow: Only frequency and totalize measurements will overflow. In case of overflow, eight least significant digits will be displayed and front panel overflow LED will be actuated. All other measurements which would theoretically cause a display of more than eight digits will result in the display of the eight most significant digits.
Gate Time: Continuously variable, NOMINALLY from 60 ms to 10 s or 1 period of the input, whichever is longer. For FREQ A, a shorter gate time of 500 μ s–30 ms is selectable by simultaneously pressing T.I. Delay and Totalize keys.
Sample Rate: Up to seven readings per second NOMINAL except in time interval mode, where it is continuously variable NOMINALLY from four readings per second to 1 reading every 10 seconds via Gate Time control.
Operating Temperature: 0° to 50°C.
Power Requirements: Selectable 100, 120, 220, or 240V (+5%, -10%) 40–66 Hz; 30 VA maximum.
Dimensions: 212 mm W \times 88 mm H \times 415 mm D (8 3/8 \times 3 1/2 \times 16 1/2 in.).

Weight: Net, 3.9 kg (8 lbs. 10 oz.); Shipping, 6.3 kg (14 lbs.).
Rack and stack metal case with rear panel, switchable AC power line module.
Rack Mount Kit: S061-0072 recommended.

HP INTERFACE BUS (HP-IB)

Data Output

Format: (alpha character) \pm (Reading) (Exponent) \pm (2 digits).
Data Output Rate: ~ 7 Readings/second max. ~ 10 in short G.T.
Talk Only Mode: Selectable by rear panel switch.

Operating Commands

5316A: Reset, Initialize (to FREQ A), Wait State ON/OFF, Service Request Enabled/Disabled, Gate Time Range.
HP-IB: Group Execute Trigger, Device Clear, Selected Device Clear, Interface Clear, Local, Remote, Local Lockout, Read Status (Serial Poll Enable).

Programmable Controls and Functions

Frequency Functions: FREQUENCY A, FREQ A ARMED BY B, TOTALIZE, A GATED BY B, RATIO A/B, and FREQ C.
Period Function: Period A.
Time Interval Functions: Time Interval A–B, Time Interval Average A–B, Time Interval Delay.
Trigger Level Commands: Set Channel A Slope \pm , set Channel B Slope (\pm), A Trigger Level: $\pm X.XX$, B Trigger Level: $\pm X.XX$.
Gate Time Command: Sets Gate Time Range.
Miscellaneous Functions: Gate Time Check, Display Test, 10 MHz Check, Interface Test.

OPTIONS

OPTION 001: High Stability Time Base TCXO
Frequency: 10 MHz.
Aging Rate: $< 1 \times 10^{-7}/\text{mo}$.
Temperature: $< 1 \times 10^{-6}$, 0° to 40°C.
Line Voltage: $< 1 \times 10^{-8}$ for $\pm 10\%$ variation.

OPTION 003: C Channel

Input Characteristics

Range: 50 to 1000 MHz, prescaled by 10.
Sensitivity: 15 mV rms sine wave -23.5 dBm to 650 MHz. 75 mV rms sine wave -9.5 dBm to 1000 MHz.
Sensitivity can be decreased continuously by up to 20 dB NOMINAL, 50 to 500 MHz and 10 dB NOMINAL, 500 to 1000 MHz by adjusting sensitivity control. Trigger level is fixed at 0V NOMINAL.

Dynamic Range:

15 mV to 1V rms -36 dB , 50 to 650 MHz.
75 mV to 1V rms -20 dB , 650 to 1000 MHz.

Signal Operating Range: +5V dc to -5V dc.

Coupling: AC

Impedance: 50 Ω NOMINAL (VSWR, 12.5:1 TYPICAL).

Damage Level: $\pm 8\text{V}$ (DC + AC peak), fuse protected.

Fuse located in BNC connector.

Frequency

Range: 50 to 1000 MHz.
LSD Displayed: 100 Hz to 1 Hz depending upon gate time. At least 7 digits per second of gate time.
LSD, Resolution and Accuracy: Same formulas as for Frequency A except "Gate Time" term becomes "(Gate Time)/10".

Table 1-1. Model 5316A Specifications (Continued)

OPTIONS (Continued)

OPTION 004: Oven Oscillator

Frequency: 10 MHz.

Aging Rate: $<5 \times 10^{-8}$ /month after 7 days of continuous operation. $<3 \times 10^{-7}$ /year after 180 days continuous operation.

Warm-up: $\pm 5 \times 10^{-8}$ of final value after 20 minutes.

Temperature: $\pm 2 \times 10^{-8}$, 0° to 50°C.

Oscillator Output: 50 mV p-p into 50Ω.

DEFINITIONS:

Resolution: Smallest discernible change of measurement result due to a minimum change in the input.

Accuracy: Deviation from the actual value as fixed by universally accepted standards of frequency and time.

Least Significant Digit (LSD) Displayed:

Frequency:

$$\frac{2.5 \times 10^{-7}}{\text{Gate Time}} \times \text{FREQ, for FREQ} < 10 \text{ MHz.}$$

$$\frac{2.5}{\text{Gate Time}} \quad \text{for FREQ} \geq 10 \text{ MHz.}$$

Period:

$$\frac{2.5 \times 10^{-7}}{\text{Gate Time}} \times \text{PER, for PER} > 100 \text{ ns.}$$

$$\frac{2.5}{\text{Gate Time}} \times \text{PER}^2, \text{ for PER} \leq 100 \text{ ns.}$$

All above calculations should be rounded to nearest decade (i.e., 5 Hz will become 10 Hz and .4 ns will be .1 ns).

NOTE

Time Interval Average is a statistical process.
LSD displayed is calculated for 1 standard deviation (σ) confidence level.

Trigger Error:

$$\frac{\sqrt{120 \times 10^{-6} \text{V}^2 + e_n^2}}{\text{Input slew rate in V/s at trigger point}} \quad \text{seconds rms.}$$

Typical where e_n is the rms noise voltage of the input for a 100 MHz bandwidth.

Time Interval Average:

	LSD
1 to 25 intervals	100 ns
25 to 2500 intervals	10 ns
2500 to 250,000	1 ns
250,000 to 25,000,000 intervals	100 ps
>25,000,000 intervals	10 ps

Hewlett Packard 5180A Waveform Recorder

The following is an excerpt of *Hewlett Packard Waveform Recorder, Model 5180A*, Operating and Programming Manual, January 1982.

OPERATING AND PROGRAMMING MANUAL

5180A WAVEFORM RECORDER

SERIAL PREFIX: 2210A

This manual applies to Serial Prefix 2210A, unless accompanied by a Manual Change Sheet indicating otherwise.

First Edition — January 1982

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HEWLETT-PACKARD COMPANY
5301 Stevens Creek Boulevard
Santa Clara, California 95050

MANUAL PART NUMBER 05180-90001
Microfiche Part Number 05180-90002

Table 1-1. Model 5180A Specifications

CHANNEL A AND B INPUTS:Input Voltage Range: ± 100 mV to ± 10 V full scale in a 1-2-5 sequence.Input Offset: \pm selected voltage range in 1% increments; accuracy: $\pm 3\%$.Amplifier Bandwidth¹: ~ 3 dB; dc to 40 MHz (dc coupling).

10 Hz to 40 MHz (ac coupling).

Input Impedance (NOMINAL): 1 M Ω || ≤ 30 pF (10 V range).1 M Ω || ≤ 35 pF (all other ranges).

Input Coupling: AC or DC, switch selectable.

Damage Level: ± 25 V (DC + peak AC) to 1 kHz, ± 12 V above 1 kHz.Cross Talk²: CHAN A or B Mode: ≤ 60 dBCHOP A,B Mode: ≤ 36 dBCalibration Signals: 0 V ground and 100 mV dc reference may be applied to either channel. Accuracy (0°C to 55°C): $\pm 0.4\%$.Probe Compensation: Square wave: ± 1 V, 1 kHz NOMINAL.Damage Level: ± 25 V (DC + peak AC) to 1 kHz.**Dynamic Performance³ (20°C to 30°C):**

TEST	RANGE	NOMINAL SINE WAVE AMPLITUDE	NOMINAL TEST FREQUENCY	
			1 MHz	10 MHz
DFT-spurious ⁴	± 1 V	2 V p-p	≤ -50 dBc	≤ -46 dBc
Differential Nonlinearity ⁵	± 1 V	2.2 V p-p	≤ 3 LSB	≤ 4 LSB
Missing Codes ⁶	± 1 V	2.2 V p-p	NONE	NONE
Sine Wave Curve Fit ⁷	± 1 V	2 V p-p	≥ 7.8 bits	≥ 7.5 bits
S/N Ratio ⁸	± 1 V	2 V p-p	≥ 48.6 dB	≥ 46.8 dB

DC Performance:

Number of bits: 10

Relative Accuracy⁹: ± 2 LSBAbsolute Accuracy¹⁰: 0°C to 20°C: $\pm 5\%$ of range20°C to 30°C: $\pm 3\%$ of range30°C to 55°C: $\pm 5\%$ of range**AUXILIARY INPUT:**Input Voltage Range: ± 1 VAmplifier Bandwidth¹: ~ 3 dB; dc to 70 MHzInput Impedance (NOMINAL): 50 Ω

Input Coupling: DC

Damage Level: ± 1.5 V (DC + peak AC), fuse protected.**AUXILIARY INPUT (Continued)****Dynamic Performance³ (20°C to 30°C):**

TEST	NOMINAL SINE WAVE AMPLITUDE	NOMINAL TEST FREQUENCY	
		≤ 1 MHz	10 MHz
DFT-Spurious ⁴	2 V p-p	≤ -52 dBc	≤ -48 dBc
Differential Nonlinearity ⁵	2.2 V p-p	≤ 3 LSB	≤ 4 LSB
Missing Codes ⁶	2.2 V p-p	NONE	NONE
Sine Wave Curve Fit ⁷	2 V p-p 0.2 V p-p	≥ 8.0 bits ≥ 8.0 bits	≥ 7.7 bits ≥ 8.0 bits
S/N Ratio ⁸	2 V p-p	≥ 49.8 dB	≥ 48.0 dB

DC Performance:

Number of bits: 10

Relative Accuracy⁹: ± 1 LSBAbsolute Accuracy¹⁰: 0°C to 20°C: $\pm 2\%$ of range20°C to 30°C: $\pm 1\%$ of range30°C to 55°C: $\pm 2\%$ of range**TRIGGER CHARACTERISTICS****Internal Trigger:**

Slope: +, -, Bi-Trigger

Level: Digital triggering. Level may be entered in 1% increments over full scale range (FSR) or in absolute volts.

Hysteresis: Digitally selectable from 0% to 100% of full scale in 1% increments or as an absolute value.

Bi-Trigger: Triggers when input signal passes through either the more positive or more negative level. Bi-Trigger mode levels are set by hysteresis control and are centered about the selected trigger level.

External Trigger:

Slope: + or -

Level: Selectable over ± 2.5 V range; nominal increments of 20 mV.

Hysteresis: 100 mV NOMINAL, centered on selected trigger level.

Width: ≥ 30 ns

Input Impedance: 10K ohms NOMINAL

Coupling: DC

Maximum Input: ± 25 V**Sweep Arm Characteristics:**

Single: Pushbutton arms 5180A for single sweep after trigger.

Auto: Pushbutton arms 5180A for continuous free-run measurements. If no trigger occurs during a sweep, then a trigger is forced.

Norm: Pushbutton arms 5180A for continuous retriggered sweeps, one sweep after each trigger. If no trigger occurs, then there will be no sweep.

Arm Delay: Selectable 5 ms, 0.18 s, 0.25 s to 99 seconds in 0.25 second increments. Controls the time between measurements.

Table 1-1 Model 5180A Specifications (Continued)

Trigger Position:

Range: -100% of memory to +9999% of memory in 1% increments. Also settable in absolute time with maximum delay equal to one million sample intervals or 9,999 seconds.

TIMEBASE:

Sample Interval:

Internal: 50 ns to 50 ms in a 1-2-5 sequence. In Chop A,B mode, available sample intervals (each channel) are: 200 ns, 1 μ s, 2 μ s, ... to 50 ms in a 1-2-5 sequence. In Chop A,B mode, Channel B follows Channel A by 100 ns for all sample rates.

External timebase in (rear panel): Allowable frequency range is 1 MHz to 20 MHz. Divide ratios of 1 to 1-6 available in a 1-2-4 sequence. (Time measurements using cursors assume 20 MHz timebase; scaling required if frequency is less than 20 MHz.) Input impedance is 50 Ω NOMINAL. Timebase level switch selects thresholds of -0.3V (HP-EECL), and 0V (sine wave). With 1 k Ω series resistor (HP P/N 10871-60101), switch also selects thresholds for ECL and TTL.

Modes:

Main, Mixed, Toggle.

Internal Reference:

Aging Rate: $\pm 3 \times 10^{-6}$ per year.
Temperature: $\pm 2 \times 10^{-5}$ 0°C to 55°C.

Timebase Out: 20 MHz, 0 to -0.6 volt levels into 50 Ω .

MEMORY:

Size: 16384 words

Bits: 10

Segmentation: Memory may be segmented in 1, 2, 4, 8, 16, or 32 equal blocks. Recording: Data may be recorded in any memory block.

ANALOG OUTPUT MODES

XYZ CRT Monitor Outputs:

(These outputs are compatible with most HP oscilloscopes and CRT displays.)
XY Deflection Voltage: NOMINAL -1 to 0V full scale into 50 ohms; requires 5 MHz bandwidth input (Y); 1 MHz (X).

Z Voltage: NOMINAL 0 to 2V into 1 k Ω (0 to 1V, 50 Ω); selectable as a positive or negative going blanking pulse. 1.25 MHz bandwidth input required.

XY Recorder Control Outputs:

(These outputs are compatible with most HP XY recorders.)

XY Deflection Voltage: NOMINAL -1 to 0V full scale into 50 ohms.

Pen Lift Voltage: NOMINAL 0 to 5V output. Capable of operating a 45V solenoid. Will sink 1A, peak; 200 mA, continuous.

Time/Point Plotted: Selectable with front panel SPEED control.

HEWLETT-PACKARD INTERFACE BUS:

Programmable Controls: All front panel controls and functions except power on/stby switch

Special Functions: "Talk only" to HPGL plotters, with and without page advance. "Talk only" to printers and other tabular outputs.

Input and output of entire records or discrete data points in ASCII or Binary Learn Mode Commands.

HP-IB Commands: Trigger, Clear, Remote, Local, Local Lockout, Clear Lockout and Local, Require Service, Status Byte, Abort.

Data Output Rate: 3K byte/second maximum, depending on controller.

HIGH SPEED INPUT/OUTPUT (DMA rear panel connector):

10 Data Lines

6 HP-IB Address Indicator Lines

Controls Lines: Transfer Request* (Start/Stop data) Read/Write*

Data Transfer Type: 2 Line Handshake* or Single Line Strobe*

Data Transfer Mode (selectable by internal switch):

Automatic: Transferred data defined by 5180A record location and length.

Manual: Location of transferred data defined by 5180A record location;

Length of data string defined by Transfer request control line.

Data Input/Output Rate: 1M word/second maximum, depending on controller.

SERVICE AIDS:

Power-Up Test: Verifies high speed memory and microprocessor operation.

Service Interval Timer: Displays total operational time in seconds since last service calibration. Displayed at end of self-test.

Signature Analysis: Internal switches select from among 7 signature analysis routines. HP 5005A recommended for troubleshooting.

Service Loops: Internal switches select from among 6 microprocessor controlled service loop routines for troubleshooting.

Front Panel Troubleshooting: With HP-IB address switch set to 99, troubleshooting routines may be accessed from the front panel for fault isolation.

GENERAL

Front Panel Memory: Four complete front panel setups may be saved and recalled. Current setup is also saved in location 5 when a PRESET or AUTOSET is executed. Settings are stored for 4 days with no power.

Front Panel Lockout: Panel Lock key locks out front panel control: Unlock/Local key returns front panel control.

Calibrate: The CAL key places a known pattern on the external XYZ outputs for adjusting external display gains and offsets.

Dot/Line: Dot mode displays collected data via the XYZ outputs; Line mode displays the same points connected by curved lines generated by analog interpolation.

Self-Test: Initiates internal test of all RAM and ROM in the 5180A. Exercises internal displays and XYZ outputs. Performs input amplifier calibration check.

*TTL logic levels — Positive/negative logic selectable by internal switch

Table 1-1. Model 5180A Specifications (Continued)

Available Display Cursors: Trigger point cursor (intensified dot); Cursor (box shaped cursor); 5180A displays absolute volts or time from trigger point; Delta Cursor (cross shaped cursor); 5180A displays delta volts, delta time from cursor; trigger level and hysteresis cursors; timebase change cursor.

Display Zoom and Position: Zoom controls the horizontal spread of data displayed on the XYZ display. When zoomed out, the 5180A displays complete memory block selected, skipping points as necessary to reduce the total of 1024 points. Display may be zoomed in until points displayed correspond one for one with data in memory. Further zooming reduces number of displayed points to 256. Zoom value displayed is the number of data points in chosen record spanned by the display. The POSITION function controls the horizontal offset of the displayed portion of memory.

Display Gain and Offset: GAIN controls the vertical spread of the data displayed on the XYZ display. The GAIN value displayed is the full scale voltage range on the CRT display. The OFFSET function controls the vertical offset of the displayed data.

Single/Dual Display: Any two records may be simultaneously displayed. GAIN, OFFSET, ZOOM, POSITION may be specified independently for each trace.

TR1-TR2: Record defined as Trace 2 is subtracted point-by-point from record defined as Trace 1; content of original records remain unchanged.

Auto Advance: 5180A automatically advances to the next record of memory after each measurement. Arm delay determines time between measurements.

Trigger Time: Displays time of trigger, relative to set zero command, for selected memory record.

Bus Address: HP-IB address setting is displayed on 5180A display when Bus Address key is pressed.

Trigger Output (rear panel): Positive going signal from -0.6V to 0V into 50Ω used to synchronize triggering on multiple 5180A's.

N Chan Sync Input (rear panel): Synchronizes multiple 5180A timebase divide chains.

Armed Output (rear panel): TTL levels. Indicates 5180A is ready to be triggered.

Operating Temperature: 0°C to 55°C.

Power Requirements: 100/120/220/240 volts ±5%, -10%; 48 to 66 Hz -5% to 60 Hz +10%. Max power dissipation 400 watts.

Weight: Net, 22 kg (48 lbs.). Shipping, 24 kg (53 lb.).

Dimensions: 142mm H × 426 mm W × 574 mm D. (5 5/8" H × 16 3/4" W × 23" D) Excluding bottom feet and removable front handles.

1 Amplifier bandwidth is the bandwidth of the amplifier prior to the sample/hold. It is measured using a full scale sine wave in a beat frequency test. The amplifier bandwidth is found by determining the frequency of an input sine wave which causes the amplitude of the measured beat signal to decrease by 3 dB relative to the input signal amplitude.

2 Cross talk is the worst case ratio (in dB) between the rms signal level of a full scale sine wave input applied to either channel and the rms signal level which shows up in the alternate channel which has been terminated in 50Ω.

3 Dynamic Performance is specified only while using the internal timebase. The test signal is passed through 5-pole low pass filters (HP P/N 10871-60002) with cut off frequencies of 1 and 10 MHz.

4 The DFT-spurious specification for the 5180A specifies the maximum level of spurious signal (spurious means all unwanted signals, including harmonics of the input signal), relative to the test signal and is computed from DFT data at specified sine wave frequencies and amplitudes. Actual test frequencies are 0.95 MHz and 9.85 MHz. See Product Note 5180A-2 for details.

5 Differential nonlinearity is the maximum difference between the actual ADC transfer function step size and the ideal step size. Differential nonlinearity is computed from histogram data at specified sine wave frequencies and slightly greater than full scale amplitude. It is expressed in LSB (least significant bits) which equals full scale range/1024.

6 Missing codes specifies the number of codes in the ADC transfer function which do not occur as a function of input sine wave frequency. It is measured using histogram measurement techniques.

7 Sine wave curve fit — a full scale sine wave of specified frequency is digitized by the 5180A. An idealized sine wave of the form $A \sin(2\pi f t + \theta) + DC$ is fit to the data using a least squares fit and selecting A , f , θ , and DC to minimize the squared error. The idealized sine wave, $A_0 \sin(2\pi f_0 t + \theta_0) + DC_0$, is quantized in software by an ideal 10-bit ADC. The rms error (actual) between the actual data and the best fit sine wave is computed. The rms error between the idealized data (generated by an ideal 10-bit ADC) and the best fit sine wave is also computed. Then, the effective number of bits is computed as:

$$\text{effective bits} = 10 - \log_2 \frac{\text{rms error (actual)}}{\text{rms error (ideal)}}$$

The effective number of bits, then, is the number of bits in an ideal A-to-D whose quantization error would equal the rms error produced by the A-to-D under test. Actual test frequencies are 0.95 MHz and 9.85 MHz. The test record length is 1024 points. See Product Note 5180A-2 for details.

8 S/N Ratio — the ratio of rms signal to rms noise for a full scale input sine wave of specified frequency is specified. Computed from the sine wave curve fit test.

9 Relative accuracy is the maximum deviation of the ADC transfer function from a best fit straight line.

10 Absolute accuracy is the maximum deviation of the ADC transfer function from the ideal transfer function where the definition of the threshold levels is given in terms of absolute units as maintained by the National Bureau of Standards.

Tektronix DM 501A Digital Multimeter

The following is an excerpt of *Tektronix Digital Multimeter, Model DM 501A*, Instruction Manual, June 1979.



**PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL.**

**DM 501A
DIGITAL
MULTIMETER**

INSTRUCTION MANUAL

**Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077**

Serial Number _____

**070-2749-00
Product Group 75**

First Printing JUN 1979

SPECIFICATION

Introduction

The DM 501A Digital Multimeter measures dc voltage and current, ac voltage and current, dBm, dBV, resistance, and temperature. The ac functions are ac coupled only, true rms responding. All the functions and ranges are front panel push button selected, including the rear interface connector input.

Readout in dBm or dBV is selected by an internal jumper. The unit is shipped with the internal jumper in the dBm position.

The readout is a 0.4" high, 4 1/2 digit display using seven segment LED. The decimal point is automatically positioned depending on the selected operating range of the instrument. Polarity indication is automatic

Accessories

Standard accessories include this instruction manual, a set of test leads and the TEKTRONIX P6601 temperature probe with its instruction manual.

The P6601 temperature probe and temperature measurement capabilities are deleted for Option 2 instruments.

Performance Conditions

The electrical characteristics are valid only if the DM 501A has been calibrated at an ambient temperature between +21°C and -25°C and is operating at an ambient temperature between 0°C and -50°C, unless otherwise noted.

Items listed in the Performance Requirements column of the Electrical Characteristics are verified by completing the Performance Check in the Calibration section of this manual. These items are either explanatory notes or performance characteristics for which no limits are specified.

Table 1-1

ELECTRICAL CHARACTERISTICS (Front Panel)

Characteristics	Performance Requirements	Supplemental Information
DC VOLTMETER		
Accuracy for 200 mV, 2 V, 20 V 200 V and 1000 V ranges -18°C to +28°C		
200 mV range	$\pm(0.05\% \text{ of reading} - 0.015\% \text{ of full scale})$	
2 V to 200 V ranges	$\pm(0.05\% \text{ of reading} + 0.01\% \text{ of full scale})$	
1000 V range	$\pm(0.05\% \text{ of reading} + 0.02\% \text{ of full scale})$	
0°C to +18°C, -28°C to +50°C		
200 mV to 200 V range	$\pm(0.1\% \text{ of reading} + 0.025\% \text{ of full scale})$	
1000 V range	$\pm(0.1\% \text{ of reading} + 0.05\% \text{ of full scale})$	

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
DC VOLTMETER (cont)		
Common Mode Rejection Ratio	100 dB at dc. 80 dB at 50 and 60 Hz.	With a 1 k Ω unbalance.
Normal Mode Rejection Ratio	60 dB at 50 or 60 Hz ± 0.2 Hz.	
Maximum Resolution		10 μ V.
Step Response Time		<1 second.
Input Resistance		10 M Ω $\pm 0.5\%$.
Maximum Input Voltage		
VOLTS/ Ω to LOW		1000 V peak.
VOLTS/ Ω to ground		1000 V peak.
LOW to ground		1000 V peak.
Input Connectors		Front panel (EXT) or rear interface (INT)
AC VOLTMETER (TRUE RMS)		
Accuracy for 200 mV, 2 V, 20 V 200 V and 500 V ranges -18°C to -28°C		Input signal must be between 5% and 100% of full scale. The 500 V range requires a dynamic input signal between 500 V and 100 V rms
200 mV to 200 V ranges		
40 Hz to 10 kHz	$\pm(0.6\%$ of reading $- 0.05\%$ of full scale)	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(1.0\%$ of reading $- 0.05\%$ of full scale)	
500 V range		
40 Hz to 10 kHz	$\pm(0.6\%$ of reading $- 0.2\%$ of full scale)	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(1.0\%$ of reading $- 0.2\%$ of full scale)	
0°C to -18°C , -28°C to -50°C		
200 mV to 200 V ranges		
40 Hz to 10 kHz	$\pm(0.8\%$ of reading $- 0.075\%$ of full scale)	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(1.3\%$ of reading $- 0.075\%$ of full scale)	
500 V range		
40 Hz to 10 kHz	$\pm(0.8\%$ of reading $+ 0.3\%$ of full scale)	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(1.3\%$ of reading $+ 0.3\%$ of full scale)	

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
AC VOLTMETER (TRUE RMS) (cont)		
Common Mode Rejection Ratio	≥ 60 dB at 50 and 60 Hz.	With a 1 k Ω unbalance.
Maximum Resolution		10 μ V.
Response Time		< 2 seconds.
Input Impedance		10 M $\Omega \pm 0.5\%$ paralleled by 160 pF
Input Connectors		Front panel (EXT) or rear interface (INT).
Maximum Input Voltage		500 V rms or 600 Vdc not to exceed 1000 V peak.
VOLTS/ Ω to LOW		
VOLTS/ Ω to ground		1000 V peak.
LOW to ground		1000 V peak.
at Factor		4 at full scale.
DECIBELS (dB)—TRUE RMS		
or -40 dB, -20 dB, dB and $+40$ dB ranges		
$+18^\circ\text{C}$ to $+28^\circ\text{C}$		
-20 dB to -15 dB	± 0.5 dB 20 Hz to 20 kHz	
-15 dB to -20 dB	± 0.5 dB 20 Hz to 2 kHz ± 1.5 dB 2 kHz to 10 kHz	Typically ≤ 2.5 dB 10 kHz to 20 kHz.
0°C to -18°C , -28°C to -50°C		
-20 dB to -15 dB	± 1.1 dB 20 Hz to 20 kHz	
-15 dB to -20 dB	± 1.1 dB 20 Hz to 2 kHz ± 2.1 dB 2 kHz to 10 kHz	Typically ≤ 3.1 dB 10 kHz to 20 kHz.
Maximum Resolution		0.1 dB.
Response Time		< 2 seconds.
Input Impedance		10 M Ω paralleled by 160 pF.
Maximum Input Voltage		500 v rms or 600 Vdc not to exceed 1000 V peak.*
VOLTS/ Ω to LOW		
VOLTS/ Ω to ground		1000 V peak.
LOW to ground		1000 V peak.

*Equivalent to 54 dBV or 56.2 dBm.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
Crest Factor		4 at full scale.
Ref Voltage		
dBV		1 V.
dBm		0.7746 V (1 mW dissipated into 600 Ω). Selected by internal jumper.
Input Connectors		Front panel (EXT) or rear interface (INT).

OHMMETER

Accuracy for 200 Ω , 2 k Ω , 20 k Ω , 200 k Ω , 2000 k Ω and 20 M Ω ranges. +18°C to +28°C				
200 Ω to 200 k Ω LO Ω 2 k Ω to 2000 k Ω HI Ω	$\pm(0.15\%$ of reading + 0.015% of full scale)			
2000 k Ω LO	$\pm(0.3\%$ of reading + 0.015% of full scale)			
20 M Ω HI Ω	$\pm(0.5\%$ of reading + 0.015% of full scale)			
0°C to +18°C, -28°C to +50°C				
200 Ω to 200 k Ω LO Ω 2 k Ω to 2000 k Ω HI Ω	$\pm(0.3\%$ of reading + 0.025% of full scale)			
2000 k Ω LO Ω 20 M Ω HI Ω	$\pm(1.2\%$ of reading + 0.025% of full scale)			
Maximum Input Volts Any Range				250 V peak.
Measuring Current and Full Scale Volts		Range	Source Current	V Max at Full Scale
HI Ω		200 Ω	1.0 mA	0.2 V
		2 k Ω	1.0 mA	2.0 V
		20 k Ω	0.1 mA	2.0 V
		200 k Ω	10.0 μ A	2.0 V
		2000 k Ω	1.0 μ A	2.0 V
		20 M Ω	0.1 μ A	2.0 V
LO Ω		200 Ω	1.0 mA	0.2 V
		2 k Ω	0.1 mA	0.2 V
		20 k Ω	10.0 μ A	0.2 V
		200 k Ω	1.0 μ A	0.2 V
		2000 k Ω	0.1 μ A	0.2 V
		20 M Ω	0.1 μ A	2.0 V

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
Maximum Resolution		10 mΩ.
Response Time		<2 seconds, 200 Ω to 2000 kΩ. <10 seconds, 20 MΩ scale.
Maximum Open Circuit Voltage		<6 V.
Input Connectors		Front panel (EXT) or rear interface (INT).

DC AMMETER

Accuracy for 200 μ A, 2 mA, 20 mA, 200 mA and 2000 mA ranges. +18°C to +28°C	$\pm(0.2\% \text{ of reading} + 0.015\% \text{ of full scale})$													
0°C to -18°C, +28°C to -50°C	$\pm(0.3\% \text{ of reading} + 0.025\% \text{ of full scale})$													
Response Time		<1 second.												
Input Resistance		<table><tr><th>Range</th><th>Approximate Resistance</th></tr><tr><td>200 μA</td><td>1.0 kΩ</td></tr><tr><td>2 mA</td><td>100.0 Ω</td></tr><tr><td>20 mA</td><td>10.2 Ω</td></tr><tr><td>200 mA</td><td>1.2 Ω</td></tr><tr><td>2000 mA</td><td>0.4 Ω</td></tr></table>	Range	Approximate Resistance	200 μ A	1.0 k Ω	2 mA	100.0 Ω	20 mA	10.2 Ω	200 mA	1.2 Ω	2000 mA	0.4 Ω
Range	Approximate Resistance													
200 μ A	1.0 k Ω													
2 mA	100.0 Ω													
20 mA	10.2 Ω													
200 mA	1.2 Ω													
2000 mA	0.4 Ω													
Maximum Input Current		2 A any range.												
Maximum Open Circuit Input Voltage (mA to LOW)		250 V peak.												
Maximum Floating Voltage mA to ground		1000 V peak.												
LOW to ground		1000 V peak.												
Input Connectors		Front panel only.												
Maximum Resolution		10 nA.												

AC AMMETER

Accuracy for 200 μA, 2 mA, 20 mA, 200 mA and 2000 mA ranges.			
20 Hz to 10 kHz (Sinewave)			
-18°C to +2°C	±(0.6% of reading - 0.05% of full scale)	Input current must be between 5% and 100% of full scale.	
0°C to +18°C, +28°C to +50°C	±(0.7% of reading - 0.075% of full scale)	Usable to 20 kHz.	
Response Time		<2 seconds.	
Input Resistance			
		Range	Approximate Resistance
		200 μA	1.0 kΩ
		2 mA	100.0 Ω
		20 mA	10.2 Ω
		200 mA	1.2 Ω
		2000 mA	0.4 Ω

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
AC AMMETER (cont)		
Maximum Input Current		2 A any range.
Maximum Open Circuit Input Voltage (mA to LOW)		250 V peak.
Maximum Floating Voltage		
mA to ground		1000 V peak.
LOW to ground		1000 V peak
Input Connectors		Front panel only.
Maximum Resolution		10 nA
TEMPERATURE		
Accuracy for the -62°C to -240°C range.		
$+18^{\circ}\text{C}$ to $+28^{\circ}\text{C}$ ambient		
Probe calibrated to instrument	$\pm 2^{\circ}\text{C}$ from -62°C to -150°C . -0°C to -6°C from $+150^{\circ}\text{C}$ to -240°C	
Any probe	$\pm 4^{\circ}\text{C}$ from -62°C to -150°C . $+2^{\circ}\text{C}$ to -8°C from $+150^{\circ}\text{C}$ to $+240^{\circ}\text{C}$.	
0°C to -18°C . $+28^{\circ}\text{C}$ to $+50^{\circ}\text{C}$	Add 1.5°C to the above tolerance in each direction.	
Input Connectors		

Table 1-1 (cont)

ELECTRICAL CHARACTERISTICS (Rear Interface Inputs)

Characteristics	Performance Requirements	Supplemental Information
Maximum Input Voltage (dc, ac, dB, and ohms)		
Pin 28B to 28A		200 V peak. Equivalent to 43 dBV or 45.2 dBm.
Pin 28B to ground		200 V peak
Pin 28A to ground		200 V peak.

DC VOLTMETER (REAR INTERFACE INPUTS)

Accuracy for 200 mV, 2 V, 20 V, 200 V and 1000 V ranges.		
-18°C to +28°C		
200 mV range	$\pm(0.05\% \text{ of reading} - 0.015\% \text{ of full scale})$	
2 V to 200 V range	$\pm(0.05\% \text{ of reading} - 0.01\% \text{ of full scale})$	
1000 V range	$\pm(0.05\% \text{ of reading} + 0.02\% \text{ of full scale})$	
0°C to +18°C, +28°C to +50°C		
200 mV to 200 V range	$\pm(0.1\% \text{ of reading} - 0.025\% \text{ of full scale})$	
1000 V range	$\pm(0.1\% \text{ of reading} - 0.05\% \text{ of full scale})$	

(continues on next page)

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
AC VOLTMETER (REAR INTERFACE INPUTS)		
Accuracy for 200 mV, 2 V, 20 V, 200 V and 500 V ranges. -18°C to +28°C		Input signal must be between 5% and 100% of full scale input. The 500 V range is limited to between 200 V peak and 100 V rms.
200 mV to 200 V range		
40 Hz to 10 kHz	$\pm(1.6\% \text{ of reading} + 0.05\% \text{ of full scale})$	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(2.0\% \text{ of reading} + 0.05\% \text{ of full scale})$	
500 V range		
40 Hz to 10 kHz	$\pm(1.6\% \text{ of reading} + 0.2\% \text{ of full scale})$	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(2.0\% \text{ of reading} + 0.2\% \text{ of full scale})$	
0°C to +18°C, -28°C to +50°C		
200 mV to 200 V range		
40 Hz to 10 kHz	$\pm(1.8\% \text{ of reading} + 0.075\% \text{ of full scale})$	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(2.3\% \text{ of reading} + 0.075\% \text{ of full scale})$	
500 V range		
40 Hz to 10 kHz	$\pm(1.8\% \text{ of reading} + 0.3\% \text{ of full scale})$	
20 Hz to 40 Hz and 10 kHz to 20 kHz	$\pm(2.3\% \text{ of reading} + 0.3\% \text{ of full scale})$	

DECIBELS (dB)—TRUE RMS (REAR INTERFACE INPUTS)

Accuracy for -40 dB, -20 dB, 0 dB, -20 dB and -40 dB ranges -18°C to -28°C		
-20 dB to -15 dB	$\pm 0.6 \text{ dB } 20 \text{ Hz to } 20 \text{ kHz}$	
-15 dB to -20 dB	$\pm 0.6 \text{ dB } 20 \text{ Hz to } 2 \text{ kHz}$ $\pm 1.6 \text{ dB } 2 \text{ kHz to } 10 \text{ kHz}$	Typically <2.6 dB 10 kHz to 20 kHz
0°C to -18°C, -28°C to -50°C		
-20 dB to -15 dB	$\pm 1.2 \text{ dB } 20 \text{ Hz to } 20 \text{ kHz}$	
-15 dB to -20 dB	$\pm 1.2 \text{ dB } 20 \text{ Hz to } 2 \text{ kHz}$ $\pm 2.2 \text{ dB } 2 \text{ kHz to } 10 \text{ kHz}$	Typically <3.2 dB 10 kHz to 20 kHz

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
OHMMETER (REAR INTERFACE INPUTS)		
Accuracy for 200 Ω , 2 k Ω , 20 k Ω , 200 k Ω , 2000 k Ω , and 20 M Ω ranges +18°C to +28°C		
200 Ω to 200 k Ω LO Ω 2 k Ω to 2000 k Ω HI Ω	$\pm(0.15\%$ of reading - 0.015% of full scale) - 0.02 Ω	
2000 k Ω LO Ω	$\pm(0.3\%$ of reading - 0.015% of full scale) - 0.02 Ω	
20 M Ω HI Ω	$\pm(0.5\%$ of reading - 0.015% of full scale) - 0.02 Ω	
0°C to -18°C, -28°C to -50°C		
200 Ω to 200 k Ω LO Ω 2 k Ω to 2000 k Ω HI Ω	$\pm(0.3\%$ of reading - 0.025% of full scale) - 0.02 Ω	
2000 k Ω LO Ω 20 M Ω HI Ω	$\pm(1.2\%$ of reading - 0.025% of full scale) - 0.02 Ω	

Table 1-2

MISCELLANEOUS

Characteristics	Description
Power Consumption	Approximately 9 watts.
Reading Rate	3 1/3 per second.
Over-range Indication	Flashing display except on 500 Vac and 1000 Vdc ranges.
Calibration Interval	1000 hours of operation or 6 months, whichever occurs first.
Warm-up Time	30 minutes (60 minutes after storage in high humidity environment).

Table 1-3
ENVIRONMENTAL¹

Characteristics	Description	
Temperature		
Operating	0°C to -50°C ^a	Meets or exceeds MIL-T-28800B, class 5 with exceptions. ^d
Non-operating	-55°C to -75°C	
Humidity	95% to 100% for 5 days (derated above 25°C)	Meets or exceeds MIL-T-28800B, class 5
Altitude		
Operating	4.6 km (15,000 ft)	Meets or exceeds MIL-T-28800B, class 3.
Non-operating	15 km (50,000 ft)	
Vibration	0.64 mm (0.025") disp. 5-55-5 Hz ^a (sine wave) 75 min. total	Meets or exceeds MIL-T-28800B, class 3
Shock	30 g s (half sine) 11 ms 18 shocks ^a	Meets or exceeds MIL-T-28800B, class 3
Bench Handling		
Operating	45° or 4" or equilibrium ^a , whichever occurs first.	Meets or exceeds MIL-T-28800B, class 3.
E.M.C.		
Operating	30 Hz to 1 GHz ^b	Meets or exceeds MIL-T-28800B, class 3.
Electrical Discharge		
Operating	20 kV max. ^b	No MIL-T-28800 equivalent Charge applied to each protruding area of the front panel except the input connectors
Transportation		
Vibration	25 mm (1 inch at 270 rpm for 1 hr) ^c	National Safe Transit Association Preshipment Test Procedures project: 1A-B-1 and 1A-B-2.
Package Drop	10 drops from 3 ft (91 cm) ^c	

¹See Table 1-4 for system modifiers.^aWith power module.^bWithout power module.

^cTemperature: During low temperature test MIL-T-28800B paragraph 4.5.5.1.3 (b) for class 5, steps 4 and 5 shall be performed before step 2. Also, the instrument shall not be operating during step 8, paragraph 4.5.5.1.3 (e), class 5. While operating, condensed moisture shall not be present on class 5 instruments. Drying of the instrument for this class may be performed in a suitable chamber, if necessary.

Table 1-3
TM 500 SYSTEMS
ENVIRONMENTAL SPECIFICATION

Characteristics	TM 501	TM 503	TM 504	TM 506	TM 515
Temperature	Meets same test standards as plug-in.				
Operating					
Non-operating					
Humidity	Meets same test standards as plug-in.				
Operating					
Non-operating					
Altitude	Meets same test standards as plug-in.				
Operating					
Non-operating					
Vibration					
Operating	0.26 mm (0.010 in.) disp., 10-55 Hz (sine wave), 75 min. total.				0.38 mm (0.015 in.) disp. 10-55 Hz (sine wave) 75 min.
Shock					
Operating	20 g's (1/2 sine) 11 ms, 18 shocks				30 g's (1/2 sine) 11 ms, 18 shocks.
Bench Handling	Meets same test standards as plug-in.				
Operating					
Electric Discharge	Meets same test standards as plug-in.				
Operating					
Transportation	Meets same test standards as plug-in.				
Vibration					
Package Drop					

Table 1-5
PHYSICAL CHARACTERISTICS

Characteristics	Description
Finish	Anodized aluminum panel and chassis.
Net Weight	≈2.5 lbs (1.13 kg).
Overall Dimensions	2.633 in. (66.8 mm) W x 11.240 in. (285.3 mm) D x 4.961 in. (125.9 mm) H.

Tektronix FG 504 40MHz Function Generator

The following is an excerpt of *Tektronix 40MHz Function Generator, Model FG 504*, Instruction Manual, May 1982.

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FG 504 40 MHz FUNCTION GENERATOR

(SN B0400000 & ABOVE)

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077
070-2655-00

Serial Number _____

SPECIFICATION

Introduction

The FG 504 Function Generator provides low distortion sine, square, triangle, ramp, and pulse waveforms over the frequencies from 0.001 Hz to 40 MHz in ten decades. A user-definable custom frequency range is also available. The output amplitude is 10 mV to 30 V peak-to-peak into an open circuit and 5 mV to 15 V peak-to-peak into a 50 Ω load. The output impedance is 50 Ω . The FG 504 may be swept between the START and STOP FREQ dial settings with a linear or logarithmic sweep. The output may be phase locked, gated, or triggered for single cycle output. The output waveform may be shifted $\pm 80^\circ$ from the triggering waveform. The symmetry of the output waveform may also be varied. For the slower frequencies, the output may be held at any level by pushing the front panel button labeled HOLD.

A voltage-controlled frequency (VCF) input controls the output frequency from an external voltage source. The output frequency can be swept above or below the selected frequency, to a maximum of 1000.1, depending on the polarity and amplitude of the VCF input and the selected output frequency. Provision is also made for amplitude modulating the sinewave output from an external source.

The variety of swept and modulated signals available from the FG 504 make it especially useful for such applications as testing amplifier or servo-system response, distortion, and stability. It is useful for fm generation, as a beat frequency oscillator, as a gated triggered or phase-locked logic interface, or as a source for various ramp or pulse waveforms. It is also useful as a source for amplitude modulated signals for various purposes.

SPECIFICATION

Performance Conditions

The following electrical characteristics are valid if the FG 504 is calibrated at an ambient temperature between $+20^\circ\text{C}$ and $+30^\circ\text{C}$ and is operated at an ambient temperature between 0°C and $+50^\circ\text{C}$, unless otherwise noted. Forced air circulation is required at temperatures above $+40^\circ\text{C}$. Allow a one-hour warm-up period before performing verification tests.

Table 1-1
ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Frequency		
Range		
Sine-wave, square-wave, and triangle	.001 Hz to 40 MHz calibrated in 10 overlapping steps	
Ramps, pulses, or waveforms requiring use of variable SYMMETRY control		.001 Hz to nominally 4 MHz.
Duty Cycle		$\leq 7\%$ to $\geq 93\%$ below 1 MHz $\leq 20\%$ to $\geq 80\%$ above 1 MHz
5×10^1 position of MULTIPLIER switch (User selected timing capacitor)		=400 kHz maximum. A 5 μF capacitor provides a full-scale frequency of ≈ 400 Hz. The factory-installed capacitor gives a 20 Hz to 20 kHz range for the $.5 \times 10^1$ position of the MULTIPLIER switch.

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information										
Frequency (cont)												
Resolution		1 part in 10 ⁴ of full-scale setting using the FREQUENCY VERNIER control, as measured with a frequency counter.										
Stability		Applies to calibrated portion of the FREQUENCY Hz dial only.										
Time	≤0.05% for 10 minutes ≤0.1% for 1 hour ≤0.5% for 24 hours	The instrument must be at a constant ambient temperature between 0° C and +50° C and checked after a 1-hour warmup.										
Temperature		See Dial Accuracy										
Dial Calibration		1 to 40 Hz (X MULTIPLIER setting) calibrated; 0.1 to 1 Hz (X MULTIPLIER setting) uncalibrated										
Dial Accuracy												
FREQUENCY Hz (START) dial	Within 3% of full scale from 0.001 Hz to 4 MHz. Within 6% of full scale from 4 MHz to 40 MHz.	Measurements made at an ambient temperature between +15° CC and -35° C after 1 hour warmup.										
STOP FREQUENCY dial	Within 5% of the difference between the start and stop frequencies plus the FREQUENCY Hz (START) dial error	STOP FREQUENCY dial is uncalibrated on the 10 ⁴ MULTIPLIER range.										
Maximum Frequency Ranges for Dial, Sweep Frequency, and Voltage Controlled Frequency (VCF) Modes	<table><tr><th>MULTIPLIER Setting</th><th>Maximum to Minimum Frequency Ratios</th></tr><tr><td>10⁰</td><td>≥500:1</td></tr><tr><td>10¹ - 10²</td><td>≥1000:1</td></tr><tr><td>10¹, 10⁻¹, 10⁻²</td><td>≥100:1</td></tr><tr><td>10⁻¹</td><td>≥40:1</td></tr></table>	MULTIPLIER Setting	Maximum to Minimum Frequency Ratios	10 ⁰	≥500:1	10 ¹ - 10 ²	≥1000:1	10 ¹ , 10 ⁻¹ , 10 ⁻²	≥100:1	10 ⁻¹	≥40:1	
MULTIPLIER Setting	Maximum to Minimum Frequency Ratios											
10 ⁰	≥500:1											
10 ¹ - 10 ²	≥1000:1											
10 ¹ , 10 ⁻¹ , 10 ⁻²	≥100:1											
10 ⁻¹	≥40:1											
Internal Sweep Accuracy		Linear or Logarithmic. Limited by Start and Stop Frequency Specifications; use external frequency counter if greater accuracy is required										
Sweep Duration		100 s to 0.1 ms in six decades (selected by SWEEP DURATION switch). VARIABLE control overlaps decades.										
Stop Frequency to Swept Stop Frequency Error		Within 2% from 100 s to 1 ms sweep duration. Within 10% from 1 ms to 0.1 ms sweep duration.										
LINEar SWEEP	0 V to -10 V.	Output impedance 1 kΩ.										

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Internal Sweep (cont)		
OUTPUT Amplitude		
Accuracy	Within 5% from 100 s to 1 ms. Within 10% from 1 ms to 0.1 ms.	
SWEEP TRIGger INPUT		
Input sensitivity	1 V p-p.	
Level	1 V through 10 V	
Maximum Input	+ 20 V.	
Manual Trigger		Front-panel control.
Voltage-controlled Frequency Input (VCF)		
Nominal Sensitivity (Hz/volt)		= 4 X MULTIPLIER setting per voltage. A positive-going voltage increases frequency.
Maximum Frequency		= 40 X MULTIPLIER setting
Minimum Frequency		Maximum frequency divided by VCF range (see Maximum Frequency Ranges for Dial, Sweep Frequency, and Voltage Controlled Frequency (VCF) Modes)
Slew Rate		0.3 V/μs maximum
Input Impedance		10 kΩ.
OUTPUT Signal Amplitude	At least 30 V p-p into an open circuit, at least 15 V into 50 Ω.	
Flatness		
Sine-wave		
0.001 Hz to 40 kHz	Within ±0.5 dB	Typically within ±0.5 dB to 40 MHz. Reference at 10 kHz
40 kHz to 40 MHz	Within ±2 dB from 40 kHz to 40 MHz.	
Triangle		
0.001 Hz to 40 kHz	Within ±0.5 dB	Reference at 10 kHz
40 kHz to 40 MHz.	Within ±2 dB	
Square-wave		
0.001 Hz to 20 MHz	Within ±0.5 dB.	Reference at 10 kHz.
20 MHz to 40 MHz	Within ±2 dB.	
Sine-wave, Triangle, and Square-wave Amplitude Match	Within ±1 dB at 10 kHz.	

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information														
Output ATTENUATOR	<table><tr><th>Attenuator Step</th><th>Maximum Open-circuit Output Voltage (p-p)</th></tr><tr><td>0 dB</td><td>30 V</td></tr><tr><td>-10 dB</td><td>9.5 V</td></tr><tr><td>-20 dB</td><td>3 V</td></tr><tr><td>30 dB</td><td>950 mV</td></tr><tr><td>-40 dB</td><td>300 mV</td></tr><tr><td>50 dB</td><td>95 mV</td></tr></table>	Attenuator Step	Maximum Open-circuit Output Voltage (p-p)	0 dB	30 V	-10 dB	9.5 V	-20 dB	3 V	30 dB	950 mV	-40 dB	300 mV	50 dB	95 mV	
Attenuator Step	Maximum Open-circuit Output Voltage (p-p)															
0 dB	30 V															
-10 dB	9.5 V															
-20 dB	3 V															
30 dB	950 mV															
-40 dB	300 mV															
50 dB	95 mV															
Accuracy	Within ± 0.5 dB/decade.															
VARIABLE Control	Provides up to -20 dB additional attenuation to reduce the minimum output signal amplitude to 10 mV.															
OFFSET Range																
Into Open Circuit	± 7.5 V	Maximum signal plus offset peak output amplitude of ± 20 V into an open circuit and ± 11.25 V into 50 Ω . Offset defeatable by front-panel control														
Into 50 Ω	± 3.75 V															
Output Waveforms																
Without Use of SYMMETRY (variable) control		Sine, Triangle, and Square														
With SYMMETRY (variable) Control		Ramps and Pulses. Duty cycle range is $\sim 7\%$ to $\sim 93\%$ for all variable symmetry waveforms below 1 MHz limited to $\sim 20\%$ to $\sim 80\%$ for triangle and sine-waveforms above 1 MHz Actuation of SYMMETRY control divides output frequency by approximately 10.														
Triangle																
Symmetry		Typically within 2% from 0.001 Hz to 10 Hz.														
10 Hz to 400 kHz 400 kHz to 40 MHz	Within 1% Within 5%	On calibrated portion of FREQUENCY Hz dial.														
Linearity		Measured from the 20% point to the 80% point of the waveform. Typically within 2% from 0.001 Hz to 10 Hz.														
10 Hz to 400 kHz 400 kHz to 4 MHz 4 MHz to 40 MHz		Within 1%. Within 2%. Within 10%.														

Specification—FG 504 (SN 2040000 & UP)

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
External TRIG/GATE Φ LOCK Input (cont)		
Maximum Trigger Frequency	20 MHz.	
GATE		
Minimum Period		75 ns.
Maximum Gated Frequency	20 MHz.	For gating multiple-cycle burst of generator waveform.
Φ LOCK	100 Hz to 40 MHz. Adjust range $\pm 80^\circ$ from 0 100 Hz to 4 MHz.	Capture range: ± 10 major dial divisions from 100 Hz to 4 MHz; ± 8 major dial divisions from 4 MHz to 40 MHz (40 MHz may not capture, but will track.)
4 MHz to 40 MHz	± 8 major dial divisions.	
Lock Range		Generator will lock to a changing external signal, without readjusting the PHASE control within ± 10 major dial divisions from 100 Hz to 4 MHz and within ± 1 MHz from 4 MHz to 40 MHz.
PHASE		
Phase Adjustment Range		$\pm 80^\circ$ from 0.001 Hz to 4 MHz
MAN		Manual Trigger/Gate front-panel pushbutton
TRIG OUTPUT	0 V to 2 V from 50 Ω .	
HOLD		
Drift		10% of p-p output amplitude hour
Range	0 001 Hz to 400 Hz	

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Output Waveforms (cont)		
Sine-Wave		
Total Harmonic Distortion		Typically $\leq 1\%$ from 0.001 Hz to 20 Hz, measured under the following conditions: Temperature -10°C to -35°C ambient terminated into 50 Ω ; zero offset; ≤ 30 dB attenuation, and with FREQUENCY Hz (START) dial set between 4 and 40.
20 Hz to 40 kHz	0.5%	
40 kHz to 1 MHz	Greatest harmonic at least 30 dB down.	
1 MHz to 40 MHz	Greatest harmonic at least 20 dB down.	
Square-wave		
RISE AND FALL TIMES FIXED	≤ 6 ns 10 ns to 100 ms in 7 steps measured from 10% to 90%	Applies to pulse waveforms also
Aberrations	$\leq 5\%$ p-p plus 30 mV into 50 Ω load.	
VARIABLE	10 ns to 100 ms in 7 steps. Measured between the 10% and 90% points of Amplitude; accuracy within 30%. VARIABLE control has $\geq 10\text{X}$ range.	Period of waveform must exceed combined rise and fall times by 20%.
AM INPUT		
Dc to 4 MHz	5 V p-p signal produces 100% modulation of a sine-wave carrier with 5% distortion at 70% modulation	When driven from a source impedance 600 Ω .
4 MHz to 40 MHz	10% distortion at 65% modulation	Modulating frequencies from 20 Hz to 20 kHz. Modulation frequency bandwidth is dc to 100 kHz. A modulating source impedance of 10 k Ω ensures proper modulation and divides the output amplitude by 2.
Input Impedance		1 M Ω .
External TRIG. GATE Φ LOCK Input		
Input Impedance		10 k Ω .
Sensitivity	1 V p-p.	
Maximum Input Amplitude		20 V
TRIG		
LEVEL	-1 V to +10 V.	For triggering a single cycle of generator waveform.
Minimum Period		75 ns.

Table 1-2

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Description
Temperature	
Operating	0°C to -40°C (-40°C to -50°C, forced air required).
Storage	-40°C to +75°C.
Altitude	
Operating	To 15,000 feet (4,570 meters).
Storage	To 50,000 feet (15,250 meters)
Vibration	
Operating and non-operating	0.64 mm (0.025") displacement, 10-50-10 Hz sinewave, 54 minutes
Shock	
Operating and non-operating	50 g's (half sine), 11 ms, 12 shocks.
Transportation	Qualified under National Safe Transit Association Test, Procedure 1A Category II.

Table 1-3

PHYSICAL CHARACTERISTICS

Characteristics	Description
Finish	Anodized aluminum panel and chassis.
Weight	3.75 pounds (1.7 kg).
Overall Dimensions	Width 5.312" (13.49 cm), Length 12.125" (30.8 cm), Height 5.0" (12.7 cm).

Tektronix FG 504 40MHz Function Generator

The following is an excerpt of *Tektronix 40MHz Function Generator, Model FG 504*, Instruction Manual, May 1982.



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**FG 504
40 MHz
FUNCTION
GENERATOR**
(SN B0400000 & ABOVE)

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

SPECIFICATION

Introduction

The FG 504 Function Generator provides low distortion sine, square, triangle, ramp, and pulse waveforms over the frequencies from 0.001 Hz to 40 MHz in ten decades. A user-definable custom frequency range is also available. The output amplitude is 10 mV to 30 V peak-to-peak into an open circuit and 5 mV to 15 V peak-to-peak into a 50 Ω load. The output impedance is 50 Ω . The FG 504 may be swept between the START and STOP FREQ dial settings with a linear or logarithmic sweep. The output may be phase locked, gated, or triggered for single cycle output. The output waveform may be shifted $\pm 80^\circ$ from the triggering waveform. The symmetry of the output waveform may also be varied. For the slower frequencies, the output may be held at any level by pushing the front panel button labeled HOLD.

A voltage-controlled frequency (VCF) input controls the output frequency from an external voltage source. The output frequency can be swept above or below the selected frequency, to a maximum of 1000:1, depending on the polarity and amplitude of the VCF input and the selected output frequency. Provision is also made for amplitude modulating the sinewave output from an external source.

The variety of swept and modulated signals available from the FG 504 make it especially useful for such applications as testing amplifier or servo-system response, distortion, and stability. It is useful for fm generation, as a beat frequency oscillator, as a gated triggered or phase-locked logic interface, or as a source for various ramp or pulse waveforms. It is also useful as a source for amplitude modulated signals for various purposes.

SPECIFICATION

Performance Conditions

The following electrical characteristics are valid if the FG 504 is calibrated at an ambient temperature between $+20^\circ\text{C}$ and $+30^\circ\text{C}$ and is operated at an ambient temperature between 0°C and -50°C , unless otherwise noted. Forced air circulation is required at temperatures above $+40^\circ\text{C}$. Allow a one-hour warm-up period before performing verification tests.

Table 1-1

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Frequency		
Range		
Sine-wave, square-wave, and triangle	.001 Hz to 40 MHz calibrated in 10 overlapping steps	
Ramps, pulses, or waveforms requiring use of variable SYMMETRY control		.001 Hz to nominally 4 MHz.
Duty Cycle		$\leq 7\%$ to $\geq 93\%$ below 1 MHz $\leq 20\%$ to $\geq 80\%$ above 1 MHz
5×10^1 position of MULTIPLIER switch (User selected timing capacitor)		≈ 400 kHz maximum. A 5 μF capacitor provides a full-scale frequency of ≈ 400 Hz. The factory-installed capacitor gives a 20 Hz to 20 kHz range for the $.5 \times 10^1$ position of the MULTIPLIER switch.

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information										
Frequency (cont)												
Resolution		1 part in 10 ⁴ of full-scale setting using the FREQUENCY VERNIER control, as measured with a frequency counter.										
Stability		Applies to calibrated portion of the FREQUENCY Hz dial only.										
Time	≤0.05% for 10 minutes ≤0.1% for 1 hour ≤0.5% for 24 hours	The instrument must be at a constant ambient temperature between 0° C and +50° C and checked after a 1-hour warmup.										
Temperature		See Dial Accuracy										
Dial Calibration		1 to 40 Hz (X MULTIPLIER setting) calibrated; 0.1 to 1 Hz (X MULTIPLIER setting) uncalibrated										
Dial Accuracy												
FREQUENCY Hz (START) dial	Within 3% of full scale from 0.001 Hz to 4 MHz. Within 6% of full scale from 4 MHz to 40 MHz.	Measurements made at an ambient temperature between +15° CC and -35° C after 1 hour warmup.										
STOP FREQUENCY dial	Within 5% of the difference between the start and stop frequencies plus the FREQUENCY Hz (START) dial error	STOP FREQUENCY dial is uncalibrated on the 10 ⁴ MULTIPLIER range.										
Maximum Frequency Ranges for Dial, Sweep Frequency, and Voltage Controlled Frequency (VCF) Modes	<table><tr><td>MULTIPLIER Setting</td><td>Maximum to Minimum Frequency Ratios</td></tr><tr><td>10⁰</td><td>≥500:1</td></tr><tr><td>10¹ - 10²</td><td>≥1000:1</td></tr><tr><td>10¹, 10¹, 10⁻¹, 10⁻²</td><td>≥100:1</td></tr><tr><td>10⁻¹</td><td>≥40:1</td></tr></table>	MULTIPLIER Setting	Maximum to Minimum Frequency Ratios	10 ⁰	≥500:1	10 ¹ - 10 ²	≥1000:1	10 ¹ , 10 ¹ , 10 ⁻¹ , 10 ⁻²	≥100:1	10 ⁻¹	≥40:1	
MULTIPLIER Setting	Maximum to Minimum Frequency Ratios											
10 ⁰	≥500:1											
10 ¹ - 10 ²	≥1000:1											
10 ¹ , 10 ¹ , 10 ⁻¹ , 10 ⁻²	≥100:1											
10 ⁻¹	≥40:1											
Internal Sweep Accuracy		Linear or Logarithmic. Limited by Start and Stop Frequency Specifications; use external frequency counter if greater accuracy is required.										
Sweep Duration		100 s to 0.1 ms in six decades (selected by SWEEP DURATION switch) VARIABLE control overlaps decades.										
Stop Frequency to Swept Stop Frequency Error		Within 2% from 100 s to 1 ms sweep duration. Within 10% from 1 ms to 0.1 ms sweep duration.										
LINEAR SWEEP	0 V to -10 V.	Output impedance 1 kΩ.										

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Internal Sweep (cont)		
OUTPUT Amplitude		
Accuracy	Within 5% from 100 s to 1 ms. Within 10% from 1 ms to 0.1 ms.	
SWEEP TRIGger INPUT		
Input sensitivity	1 V p-p.	
Level	1 V through 10 V.	
Maximum Input	± 20 V	
Manual Trigger		Front-panel control
Voltage-controlled Frequency Input (VCF)		
Nominal Sensitivity (Hz/volt)		= 4 X MULTIPLIER setting per volt. A positive-going voltage increases frequency.
Maximum Frequency		= 40 X MULTIPLIER setting
Minimum Frequency		Maximum frequency divided by VCF range (see Maximum Frequency Ranges for Dial, Sweep Frequency, and Voltage Controlled Frequency (VCF) Modes)
Slew Rate		0.3 V/μs maximum
Input Impedance		10 kΩ.
OUTPUT Signal Amplitude	At least 30 V p-p into an open circuit, at least 15 V into 50 Ω.	
Flatness		
Sine-wave		
0.001 Hz to 40 kHz	Within ±0.5 dB	Typically within ±0.5 dB to 40 MHz. Reference at 10 kHz.
40 kHz to 40 MHz	Within ±2 dB from 40 kHz to 40 MHz.	
Triangle		
0.001 Hz to 40 kHz	Within ±0.5 dB	Reference at 10 kHz.
40 kHz to 40 MHz.	Within ±2 dB.	
Square-wave		
0.001 Hz to 20 MHz	Within ±0.5 dB.	Reference at 10 kHz.
20 MHz to 40 MHz	Within ±2 dB.	
Sine-wave, Triangle, and Square-wave Amplitude Match	Within ±1 dB at 10 kHz.	

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information														
Output ATTENUATOR	<table><tr><th>Attenuator Step</th><th>Maximum Open-circuit Output Voltage (p-p)</th></tr><tr><td>0 dB</td><td>30 V</td></tr><tr><td>-10 dB</td><td>9.5 V</td></tr><tr><td>-20 dB</td><td>3 V</td></tr><tr><td>30 dB</td><td>950 mV</td></tr><tr><td>-40 dB</td><td>300 mV</td></tr><tr><td>50 dB</td><td>95 mV</td></tr></table>	Attenuator Step	Maximum Open-circuit Output Voltage (p-p)	0 dB	30 V	-10 dB	9.5 V	-20 dB	3 V	30 dB	950 mV	-40 dB	300 mV	50 dB	95 mV	
Attenuator Step	Maximum Open-circuit Output Voltage (p-p)															
0 dB	30 V															
-10 dB	9.5 V															
-20 dB	3 V															
30 dB	950 mV															
-40 dB	300 mV															
50 dB	95 mV															
Accuracy	Within ± 0.5 dB/decade															
VARIABLE Control	Provides up to -20 dB additional attenuation to reduce the minimum output signal amplitude to 10 mV															
OFFSET Range																
Into Open Circuit	± 7.5 V	Maximum signal plus offset peak output amplitude of ± 20 V into an open circuit and ± 11.25 V into 50 Ω . Offset defeatable by front-panel control.														
Into 50 Ω	± 3.75 V															
Output Waveforms																
Without Use of SYMMETRY (variable) control		Sine, Triangle, and Square														
With SYMMETRY (variable) Control		Ramps and Pulses. Duty cycle range is $\approx 7\%$ to $\approx 93\%$ for all variable symmetry waveforms below 1 MHz, limited to $\approx 20\%$ to $\approx 80\%$ for triangle and sine-waveforms above 1 MHz. Actuation of SYMMETRY control divides output frequency by approximately 10.														
Triangle																
Symmetry		Typically within 2% from 0.001 Hz to 10 Hz.														
10 Hz to 400 kHz 400 kHz to 40 MHz	Within 1%. Within 5%	On calibrated portion of FREQUENCY Hz dial.														
Linearity		Measured from the 20% point to the 80% point of the waveform. Typically within 2% from 0.001 Hz to 10 Hz.														
10 Hz to 400 kHz 400 kHz to 4 MHz 4 MHz to 40 MHz		Within 1%. Within 2%. Within 10%.														

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
External TRIG/GATE		
Φ LOCK Input (cont)		
Maximum Trigger Frequency	20 MHz.	
GATE		
Minimum Period		75 ns.
Maximum Gated Frequency	20 MHz	For gating multiple-cycle burst of generator waveform.
Φ LOCK		
	100 Hz to 40 MHz. Adjust range $\pm 80^\circ$ from 0 100 Hz to 4 MHz.	Capture range: ± 10 major dial divisions from 100 Hz to 4 MHz; ± 8 major dial divisions from 4 MHz to 40 MHz (40 MHz may not capture, but will track.)
4 MHz to 40 MHz	± 8 major dial divisions	
Lock Range		Generator will lock to a changing external signal, without readjusting the PHASE control within ± 10 major dial divisions from 100 Hz to 4 MHz and within ± 1 MHz from 4 MHz to 40 MHz
PHASE		
Phase Adjustment Range		$\pm 80^\circ$ from 0 001 Hz to 4 MHz
MAN		
		Manual Trigger/Gate front-panel pushbutton
TRIG OUTPUT		
	0 V to 2 V from 50 Ω .	
HOLD		
Drift		10% of p-p output amplitude, hour
Range	0 001 Hz to 400 Hz	

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Output Waveforms (cont)		
Sine-Wave		
Total Harmonic Distortion		Typically $\leq 1\%$ from 0.001 Hz to 20 Hz, measured under the following conditions: Temperature -10°C to -35°C ambient terminated into 50 Ω ; zero offset; ≤ 30 dB attenuation, and with FREQUENCY Hz (START) dial set between 4 and 40.
20 Hz to 40 kHz	0.5%.	
40 kHz to 1 MHz	Greatest harmonic at least 30 dB down.	
1 MHz to 40 MHz	Greatest harmonic at least 20 dB down.	
Square-wave		
RISE AND FALL TIMES	≤ 6 ns 10 ns to 100 ms in 7 steps	Applies to pulse waveforms also
FIXED	measured from 10% to 90%.	
Aberrations	$\leq 5\%$ p-p plus 30 mV into 50 Ω load.	
VARIABLE	10 ns to 100 ms in 7 steps. Measured between the 10% and 90% points of Amplitude; accuracy within 30%. VARIABLE control has $\geq 10\text{X}$ range.	Period of waveform must exceed combined rise and fall times by 20%.
AM INPUT		
Dc to 4 MHz	5 V p-p signal produces 100% modulation of a sine-wave carrier with 5% distortion at 70% modulation.	When driven from a source impedance 600 Ω
4 MHz to 40 MHz	10% distortion at 65% modulation.	Modulating frequencies from 20 Hz to 20 kHz. Modulation frequency bandwidth is dc to 100 kHz. A modulating source impedance of 10 k Ω ensures proper modulation and divides the output amplitude by 2.
Input Impedance		1 M Ω .
External TRIG. GATE		
⊕ LOCK Input		
Input Impedance		10 k Ω .
Sensitivity	-1 V p-p.	
Maximum Input Amplitude		-20 V
TRIG		
LEVEL	-1 V to +10 V.	For triggering a single cycle of generator waveform.
Minimum Period		75 ns.

Table 1-2

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Description
Temperature	
Operating	0° C to -40° C (-40° C to -50° C, forced air required).
Storage	-40° C to +75° C.
Altitude	
Operating	To 15,000 feet (4,570 meters).
Storage	To 50,000 feet (15,250 meters)
Vibration	
Operating and non-operating	0.64 mm (0.025") displacement, 10-50-10 Hz sinewave, 54 minutes
Shock	
Operating and non-operating	50 g's (half sine), 11 ms, 12 shocks
Transportation	Qualified under National Safe Transit Association Test, Procedure 1A Category II.

Table 1-3

PHYSICAL CHARACTERISTICS

Characteristics	Description
Finish	Anodized aluminum panel and chassis
Weight	3.75 pounds (1.7 kg).
Overall Dimensions	Width 5.312" (13.49 cm), Length 12.125" (30.8 cm), Height 5.0" (12.7 cm).

Tektronix FG 504 40MHz Function Generator

The following is an excerpt of *Tektronix 40MHz Function Generator, Model FG 504*, Instruction Manual, May 1982.

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COMMITTED TO EXCELLENCE

PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL.

FG 504
40 MHz
FUNCTION
GENERATOR
(SN B0400000 & ABOVE)

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077
070-2855-00
Product Group 75

Serial Number _____

SPECIFICATION

Introduction

The FG 504 Function Generator provides low distortion sine, square, triangle, ramp, and pulse waveforms over the frequencies from 0.001 Hz to 40 MHz in ten decades. A user-definable custom frequency range is also available. The output amplitude is 10 mV to 30 V peak-to-peak into an open circuit and 5 mV to 15 V peak-to-peak into a 50 Ω load. The output impedance is 50 Ω . The FG 504 may be swept between the START and STOP FREQ dial settings with a linear or logarithmic sweep. The output may be phase locked, gated, or triggered for single cycle output. The output waveform may be shifted $\pm 80^\circ$ from the triggering waveform. The symmetry of the output waveform may also be varied. For the slower frequencies, the output may be held at any level by pushing the front panel button labeled HOLD.

A voltage-controlled frequency (VCF) input controls the output frequency from an external voltage source. The output frequency can be swept above or below the selected frequency, to a maximum of 1000.1, depending on the polarity and amplitude of the VCF input and the selected output frequency. Provision is also made for amplitude modulating the sinewave output from an external source.

The variety of swept and modulated signals available from the FG 504 make it especially useful for such applications as testing amplifier or servo-system response, distortion, and stability. It is useful for fm generation, as a beat frequency oscillator, as a gated triggered or phase-locked logic interface, or as a source for various ramp or pulse waveforms. It is also useful as a source for amplitude modulated signals for various purposes.

SPECIFICATION

Performance Conditions

The following electrical characteristics are valid if the FG 504 is calibrated at an ambient temperature between $+20^\circ\text{C}$ and $+30^\circ\text{C}$ and is operated at an ambient temperature between 0°C and $+50^\circ\text{C}$, unless otherwise noted. Forced air circulation is required at temperatures above $+40^\circ\text{C}$. Allow a one-hour warm-up period before performing verification tests.

Table 1-1

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Frequency		
Range		
Sine-wave, square-wave, and triangle	.001 Hz to 40 MHz calibrated in 10 overlapping steps	
Ramps, pulses, or waveforms requiring use of variable SYMMETRY control		.001 Hz to nominally 4 MHz
Duty Cycle		$\leq 7\%$ to $\geq 93\%$ below 1 MHz $\leq 20\%$ to $\geq 80\%$ above 1 MHz
.5 X 10^1 position of MULTIPLIER switch (User selected timing capacitor)		=400 kHz maximum. A 5 μF capacitor provides a full-scale frequency of ≈ 400 Hz. The factory-installed capacitor gives a 20 Hz to 20 kHz range for the .5 X 10^1 position of the MULTIPLIER switch.

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information										
Frequency (cont)												
Resolution		1 part in 10 ⁴ of full-scale setting using the FREQUENCY VERNIER control, as measured with a frequency counter.										
Stability		Applies to calibrated portion of the FREQUENCY Hz dial only.										
Time	≤0.05% for 10 minutes ≤0.1% for 1 hour ≤0.5% for 24 hours	The instrument must be at a constant ambient temperature between 0° C and +50° C and checked after a 1-hour warmup.										
Temperature		See Dial Accuracy										
Dial Calibration		1 to 40 Hz (X MULTIPLIER setting) calibrated; 0.1 to 1 Hz (X MULTIPLIER setting) uncalibrated.										
Dial Accuracy												
FREQUENCY Hz (START) dial	Within 3% of full scale from 0.001 Hz to 4 MHz. Within 6% of full scale from 4 MHz to 40 MHz.	Measurements made at an ambient temperature between +15° CC and +35° C after 1 hour warmup.										
STOP FREQUENCY dial	Within 5% of the difference between the start and stop frequencies plus the FREQUENCY Hz (START) dial error.	STOP FREQUENCY dial is uncalibrated on the 10 ⁴ MULTIPLIER range.										
Maximum Frequency Ranges for Dial, Sweep Frequency, and Voltage Controlled Frequency (VCF) Modes	<table><tr><td>MULTIPLIER Setting</td><td>Maximum to Minimum Frequency Ratios</td></tr><tr><td>10⁴</td><td>≥500:1</td></tr><tr><td>10³—10²</td><td>≥1000:1</td></tr><tr><td>10¹, 1, 10⁻¹, 10⁻²</td><td>≥100:1</td></tr><tr><td>10⁻¹</td><td>≥40:1</td></tr></table>	MULTIPLIER Setting	Maximum to Minimum Frequency Ratios	10 ⁴	≥500:1	10 ³ —10 ²	≥1000:1	10 ¹ , 1, 10 ⁻¹ , 10 ⁻²	≥100:1	10 ⁻¹	≥40:1	
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10 ⁴	≥500:1											
10 ³ —10 ²	≥1000:1											
10 ¹ , 1, 10 ⁻¹ , 10 ⁻²	≥100:1											
10 ⁻¹	≥40:1											
Internal Sweep Accuracy		Linear or Logarithmic. Limited by Start and Stop Frequency Specifications; use external frequency counter if greater accuracy is required.										
Sweep Duration		100 s to 0.1 ms in six decades (selected by SWEEP DURATION switch). VARIABLE control overlaps decades.										
Stop Frequency to Swept Stop Frequency Error		Within 2% from 100 s to 1 ms sweep duration. Within 10% from 1 ms to 0.1 ms sweep duration.										
LINEAR SWEEP	0 V to -10 V.	Output impedance 1 kΩ.										

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Internal Sweep (cont)		
OUTPUT Amplitude		
Accuracy	Within 5% from 100 s to 1 ms. Within 10% from 1 ms to 0.1 ms.	
SWEEP TRIGger INPUT		
Input sensitivity	1 V p-p.	
Level	1 V through 10 V.	
Maximum Input	+ 20 V.	
Manual Trigger		Front-panel control.
Voltage-controlled Frequency Input (VCF)		
Nominal Sensitivity (Hz/volt)		=4 X MULTIPLIER setting per volt A positive-going voltage increases frequency.
Maximum Frequency		=40 X MULTIPLIER setting.
Minimum Frequency		Maximum frequency divided by VCF range (see Maximum Frequency Ranges for Dial, Sweep Frequency, and Voltage Controlled Frequency (VCF) Modes)
Slew Rate		0.3 V/ μ s maximum.
Input Impedance		10 k Ω .
OUTPUT Signal Amplitude	At least 30 V p-p into an open circuit, at least 15 V into 50 Ω .	
Flatness		
Sine-wave		
0.001 Hz to 40 kHz	Within ± 0.5 dB.	Typically within ± 0.5 dB to
40 kHz to 40 MHz	Within ± 2 dB from 40 kHz to 40 MHz.	40 MHz. Reference at 10 kHz.
Triangle		
0.001 Hz to 40 kHz	Within ± 0.5 dB.	Reference at 10 kHz.
40 kHz to 40 MHz.	Within ± 2 dB.	
Square-wave		
0.001 Hz to 20 MHz	Within ± 0.5 dB.	Reference at 10 kHz.
20 MHz to 40 MHz	Within ± 2 dB.	
Sine-wave, Triangle, and Square-wave Amplitude Match	Within ± 1 dB at 10 kHz.	

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information														
Output ATTENUATOR	<table><tr><th>Attenuator Step</th><th>Maximum Open-circuit Output Voltage (p-p)</th></tr><tr><td>0 dB</td><td>30 V</td></tr><tr><td>-10 dB</td><td>9.5 V</td></tr><tr><td>-20 dB</td><td>3 V</td></tr><tr><td>30 dB</td><td>950 mV</td></tr><tr><td>-40 dB</td><td>300 mV</td></tr><tr><td>50 dB</td><td>95 mV</td></tr></table>	Attenuator Step	Maximum Open-circuit Output Voltage (p-p)	0 dB	30 V	-10 dB	9.5 V	-20 dB	3 V	30 dB	950 mV	-40 dB	300 mV	50 dB	95 mV	
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-10 dB	9.5 V															
-20 dB	3 V															
30 dB	950 mV															
-40 dB	300 mV															
50 dB	95 mV															
Accuracy	Within ± 0.5 dB/decade.															
VARIABLE Control	Provides up to -20 dB additional attenuation to reduce the minimum output signal amplitude to 10 mV.															
OFFSET Range																
Into Open Circuit	± 7.5 V	Maximum signal plus offset peak output amplitude of ± 20 V into an open circuit and ± 11.25 V into 50 Ω . Offset defeatable by front-panel control.														
Into 50 Ω	± 3.75 V															
Output Waveforms																
Without Use of SYMMETRY (variable) control		Sine, Triangle, and Square														
With SYMMETRY (variable) Control		Ramps and Pulses. Duty cycle range is $\approx 7\%$ to $\approx 93\%$ for all variable symmetry waveforms below 1 MHz. limited to $\approx 20\%$ to $\approx 80\%$ for triangle and sine-waveforms above 1 MHz. Actuation of SYMMETRY control divides output frequency by approximately 10.														
Triangle																
Symmetry		Typically within 2% from 0.001 Hz to 10 Hz.														
10 Hz to 400 kHz	Within 1%	On calibrated portion of FREQUENCY Hz dial.														
400 kHz to 40 MHz	Within 5%.															
Linearity		Measured from the 20% point to the 80% point of the waveform. Typically within 2% from 0.001 Hz to 10 Hz.														
10 Hz to 400 kHz	Within 1%.	Within 1%. Within 2%. Within 10%.														
400 kHz to 4 MHz	Within 2%.															
4 MHz to 40 MHz	Within 10%.															

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Output Waveforms (cont)		
Sine-Wave		
Total Harmonic Distortion	0.5%.	Typically $\leq 1\%$ from 0.001 Hz to 20 Hz, measured under the following conditions: Temperature -10°C to -35°C ambient terminated into 50 Ω ; zero offset; ≤ 30 dB attenuation, and with FREQUENCY Hz (START) dial set between 4 and 40.
20 Hz to 40 kHz	Greatest harmonic at least 30 dB down.	
40 kHz to 1 MHz	Greatest harmonic at least 20 dB down.	
1 MHz to 40 MHz		
Square-wave		
RISE AND FALL TIMES FIXED	≤ 6 ns 10 ns to 100 ms in 7 steps measured from 10% to 90%	Applies to pulse waveforms also.
Aberrations	$\leq 5\%$ p-p plus 30 mV into 50 Ω load	
VARIABLE	10 ns to 100 ms in 7 steps. Measured between the 10% and 90% points of Amplitude; accuracy within 30%. VARIABLE control has $\geq 10\times$ range.	Period of waveform must exceed combined rise and fall times by 20%.
AM INPUT		
Dc to 4 MHz	5 V p-p signal produces 100% modulation of a sine-wave carrier with 5% distortion at 70% modulation.	When driven from a source impedance 600 Ω .
4 MHz to 40 MHz	10% distortion at 65% modulation	Modulating frequencies from 20 Hz to 20 kHz. Modulation frequency bandwidth is dc to 100 kHz. A modulating source impedance of 10 k Ω ensures proper modulation and divides the output amplitude by 2.
Input Impedance		1 M Ω .
External TRIG/GATE Φ LOCK Input		
Input Impedance		10 k Ω .
Sensitivity	± 1 V p-p.	
Maximum Input Amplitude		± 20 V
TRIG		
LEVEL	-1 V to $+10$ V.	For triggering a single cycle of generator waveform.
Minimum Period		75 ns.

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
External TRIG/GATE/ Φ LOCK Input (cont)		
Maximum Trigger Frequency	20 MHz.	
GATE		
Minimum Period		75 ns.
Maximum Gated Frequency	20 MHz.	For gating multiple-cycle burst of generator waveform.
Φ LOCK	100 Hz to 40 MHz. Adjust range $\pm 80^\circ$ from 0 100 Hz to 4 MHz.	Capture range: ± 10 major dial divisions from 100 Hz to 4 MHz; ± 8 major dial divisions from 4 MHz to 40 MHz (40 MHz may not capture, but will track.)
4 MHz to 40 MHz	± 8 major dial divisions.	
Lock Range		Generator will lock to a changing external signal, without readjusting the PHASE control, within ± 10 major dial divisions from 100 Hz to 4 MHz and within ± 1 MHz from 4 MHz to 40 MHz
PHASE		
Phase Adjustment Range		$\pm 80^\circ$ from 0.001 Hz to 4 MHz
MAN		Manual Trigger/Gate front-panel pushbutton.
TRIG OUTPUT	0 V to 2 V from 50 Ω .	
HOLD		
Drift		10% of p-p output amplitude, hour
Range	0.001 Hz to 400 Hz.	

Table 1-2

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Description
Temperature	
Operating	0°C to +40°C (+40°C to +50°C: forced air required).
Storage	-40°C to +75°C.
Altitude	
Operating	To 15,000 feet (4,570 meters).
Storage	To 50,000 feet (15,250 meters).
Vibration	
Operating and non-operating	0.64 mm (0.025") displacement, 10-50-10 Hz sinewave, 54 minutes.
Shock	
Operating and non-operating	50 g's (half sine), 11 ms, 12 shocks.
Transportation	Qualified under National Safe Transit Association Test, Procedure 1A Category II.

Table 1-3

PHYSICAL CHARACTERISTICS

Characteristics	Description
Finish	Anodized aluminum panel and chassis.
Weight	3.75 pounds (1.7 kg)
Overall Dimensions	Width 5.312" (13.49 cm), Length 12.125" (30.8 cm). Height 5.0" (12.7 cm).